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ULTRATHIN NITRIDED GATE OXIDES - GROWTH, MEASUREMENT AND CHARACTERIZATION

A Thesis

Presented to

The Faculty of the Department of Chemical

Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Rohini Ranganathan

May 2002

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ABSTRACT

This thesis focuses on the physical characterization of nitric oxide (NO) annealed ultrathin nitrided gate oxides in the thickness range of 16-32 Å. In this work the effect of organic contamination on thickness measurement was studied. This work examines the effect of recipe parameters such as oxidation temperature, oxidation time, and NO anneal temperature on the physical characteristics of the gate oxide. A simple method using reoxidation was used to estimate the amount of nitrogen incorporated. The experimental details for the physical characterization of nitrided gate oxides are outlined in this work.

The work concludes that the amount of nitrogen incorporated in the gate oxide is mainly a function of the NO anneal temperature independent of the starting thickness of the gate oxide and increases with increase in anneal temperature.

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LIST OF SYMBOLS

Å : Angstrom

D_{it} : Interface Trapped Charge Density

ε : Dielectric Constant

k : Extinction Coefficient

n_i : Refractive Index

nm : Nanometer

N, N_2 : Nitrogen

NH_3 : Ammonia

NO : Nitric Oxide

N_2O : Nitrous Oxide

O_2 : Oxygen

Q_{BD} : Charge to Breakdown

Si : Silicon

SiO_2 : Silicon dioxide

t : Thickness

µm : micron

V_{BD} : Breakdown Voltage

V_g : Gate voltage

V_T : Threshold Voltage

LIST OF ABBREVIATIONS

AES : Auger Electron Spectroscopy

ALD : Atomic Layer Deposition

APM : Ammonia Peroxide Mixture

C-V : Capacitance-Voltage

CVD : Chemical Vapor Deposition

DOE : Design of Experiments

EEPROM : Electrically Erasable Programmable Read Only Memory

FTIR : Fourier Transform Infrared Spectroscopy

HF : Hydrofluoric Acid

HPM : Hydrochloric Peroxide Mixture

IC : Integrated Circuit

ITRS : International Technology Roadmap for Semiconductors

I-V : Current-Voltage

JVD : Jet Vapor Deposition

MEIS : Medium Energy Ion Scattering

MOSFET : Metal Oxide Semiconductor Field Effect Transistor

NGOX : Nitrided Gate Oxide

NRA : Nuclear Reaction Analysis

NTRS : National Technology Roadmap for Semiconductors

pMOS : p-type Metal Oxide Semiconductor

RCA : Radio Corporation of America

ROST : Rapid Optical Surface Treatment

RTP : Rapid Thermal Processing

SC-1 : Standard Clean 1

SC-2 : Standard Clean 2

SE : Spectroscopic Ellipsometry

SIA : Semiconductor Industry Association

SIMS : Secondary Ion Mass Spectroscopy

SPM : Sulfuric Peroxide Mixture

SVG : Silicon Valley Group

TDDB : Time Dependent Dielectric Breakdown

ULSI : Ultra Large Scale Integration

VTR : Vertical Thermal Reactor

XPS : X-ray Photoelectron Spectroscopy

CHAPTER ONE
INTRODUCTION

1.1 Ultrathin Oxides

In the last three decades. telecommunication. computer. and semiconductor industries have progressed at an unmatched exponential pace in both performance and productivity. The fuel behind this remarkable progress has been the large-scale integration of devices on silicon. The feature sizes of the MOSFET. invented in 1962. have been scaled down dramatically. Moore's law. which states that the number of devices on a chip will double every 18 months. has held amazingly true for more than a decade. The scalability of MOSFET's has taken integration from a few bits to a billion bits/chip permitting system on a chip with giga-scale integration capability that has resulted in lower power consumption and lower cost of manufacturing.

The schematic of a MOSFET is shown in **Figure 1** [1]. As the name implies. in field effect devices. a voltage at the gate controls the current between the source and the drain [2]. The electric field due to the voltage at the gate alters the resistance of the 'channel' connecting the source and drain terminals to achieve this change in current. In a MOSFET. the gate is a conducting layer of silicon grown over a thin layer of SiO_2. This sandwich of metal (highly doped Si). oxide (SiO_2) and lightly doped Si (Substrate) is the core of the MOS Field Effect Transistor. The MOSFET is brought into conduction by applying a voltage on the gate in such a way as to attract the minority carriers in the substrate to the Si/SiO_2 interface. The channel is said to be in inversion when the number voltage applied at the gate to achieve channel inversion is called the threshold voltage for that transistor.

The "heart" of the MOSFET is the gate dielectric. The gate oxide or the gate dielectric is an insulator between the gate and the channel regions of the MOSFET. The gate oxide is extremely critical for the proper functioning of MOS transistors. It determines how the device will perform and the device reliability. The gate oxide thickness is the most important vertical dimension in the active area of the transistor since it determines the threshold voltage of the device. This requires that the thickness and composition of the dielectric should be under very tight control to obtain a good yield.

ULSI devices demand ultrathin oxide films with high reliability for scaling down the minimum device dimension. The scalability of MOS devices can be primarily attributed to the fact that silicon has a native gate dielectric SiO_2. It has been possible to scale down the gate dielectric thickness from ~200 nm to ~2-3 nm in manufacturing with reduction in minimum feature size.

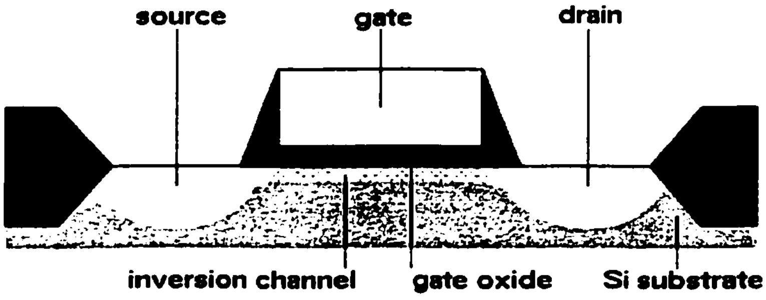


Figure 1: Schematic of a MOSFET. Source: Sze, S.M. (1988)

The gate dielectric or gate oxide is arguably the biggest challenge facing the physical scaling of the MOSFET [3]. The scaling of the gate oxide in MOS technology has rapidly accelerated over the past few years [4]. To demonstrate how these dimensions will continue to be reduced, the time line for the reduction lithography and the equivalent oxide thickness is given (ITRS, 2000 Update) in **Table 1**. Equivalent oxide thickness, t_{eq}, refers to the thickness of any dielectric scaled by the ratio of its dielectric constant to that of silicon dioxide (where $\varepsilon_{oxide} = 3.9$) such that

$$t_x = t_{eq} * \varepsilon_x / \varepsilon_{oxide}$$

where t_{eq} and t_x are the equivalent oxide and physical thickness, respectively, and ε_{oxide} and ε_x are respectively the dielectric constant of silicon dioxide and that of the other dielectric. If the gate dielectric were to remain SiO_2, by the year 2014, assuming a constant rate of scaling, its thickness would be only 5-6 Å, or about 2 atomic layers, whereas with an alternate dielectric x, with $\varepsilon_x > \varepsilon_{oxide}$, a thicker layer could be used.

Table 1: Roadmap for technology and equivalent dielectric thickness. Source: ITRS, 2000 Update

Production Year	Minimum feature size (µm)	Equivalent dielectric thickness (Å)
1999	0.18	19-25
2001	0.13	15-19
2004	0.09	12-15
2008	0.06	8-12
2011	0.04	6-8
2014	0.03	4-6

1.2 Growth of Ultrathin Oxides

The ultrathin gate oxides are grown in furnaces or rapid thermal processors (RTP). The hot-wall horizontal diffusion furnace was the backbone of the IC industry until the mid-1980's when vertical furnaces began to replace them in production. Vertical furnaces offer several technological advantages over the horizontal furnaces. although the horizontal furnaces offer high productivity at low cost. A 4-stack horizontal furnace tool in 1998 cost approximately \$1.0 million. while one vertical furnace costs nearly the same. The reason for using vertical furnaces despite a 4x cost factor is that it offers a) improved thermal and process gas control; b) improved particle performance: and c) improved automation capabilities [5].

The advantage of vertical furnaces over horizontal furnaces is that the radial temperature gradient across the wafer is smaller since the wafers are parallel to the horizontal plane. The wafer spacing is equal between all the wafers since each wafer sits on the bottom of a slot in the fused silica pedestal rather than balancing on its edge in a slot of the horizontal furnace. Another advantage of the vertical furnace is that it offers better ambient and particle control than the horizontal furnaces. Vertical furnaces have a loading station where the loading and unloading atmosphere can be controlled [5].

Recently rapid thermal processors have replaced vertical furnaces in some critical applications. Rapid thermal processing is a single wafer. fast ramp thermal processing capability that can be used to heat a wafer from room temperature to 1100°C in a matter of seconds. The advantages of RTP over furnaces are reduced thermal budget. single wafer processing, higher temperature processing, and improved gas distribution. RTP is widely used when control of the processing atmosphere is crucial, when very short anneal times are required, or when reduced thermal budget is important. Despite these advantages RTP has not replaced vertical furnaces in all applications. Vertical furnaces continue to be used in production because of lower cost for certain applications [5].

1.3 Measurement of Ultrathin Oxides

The accurate measurement of oxide film thickness is critical in ULSI processing. The thickness of gate oxides in ULSI MOSFETs, which are in the range of 20-40Å have to be tightly controlled, as it directly determines the device threshold voltage V_T. Various techniques are available for measuring oxide thickness such as a) optical interference, b) ellipsometry, c) capacitance, and d) physical thickness measurement. Optical interference and ellipsometry are the most widely used techniques for thickness measurement in production. Some of the commercial measuring systems currently used in production are Thermawave Opti-Probe and KLA ASET-F5. These instruments are capable of measuring the oxide thickness with an accuracy of +/-0.03Å and with a repeatability of +/-0.07 Å [5].

1.4 Limitations of Ultrathin Oxides

For many years, thermally grown silicon dioxide has been the primary gate dielectric and has demonstrated robustness and effectiveness. Advances in technology have resulted in a continued decrease of SiO_2 film thickness. The 1997 National Technology Roadmap for Semiconductors identified several potential deficiencies for SiO_2 films below 2 nm [6]. The major deficiencies are tunneling and inability to prevent boron penetration from the p^+ gate layer during a high-temperature processing step. Mobility degradation is another serious concern for ultrathin oxides.

The size reduction in MOS circuitry dictated by the advancing technology requires the use of thin gate dielectrics with high performance and reliability. The dielectric material used in the fabrication of the gate is a key factor in determining the long-term reliability of the device. In a MOS transistor. the gate dielectric must sustain a substantial voltage difference applied between the gate electrode and the underlying silicon substrate. With extremely small dimensions. electrons can tunnel in the gate material when the device is toggled between on and off positions. in normal usage. The electrons can create the undesirable long-term effect of threshold voltage drift of the transistor. and eventually this could cause circuit failure. This problematic behavior can be a limiting factor for thermally grown SiO_2 gates with thickness in the range below 80-100 Å [7]. Also. boron diffusion from the heavily doped p^+ poly silicon gate through the thin gate dielectric can cause undesirable shifts in the threshold voltage of the devices causing them to fail.

The problem of electron tunneling was attributed to structural imperfections in the interfacial Si/SiO_2 region. where the stereo-chemical differences between SiO_2 and Si create high stress/strain in the transition layer. To alleviate this stress. it was proposed to introduce a small quantity of nitrogen in this transitional region that would reduce the number of distorted Si-O bonds and therefore improve the electrical behavior [7].

In addition, another important advantage obtained by the introduction of nitrogen at the Si/SiO_2 interface is that it behaves as a barrier to boron atoms, impeding their penetration into the gate material, which is typically observed when p^+ poly silicon is used in p-MOSFET's. The presence of nitrogen in the gate dielectric showed better electrical properties like increased V_{BD} and Q_{BD}. Some of the disadvantages reported for nitrided oxides include: a) increased fixed charge and interface charge density, and b) reduced channel mobility [5]. Despite these disadvantages, the nitrided oxides exhibit characteristics superior to those of the SiO_2 gate dielectrics and appear to be the dielectric of the future.

In this work, an attempt has been made to study the effect of recipe parameters like oxidation temperature, oxidation time, and NO anneal temperature on the physical characteristics of ultra thin nitrided gate oxides in the thickness range between 16 and 32Å. Also, the effect of organic contamination on the thickness measurements of ultrathin oxide films was studied. From the experiments carried out it is possible to get an idea of the achievable thickness, standard deviation, and concentration of nitrogen incorporated for the different gate oxides.

CHAPTER TWO
LITERATURE REVIEW

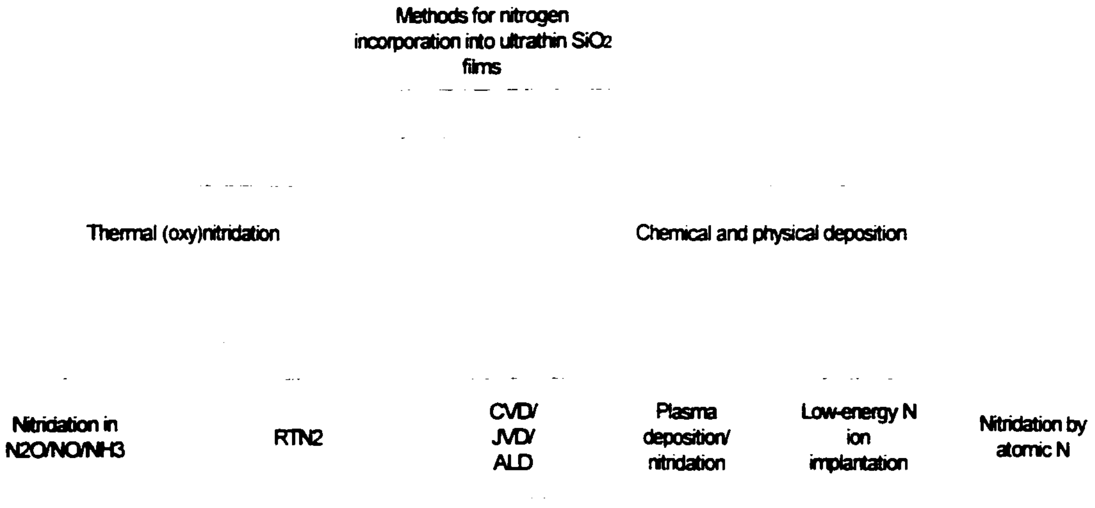
SiO_2 has been used as the primary gate dielectric material in field effect devices since 1957, when the usefulness of the Si/SiO_2 material system was first demonstrated by C.J. Frosch and L. Derick [4]. Thermally grown SiO_2 films have many applications in silicon devices and technology, including gate dielectrics of MOSFETs and tunnel insulators for nonvolatile memories such as electrically erasable programmable read only memory (EEPROM). As the SiO_2 films were made thinner, several technological and reliability problems arose in this very thin regime [8]. Issues related to the manufacture of integrated circuits included the dielectric thickness variation, penetration of impurities from the gate (e.g., boron) into the gate dielectric, and the reliability and lifetimes of devices made with these ultrathin films. Incorporation of nitrogen into the SiO_2 layer has been shown to greatly improve the properties of the resulting oxide film [4].

2.1 Nitrided Gate Oxides

Nitrided gate oxides exhibit several properties superior to conventional thermal SiO_2, suppression of boron penetration from the p^+ poly-Si gate, smaller charge trapping, large charge to breakdown ratio, and enhanced reliability [9]. Since the presence of nitrogen imparts these properties to the nitrided gate oxide layer, it is important to precisely insert nitrogen into the film at the desired position and concentration. The dielectric constant of the nitrided gate dielectric increases linearly with the percentage of nitrogen from $\varepsilon(SiO_2) = 3.8$ to $\varepsilon(Si_3N_4) = 7.8$. Most SiO_xN_y films grown currently are lightly "doped" with N

(<10 at. %). Nitrogen may be incorporated into SiO_2 using either thermal oxidation/annealing or chemical and physical deposition methods as shown in **Figure 2.**

Figure 2: Different nitridation methods. Source: Gusev et al., 1999


Methods for nitrogen incorporation into ultrathin SiO2 films
Thermal (oxy)nitridation
Chemical and physical deposition
Nitridation in N2O/NO/NH3
RTN2
CVD/ JVD/ ALD
Plasma deposition/ nitridation
Low-energy N ion implantation
Nitridation by atomic N

Thermal nitridation of SiO_2 in NO or N_2O generally results in a relatively low concentration of nitrogen in the films, of the order of 10^{15} N atoms/cm^2. Since nitrogen content increases with temperature, thermal nitridation is typically performed at high temperatures, i.e., > 800°C. For more heavily N-doped SiO_2 films, other methods of deposition such as chemical vapor deposition, jet vapor deposition, atomic layer deposition, or nitridation by energetic nitrogen particles (plasma, N atoms, or ions) can be used [10]. These nitridation methods can be performed at lower temperatures, ~300-400°C. However, low temperature deposition methods may result in non-equilibrium films, and subsequent thermal processing steps are often required to improve film quality and minimize defects and induced damage [11].

Incorporation of nitrogen in the gate oxide can be carried out in two ways. Ultrathin nitrided silicon dioxide films can be grown by direct exposure of Si to gases containing N and O (NO or N_2O) or by nitridation of ultrathin silicon dioxide films in nitrogen containing gases. NH_3 and N_2O have been widely used as nitridation gases. NH_3 nitrided thermal oxides show superior boron-stopping properties compared to pure oxides due to the high nitrogen concentration incorporated in the nitrided oxides. but these dielectric films suffer from hydrogen related electron trapping, which makes them less ideal for MOSFET applications [10]. N_2O grown or N_2O annealed dielectrics have shown superior electrical properties and reliability [12]. but they present poor boron-stopping properties due to their low levels of nitrogen incorporation. A definite advantage of using N_2O is the low thermal budget required to obtain an oxide of desired thickness in adequate processing times. It is thought that nitrogen incorporation in the N_2O process is driven by NO species. which is a product of N_2O molecule dissociation [10]. The N_2O molecule. in fact. likely dissociates into NO (4.7%). N_2 (64.3%). and O_2 (31%) according to calculations [13]. Such by-products act in competition: while NO incorporates nitrogen. O_2 continues the oxidation by reacting with the silicon substrate and N_2 reduces the partial pressure of the nitriding species. increasing the thermal budget. The parallel oxidation explains the observed increase in oxide thickness during annealing in N_2O. The choice of starting with thermal growth in NO or thermal annealing of oxides in NO seems to be the natural one. since NO is one of the products of thermal dissociation of N_2O at high temperatures. and it is considered as the main mobile. nitriding species in the cases of direct growth in N_2O or oxide annealing in N_2O [14].

NO-grown oxides require even lower thermal budgets than those used in N_2O processing. to introduce the same quantity of nitrogen into the gate oxide. In addition. NO-grown oxides also exhibit a higher amount of nitrogen incorporation than in the case with N_2O. at similar processing conditions. The higher nitrogen incorporation efficiency of NO is probably due to the high reactivity of the products of dissociation of NO with Si(100). compared to nitrogen incorporation in Si through the reaction of N_2O with Si(100) which is thermodynamically a less favorable reaction [15]. An additional advantage of using NO annealed SiO_2 is that it allows for varying nitrogen profiles in the dielectric without causing a simultaneous increase in oxide thickness.

Excellent electrical properties are demonstrated by the NO-grown gate oxides. confirming the importance of nitrogen introduction into the SiO_2 gate material and at the interface. The nitrogen introduced at the Si/SiO_2 interface by using a NO atmosphere during oxidation can effectively create a barrier to Boron penetration. The advantage obtained by nitrogen accumulation in the interfacial region is somewhat diminished by a decrease in gate reliability because of the accumulation of boron within the gate oxide [7]. **Figure 3** shows the effect of the interface layer in stopping boron penetration and producing an accumulation of boron atoms within the gate oxide. Such accumulation results in degradation of gate charge trapping properties. However. while such degradation is certainly an undesirable effect. the overall performance and reliability behavior of NO-grown gate dielectric material is always found to be superior to SiO_2 gate oxides of similar thickness.

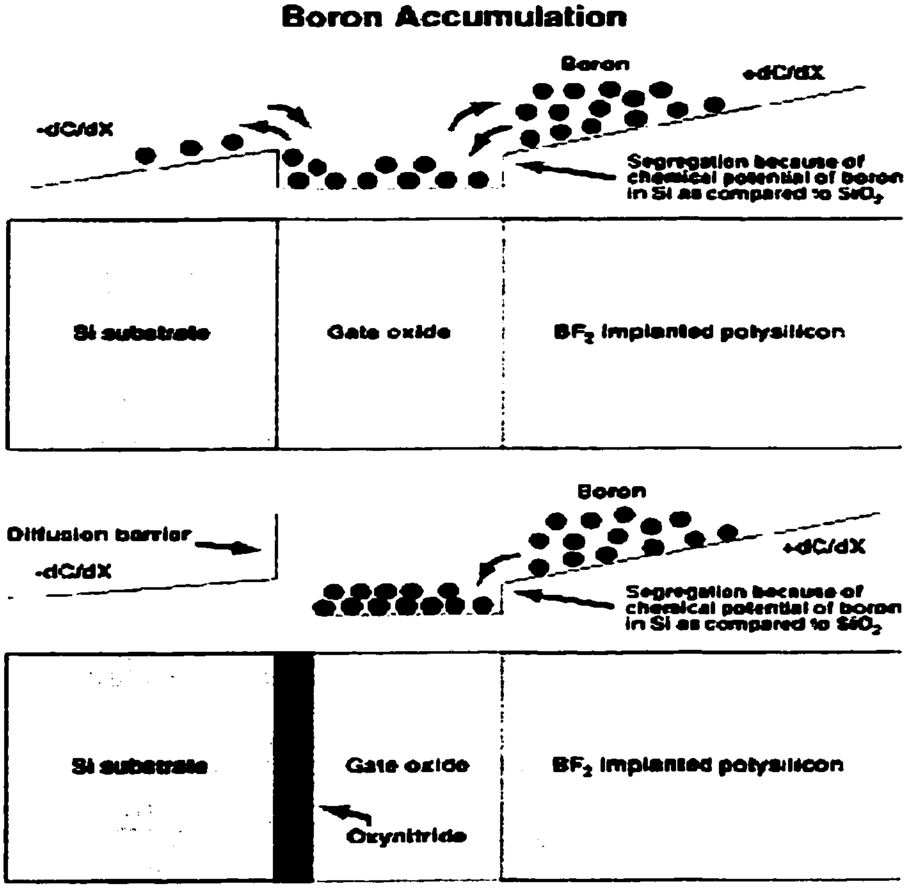

Boron Accumulation
Boron
+dC/dX
-dC/dX
Segregation because of chemical potential of boron in Si as compared to SiO2
Si substrate
Gate oxide
BF2 implanted polysilicon
Boron
Diffusion barrier
-dC/dX
+dC/dX
Segregation because of chemical potential of boron in Si as compared to SiO2
Si substrate
Gate oxide
Oxynitride
BF2 implanted polysilicon

Figure 3: Comparison of gate oxide layer with and without interface layer. Source: Leonarduzzi, G.D. et al., Semiconductor International, 1998.

The amount of nitrogen incorporated in the nitrided gate oxide is very critical. The incorporation of very large amounts of nitrogen leads to a reduction of boron penetration but can cause threshold voltage shifts and mobility and transconductance degradation, which are dependent on nitrogen concentration and the concentration profile. This is due to the positive charge that results from the nitrogen incorporation into the SiO_2 matrix.

The nitrogen incorporated near the Si/SiO$_2$ interface also reduces mobility of the device [4].

It has been agreed upon by a number of investigators that NO processing incorporates in the dielectric the desired properties of NH$_3$ and N$_2$O processes [13.15.17]. Unlike N$_2$O processing it provides dielectrics with a high concentration of nitrogen and unlike NH$_3$ processing it provides nitrogen in a hydrogen-free environment.

2.2 Nature and Distribution of Nitrogen in Nitrided Gate Oxide Films

Through a number of studies. it has been observed that different process conditions or nitrogen source gases can introduce nitrogen at different positions. relative to the poly electrode and the underlying channel layer [8.10.13.16.17]. This led investigators to try positioning the nitrogen atoms within the gate to optimize both electrical and reliability performance.

Leonarduzzi. G.D. et al. [7] generated three different nitrogen profiles within a p$^+$ poly pMOS device with a gate thickness of about 50Å:

- Case A: Nitrogen peak located at the SiO$_2$/Si interface. generated by growing oxide in pure O$_2$ ambient. followed by a short NO anneal
- Case B: Nitrogen peak at the poly/SiO$_2$ interface. generated by nitrogen implantation. followed by N$_2$ anneal (30 min at 900°C) to drive in the nitrogen at the desired interface

- Case C: Nitrogen peaks at both the interfaces. generated by a combination of the two methods

These three profiles were compared with a pure sample of SiO_2 gate oxide of the same thickness. The boron-trapping behavior of the three cases is shown in **Figure 4.**

In all the three cases. they found that the electrical properties improved because of the presence of the boron barrier. independent of its position within the gate area. **Figure 4a** represents the control. where boron can easily diffuse into the gate during activation. resulting in degradation of interface quality and reliability. **Figure 4b** shows the blocking effect of a nitrogen barrier at the Si/SiO_2 interface. which reduces the voltage shift. but accumulation of boron atoms within the gate oxide causes charge trapping. **Figure 4c** shows an improved scenario. where the nitrogen barrier positioned at the poly/SiO_2 greatly reduces the boron penetration into the gate oxide. **Figure 4d** behaves as a "double wall" nitrogen barrier. The boron atoms that penetrate the poly/SiO_2 interface are effectively trapped in the gate oxide leading to a poorer performance compared to the case presented in **Figure 4c**.

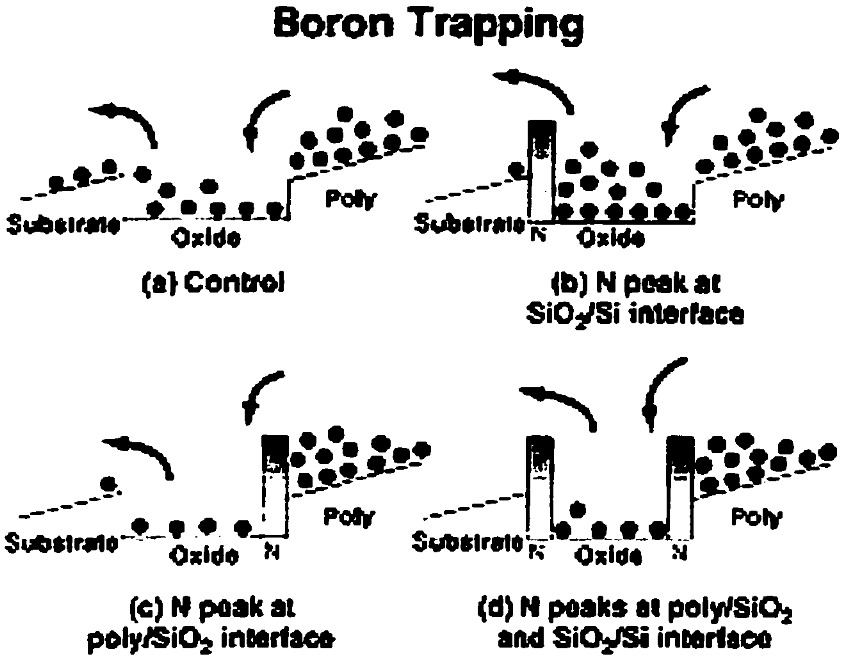

Boron Trapping
Substrate
Oxide
Poly
(a) Control
Substrate
N
Oxide
Poly
(b) N peak at SiO2/Si interface
Substrate
Oxide
N
Poly
(c) N peak at poly/SiO2 interface
Substrate
N
Oxide
N
Poly
(d) N peaks at poly/SiO2 and SiO2/Si interface

Figure 4: The impact of boron penetration on gates (a) without any interface layers, (b) with N at the SiO_2/Si interface, (c) N at the poly/SiO_2 interface and (d) N at both interfaces. Source: Leonarduzzi,G.D. et al., Semiconductor International, 1998.

Over the past few years, several techniques, such as secondary ion mass spectroscopy (SIMS), nuclear reaction analysis (NRA), medium energy ion scattering (MEIS), x-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), Fourier transform infrared spectroscopy (FTIR), spectroscopic ellipsometry (SE), and others have been utilized to study nitrogen concentrations, depth profiles, nitrogen bonding, and microstructure of nitrided oxide films [10].

SIMS is one of the most commonly used techniques to characterize the nitrogen profile and concentration in ultrathin gate oxides. It is an expensive process and costs about $400/hour. SIMS technology enables ion beam driven profiling of wafer implants down to ultra-shallow levels. It provides the most accurate and reliable identification of matrices and elements with the highest possible resolution. SIMS uses "primary ion" bombardment of the sample surface as the probing beam. This ion beam bombardment sputter-etches the sample material, causing the emission of "secondary ions." The secondary ions represent the qualitative sample composition. The sample material is continuously eroded during the measurement, and the secondary ion intensity is recorded as a function of time - the "raw depth profile." Scanning the focused primary ion beam allows uniform material removal, gating techniques to avoid "edge" effects, and spatially resolved depth profiles.

Many researchers have studied the depth profile of nitrogen in nitrided silicon dioxide films [8,13,16,17]. In 1994, Okada, Y. et al., was the first to grow NO nitrided gate dielectric in a conventional horizontal furnace [13]. In their work they used a 105Å thick gate oxide grown at 950°C in O_2 +3% HCl as a control oxide. For the NO nitrided dielectrics, this oxide was annealed with 2.5% NO in an inert gas for 28 min at various temperatures. As a reference, 105Å N_2O nitrided gate dielectric was grown by annealing 80Å oxide at 950°C in N_2O for 28 min. Using SIMS they found that the NO nitrided gate oxide provided a much tighter nitrogen distribution than the N_2O nitrided gate oxide as shown in **Figure 5.** Also, the nitrogen peak is slightly inside SiO_2 for the N_2O annealed gate dielectric whereas it is slightly inside the silicon substrate for the NO annealed gate dielectric.

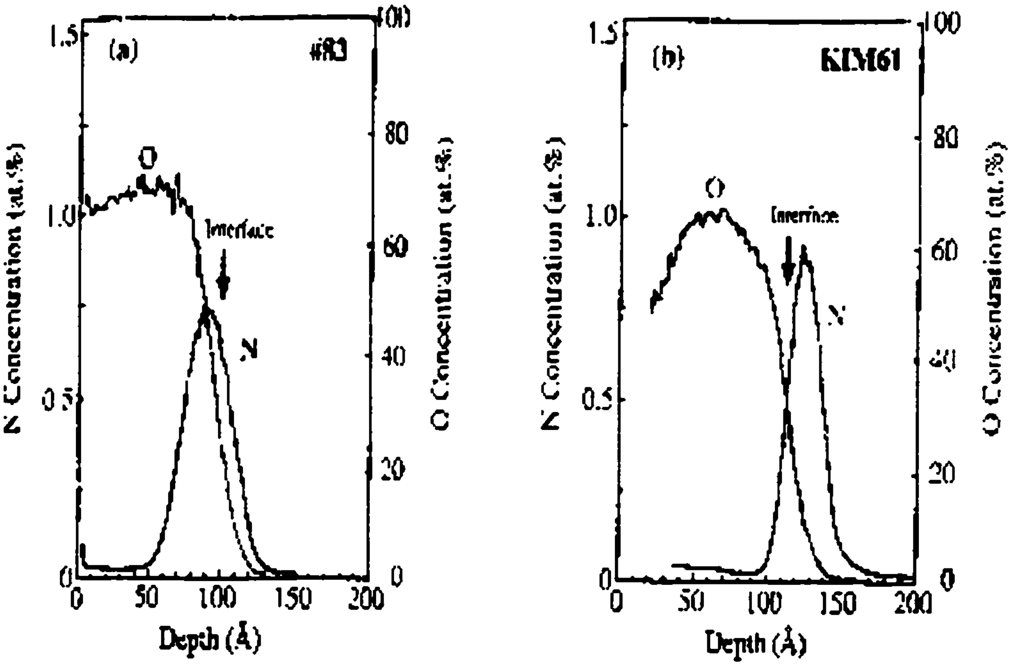


Figure 5: SIMS profiles of (a) N_2O and (b) NO oxynitride grown at 950°C. Source: Okada, Y. et al., 1994

In 1996, Lu et al., compared the nitrogen depth profiles for ~50Å nitrided gate oxide films grown by thermal oxy-nitridation of Si in N_2O both in a furnace and in an RTP reactor, and in O_2 followed by NO [18]. As seen in **Figure 6,** the depth profiles measured by SIMS are different depending on the processing conditions. The NO annealed film had the highest concentration of nitrogen incorporated near the SiO_2/Si interface. The RTP N_2O film also showed nitrogen located near the interface, whereas the furnace grown film had a broader nitrogen depth distribution.

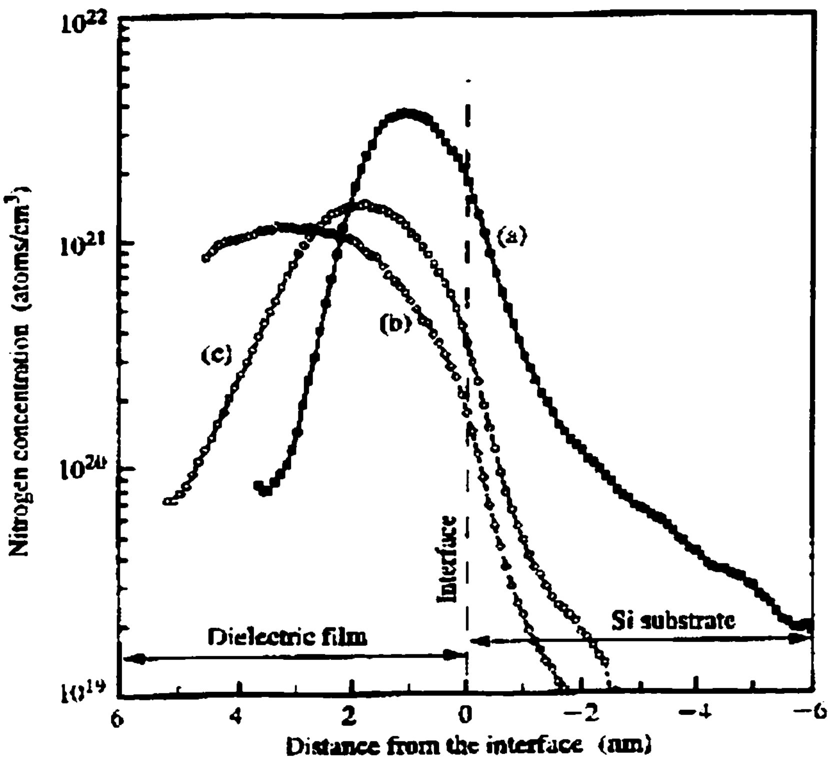


Figure 6: Depth profiles of N measured by SIMS for (a) SiO_2 film annealed in NO at 950°C for 1 hr; (b) film grown in a furnace at 850°C for 110 min; and (c) film grown by RTP in N_2O at 1000°C for 2.3 min. Source: Lu et al., 1996

Gerardi, C. et al. (1999) studied the physical and chemical properties of NO annealed thin steam oxides grown in commercial furnaces in comparison with the N_2O process [19]. They found that the quantity of nitrogen incorporated at the interface with the N_2O anneal was less than that obtained with the 10% NO, 30 minutes. Also a 50% NO/N_2 process yielded more than twice the corresponding value of N_2O. The authors found that nitrogen incorporation was negligible in the case of N_2 treatment. The results of their study of nitrogen incorporation under various conditions are shown in **Table 2.**

Table 2: Process description, final thickness, and nitrogen content. Source : Gerardi et al., 1999

Process Description	Final Thickness (nm)	N concentration (SIMS) (Atoms/cm^2)
10% NO, 15min, 850°C	7.5	6.4×10^{14}
10% NO, 30min, 850°C	7.4	1.1×10^{15}
10% NO, 60min, 850°C	7.5	1.6×10^{15}
50% NO, 60min, 850°C	7.5	2.0×10^{15}
100% N_2, 60min, 850°C	7.7	1.8×10^{15}
100% N_2O, 20min, 900°C	7.6	9.0×10^{14}

Using SIMS, Gerardi et al. found that the nitrogen peak in the N_2O process is slightly shifted towards the oxide bulk with respect to the NO case as shown in **Figure 7** [19]. They attributed both broader nitrogen distribution and peak shift to a different nitridation process that takes place in the N_2O treatment. The oxidizing species resulting from the dissociation of N_2O continues to react with the silicon substrate, causing a broader interface with additional oxide growth.

Since the reactivities of NO, N_2O, and O_2 with Si, SiO_2, and SiO_xN_y are quite different, properly chosen sequences of thermal reactions with Si can lead to nitrided gate oxide films with different nitrogen concentrations and profiles, and therefore electrical properties. Gusev et al. (1999) found that most of the reactions are very condition-dependent: as pressure, film thickness, heating mode (conventional furnace vs. rapid thermal), etc. are changed, the nitrogen profiles can change significantly [10]. So, it can be seen that the nitrogen profile in the nitrided gate oxide film is a function of the conditions under which the nitrogen is incorporated.

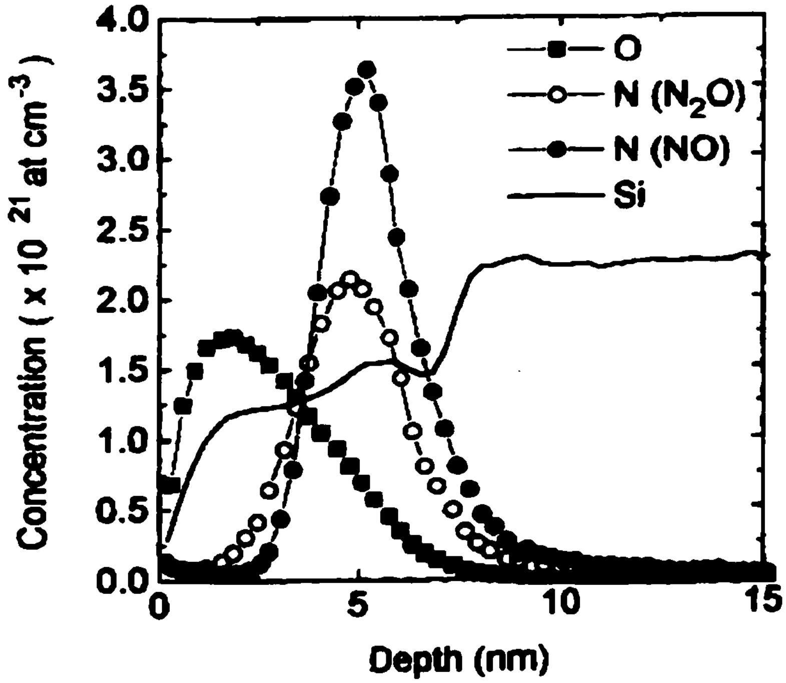


Figure 7: Quantitative SIMS profiles of nitrogen distributions in NO (30min, 10%) and N_2O annealing. Source: Gerardi et al., 1999.

Investigators [20,21] showed that the frequently observed nitrogen accumulation near the interface tends to degrade the channel mobility of MOS transistors. Yoshinao, M. et al. (2000) studied the reoxidation effects on the chemical bonding states of nitrogen accumulated at the nitrided oxide/silicon interface [22]. They used a reoxidation process to change the nitrogen location in the depth profile. The nitrogen accumulated at the interface just after NO nitridation moved away from the interface by 0.5-1.5 nm as the reoxidation proceeded. **Figure 8** shows the nitrogen depth profiles of three samples as determined by SIMS. In Sample A. nitrogen accumulated near the Si/SiO$_2$ interface. After reoxidation. the interfacial nitrogen was incorporated into the bulk SiON films by ~0.5nm from the interface as seen in Sample B. After reoxidation at a higher temperature. the nitrogen was incorporated deeper in the oxide (1-2nm) as shown in Sample C.

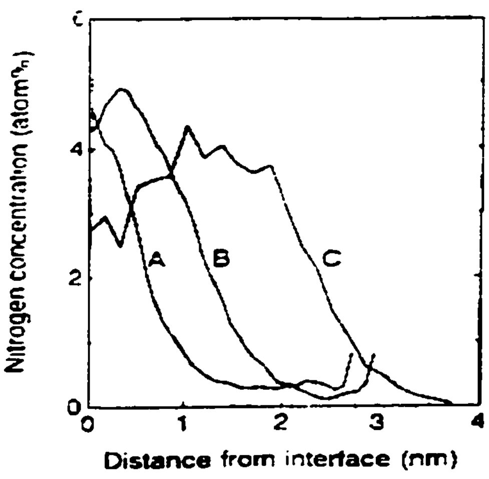


Figure 8: Nitrogen depth profile determined for samples reoxidized to various degrees. Source: Yoshinao, M. et al., 2000.

It has been shown that the presence of nitrogen in the gate oxide slows down the oxidation process. This has been demonstrated by Narayanan. S. (2001) [23]. In this work nitrided and non-nitrided gate oxide wafers were reoxidized and the rate of reoxidation was compared. It was determined that the rate of reoxidation for nitrided gate oxides was much slower than the non-nitrided gate oxides. This is an inexpensive method of determining whether nitrogen has been incorporated in the gate oxide.

Investigations were carried out by Bhat et al., on the impact of nitrogen concentration and distribution on the electrical and reliability properties of rapid-thermally NO-annealed oxides [15]. They studied the chemical composition of NO-nitrided SiO_2 gate dielectrics and studied their impact on the electrical properties by varying NO anneal condition which results in varying nitrogen distribution and concentrations. They found that the NO nitrided oxides had several attractive features like excellent interface endurance, negligible charge trapping and improved Q_{BD} over O_2 and N_2O grown oxides under high field stress. In their study, they found that the non-uniform distribution of nitrogen in the bulk of the dielectric causes an asymmetric polarity dependence in Q_{BD} values of NO nitrided SiO_2 gate dielectrics annealed under varying conditions. **Figure 9** shows the impact of nitridation condition on the breakdown characteristics of the dielectric under +/- V_g at 100mA/cm^2. It is seen that with a 10s NO nitridation, Q_{BD} values under $+V_g$ are significantly enhanced over control and do not increase any further with increasing nitrogen concentration at the interface. Under $+V_g$, the dielectric breakdown is related to defect creation and propagation to the injecting surface where the accumulation of defects leads to the weakening of the interface. However, it has been seen that in NO annealed oxides, the nitrogen at the interface acts as a barrier to hydrogen atoms that migrate to the cathode and cause the interface to weaken [24]. However, the trend observed for the case of $-V_g$ is different. Q_{BD} values increase with nitridation for a short (10s) NO anneal at which point a turnaround is observed and the Q_{BD} decreases with further nitridation. According to Bhat et al., the fact that the impact of over nitridation is seen only under $-V_g$ is possibly related to the non-uniform nitrogen distribution in the bulk of the dielectric.

Since the nitrogen concentration is higher at the Si/SiO$_2$ interface, the injected energetic electrons from the gate, under the -V_g stress, interacts directly with the nitrided bulk region near the anode causing the Q_{BD} values to be degraded [15].

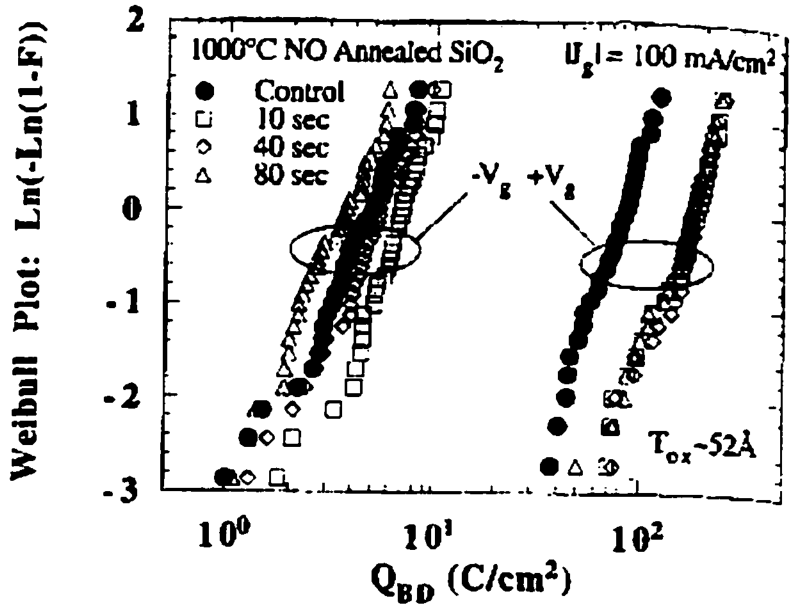


Figure 9: Weibull plots of Q_{BD} of MOS capacitors with SiO$_2$ and (10,40 and 80s) NO-annealed SiO$_2$ gate dielectrics. Source: Bhat et al., 1995.

Gerardi et al. (2000) studied the effects of nitridation with NO on the leakage current of thin gate oxides [25]. The samples they used had NO surface concentrations of (a) 6.4×10^{14} atoms/cm^2, (b) 11.0×10^{14} atoms/cm^2, (c) 16.0×10^{14} atoms/cm^2, and (d) 20.0×10^{14} atoms/cm^2. They found that increase in annealing time and NO/N$_2$ ratio led to an increment of nitrogen incorporation. The leakage currents measured by the authors across the oxides under both accumulation and inversion conditions are shown in **Figure**

10. The I-V characteristics on the right side and on the left side of the figure were obtained under accumulation and inversion, respectively. The continuous lines are the theoretical curves. They showed that the nitrogen-rich layer existing at the SiO_2/Si interface lowers the leakage tunneling through the dielectric for electrons injected from that interface.

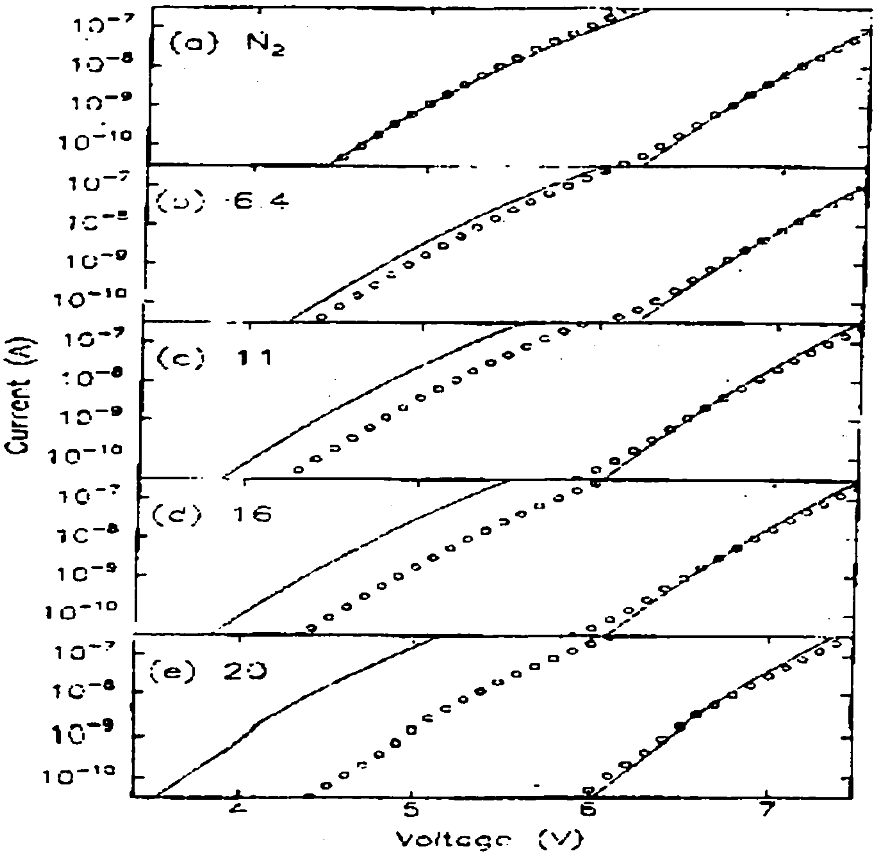


Figure 10: I-V data recorded under gate and substrate injection. Source: Gerardi et al., 2000.

2.3 Factors Affecting Gate Oxide Quality and Measurement

One of the most significant challenges for ULSI process engineers is to develop and maintain a gate oxide process that results in uniform and reproducibly high quality gate dielectrics that are only few atomic layers thick. Some of the factors that can adversely impact the control of oxide thickness uniformity include (1) pre-oxidation cleaning effects: (2) the presence of native oxide films on the silicon surface prior to gate oxidation; (3) growth of oxide during the ramp up and ramp down; and (4) the residual water content of the O_2 gas in dry oxidation processes [26]. Major advances in wafer cleaning, furnace technology, and the introduction of rapid thermal oxidation have gone a long way to achieve the growth of uniform thin gate oxides. The two key issues that must be satisfied to permit the utilization of thin oxides are: (1) it must be possible to grow ultrathin oxides uniformly across the wafer; and (2) MOSFETs with ultrathin oxides must exhibit adequate reliability characteristics under normal circuit operating conditions.

Cleaning is the most frequently repeated step in IC production. A wet cleaning procedure precedes the formation of the gate dielectric by silicon oxidation or deposition of a dielectric. This pre-gate cleaning has been shown to affect surface contamination and roughness, both of which can strongly degrade the final device performance [27]. Cleaning processes traditionally used prior to gate oxidation result in the growth of chemical oxides. The presence of chemical oxides has become a serious concern in the control of the thickness and electrical characteristics of advanced gate dielectrics. In an ideal case, we would like all the processes to take place continuously so that there is no time for the native oxide to grow on the passivated surface. But in reality, continuous processing is not possible. There is generally a queue time between two processes during which the wafers are temporarily stored. There may be sufficient time for the wafers to be contaminated by organics from the containers and atmospheric ambient. During gate oxidation, the insertion temperature into the furnace is typically 700-750°C [27]. The temperature is then ramped up to the growth temperature (~15°C/min). So, it is necessary to control oxide growth and surface micro-roughness during ramp up. All these factors influence the thickness measurement and characteristics of ultrathin gate oxides.

2.3.1 Surface Terminations

The chemical state in which a surface is left subsequent to a clean is as important as the clean itself because a surface that becomes recontaminated before the next processing step will not be useful. The best cleaning techniques are therefore the ones that chemically passivate the surface in the act of cleaning it.

Depending on the cleaning chemistries used, silicon can have different surface terminations. There are two predominant ways to clean and passivate silicon surfaces chemically. The first is to grow a thin layer of oxide in the act of cleaning. This is best accomplished using the RCA clean [27], which was formulated by Kern and Puotinen at RCA in 1965. The original RCA clean was a two-step process comprising of SC-1 (Standard Clean 1) and SC-2 (Standard Clean 2) as shown in **Table 3.**

The peroxide solutions in the RCA clean leave a few angstroms of oxide on the surface that prevents recontamination of silicon. Such surfaces are hydrophilic in nature and are easily wetted by aqueous solutions.

Table 3: Original RCA Clean. Source: Kern. W., 1993

Step	Chemical Composition	Function
Standard Clean 1 (SC-1)	$H_2O:H_2O_2:NH_4OH$ 5 : 1 : 1	Removes organic surface films and trace metals.
Standard Clean 2 (SC-2)	$H_2O:H_2O_2:HCl$ 6 : 1 : 1	Removes alkali ions and metallic hydroxides.

A second option to clean and passivate the surface is to dissolve the surface oxide completely in dilute hydrofluoric acid. This is achieved by the modified RCA clean where an additional step of treating the wafers with dilute HF is carried out after SC-2 at the end. The hydrogen-terminated surfaces are hydrophobic in nature and are not wetted by aqueous solutions. Both hydrophilic and hydrophobic surface cleans affect the morphology of the silicon surface and causes increase in surface roughness [27].

The RCA clean results in the growth of a few angstroms of chemical oxide. which can lead to increased thickness measurements. An RCA cleaning process with an additional HF treatment at the end results in less oxide growth but affects the surface roughness. This surface roughness can lead to a large standard deviation in thickness measurement.

2.3.2 Native Oxide

Chemical oxides. also known as native oxides are generated by aqueous oxidative chemistries such as SPM (Sulfuric acid-hydrogen peroxide mixture). APM (Ammonia-hydrogen peroxide mixture). and HPM (Hydrochloric acid-hydrogen peroxide mixture). With advances in ULSI miniaturization. native oxide formation on a silicon surface and interface control is becoming critical to device performance [28]. The extent to which the native oxide growth affects the subsequent processes like gate oxide growth and electrical characteristics of the devices is not completely understood.

Studies have been carried out on the growth kinetics of oxides on wafer surfaces with different surface terminations at room and elevated temperatures to gain a better understanding of the impact of pre-existing chemical oxides on the thermal oxide growth [29]. They found that at room temperature. the oxide grows faster on the HF last processed wafer than those covered by a layer of chemical oxide. Ultimately the thickness for wafers of both terminations converge and become comparable when the oxide thickness reaches 9Å after about 390 hours as shown in **Figure 11**.

From their studies. Guan et al.. found that chemical oxides contribute only a very moderate increase to the thickness of subsequently grown thermal oxides. They found this to be true regardless of the preparation conditions of both chemical and thermal oxide. They came up with possible explanations to describe their observations. According to them. it could be possible that the chemical oxide acts as a diffusion barrier, slowing the thermal oxidation rate. However, results indicated that the oxidation kinetics for 25-45Å oxides fall in the linear regime of the Deal-Grove model for the temperatures used. So the process is reaction limited and chemical oxide cannot act as a diffusion barrier. But at room temperature the chemical oxide acts as a diffusion barrier.

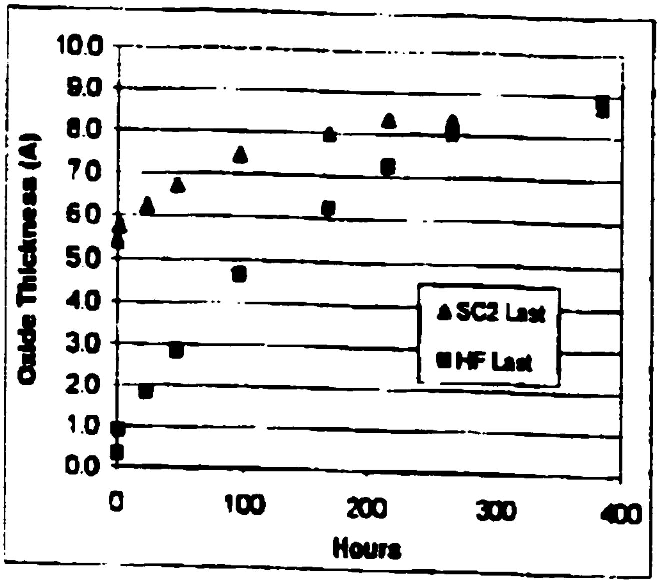
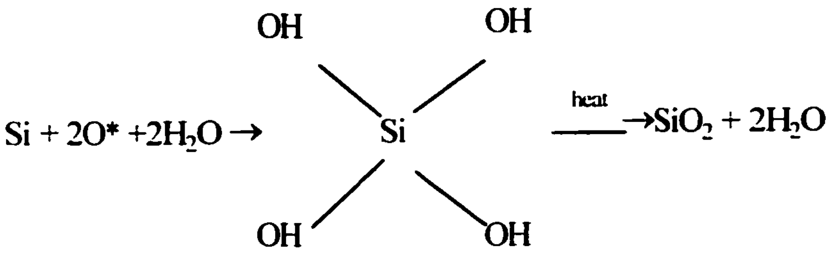


Figure 11: Kinetics of native oxide growth at room temperature in a fab atmosphere. Source: Guan et al., 1999

Another possible explanation by Guan et al., is that the compositional and optical properties of chemical oxides differ from those of thermal oxides as shown in **Figure 12,** and that high temperatures will densify the chemical oxides. Oxidation of silicon in an aqueous medium is likely to form hydrated silicic acid. It is likely that the chemical oxide is composed of large aggregates of hydrated silicic acid instead of SiO_2 to form a layer which may measure up to 15Å. Each hydrated silicic acid molecule upon subsequent thermal treatment will lose two molecules of water and the thickness of the chemical oxide will decrease such that it accounts for less than 1Å of the total gate oxide thickness.

Thus they concluded that the contribution of chemical oxide generated in oxidative pre-gate clean chemistries to the thickness of gate oxides < 20 Å may not be as significant as believed. If this is the case. then the current practice of HF-last pre-gate clean processing for the preparation of advanced gate stacks to achieve an equivalent oxide thickness <15 Å may not be necessary.


Si + 2O* +2H₂O →
OH
OH
Si
OH
OH
heat
→SiO₂ + 2H₂O

Hydrated Silicic Acid

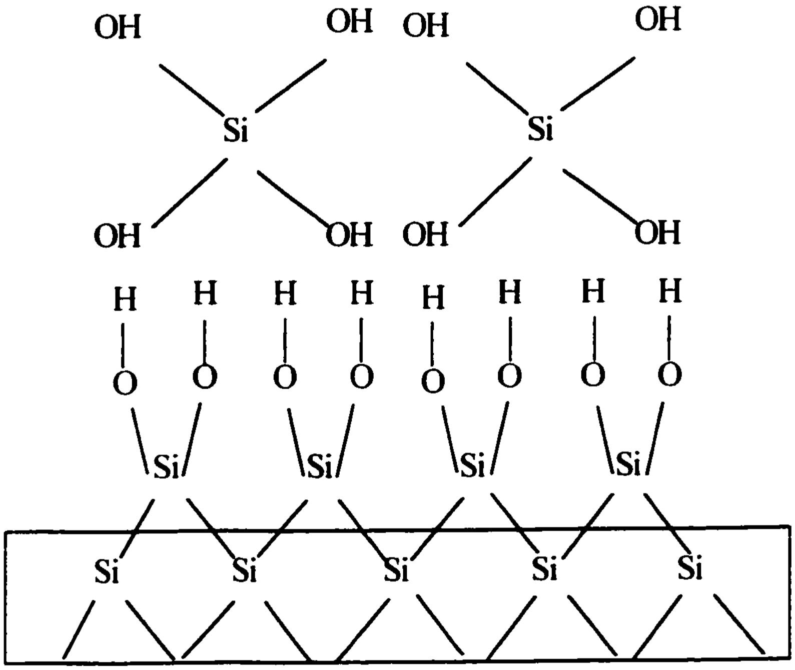

OH
OH
OH
OH
Si
Si
H
O
Si

Figure 12: Suggested model for the chemical oxide formation in an oxidative aqueous medium.

Source: Guan et al., 1999

Electrical characteristics of MOS field-effect transistors are found to be adversely affected by disorder of the oxide-semiconductor interface [27]. In order to improve device performance and reliability, and accurately measure the ultra thin oxides, it is becoming necessary to prepare a well-defined, native oxide free, and atomically flat surface prior to various advanced processes.

2.3.3 Queue Time and Ambient

Queue time is the amount of time a wafer waits at a work center before a job is performed on it. Time windows between special wet etch and furnace operations are specified by technology development engineers to prevent native oxide growth or contamination effects on the wafer surface. For example, a strong dependence between the formation of undesirable interfaces between conductive layers and the waiting time after the wet-etch process were observed. This leads to contact failures, and low and unstable yields [30]. Organic contamination has also been identified as a possible origin of a degraded gate oxide quality [31]. Organic pickup during IC processing is difficult to avoid. Transportation and storage of wafers in plastic boxes results in potential organic contamination. Various process steps can be clustered in vacuum tools, but Si surfaces handled in a vacuum environment are vulnerable to organic contamination. Organic contamination is generally found in different forms. They can be chemically bound to the surface, physically adsorbed from exposure, or come from storage in a vacuum cluster [32]. During queue time, there is sufficient time to contaminate wafers. Organic contamination on the wafer surface leads to errors in thickness measurements of thin oxides.

The total thickness of the gate dielectric film comprises the native oxide grown after the pre-clean, oxide grown during ramp up, oxide grown during thermal oxidation, oxide grown during the annealing step. and oxide grown during ramp down. It is therefore necessary to minimize the growth of native oxide after the pre-clean and the oxide growth during the furnace ramp up and ramp down. Also. it is necessary to minimize the queue time to ensure that organic contamination on the wafer surface is minimized and results in better thickness measurements.

CHAPTER THREE
HYPOTHESIS AND JUSTIFICATION

SiO_2 has been used as the gate dielectric for metal-oxide-semiconductor field effect transistors. or MOSFETs for more than 30 years. As the SiO_2 gate dielectric was made thinner. new technological problems arose. These problems include the dielectric thickness variation. penetration of impurities from the gate (e.g.. boron) into the gate dielectric. and the reliability and lifetimes of devices made with these ultrathin films [4].

As the SiO_2 films are made thinner. a tighter tolerance is required of its thickness. The presence of organic contamination on the wafer surface causes a variation in the thickness of ultrathin oxides and leads to errors in measurement. For example. consider a 30Å oxide with a total tolerance of +/-2Å. The allowable variation in the oxide thickness is required to be less than 20% of the tolerance. This implies that the precision of the thickness measurement should be within +/-0.4Å. The presence of organic contamination on the surface becomes unacceptable for these ultrathin films.

As SiO_2 films are made thinner. the gate leakage current through the film increases exponentially [4]. This exponential increase in gate leakage current with decreasing dielectric thickness is one of the major contributors leading to the limited extendibility of SiO_2 as the gate dielectric in the 15-20Å regime.

The incorporation of nitrogen into the SiO_2 films has been used to eliminate a number of problems. The use of p^+ gates for CMOS processes was first introduced to reduce short-channel effects and lower threshold voltages as the devices were pushed into the submicron regime [4]. However. with the use of boron as the dopant for the p+ gates. dopant diffusion and its subsequent penetration into the gate dielectric have become a problem [33]. Boron penetration shifts the threshold voltage of MOS devices to more positive values. Nitrogen incorporation into the oxide film may be used to retard the effects of boron penetration.

The positioning of nitrogen in the gate dielectric is very important. High temperature processing incorporates more nitrogen in the gate oxide. This could reduce mobility in the channel region and affect the devices. This requires the 'NO' anneal temperature to be optimized to ensure that the positive aspects of nitrogen incorporation be utilized.

In this work. the effect of recipe parameters such as dry oxidation time. dry oxidation temperature. and 'NO' anneal temperature on the physical characteristics of ultrathin nitrided gate oxides was studied. The effect of organic contamination on thickness measurements was also investigated. From the experiments carried out it is possible to determine the achievable thickness. standard deviation. and nitrogen incorporated for the different gate oxides. A simple method using reoxidation described in Section 2.2 was used to determine the amount of nitrogen incorporated in the ultrathin nitrided gate oxides.

CHAPTER FOUR
EXPERIMENTAL METHODS

The aim of this research work was to study the growth. measurement. and physical characteristics of 'NO' annealed ultrathin nitrided gate oxides in the thickness range between 16 and 32 Å. The recipe parameters that were studied include dry oxidation time. dry oxidation temperature. and anneal temperature. In addition. the effect of organic contamination on the thickness measurements of ultrathin oxide films was investigated.

4.1 Equipment Used

The equipment used in this work include the ROST tool. FSI Mercury® spray processor. SVG vertical thermal reactor. STEAG rapid thermal processor. and Thermawave Opti-Probe. The ROST tool was used to study the effect of organic contamination on thickness measurements. The FSI Mercury Spray Processor was used to perform the pre-gate cleans. The SVG Vertical Thermal Reactor was used to perform the gate oxidation and anneal steps. The STEAG Heatpulse 8800 Rapid Thermal Processor was used to reoxidize the nitrided gate oxide wafers. The metrology tool used to measure thickness was the Thermawave Opti-Probe. A brief description of these tools is discussed below.

Rapid Optical Surface Treatment (ROST) tool: This tool was used to study the effect of surface organic contamination on the thickness measurements of ultrathin oxide films. The ROST tool is a surface preparation tool that performs wafer conditioning as a pre-step prior to thickness measurements. A low-temperature rapid photo-thermal processor is designed to provide uniform light and heat energy over the entire wafer surface. The ROST process chamber contains a high-energy lamp array, an IR thermocouple for measurement of the effective wafer temperature, and a water-cooled processing chamber. These elements provide the required light and temperature conditions to ensure consistent and uniform wafer surface conditioning. The tool is capable of reaching temperatures up to 360°C. A schematic of the effect of surface treatment using the ROST tool is shown in **Figure 13.**

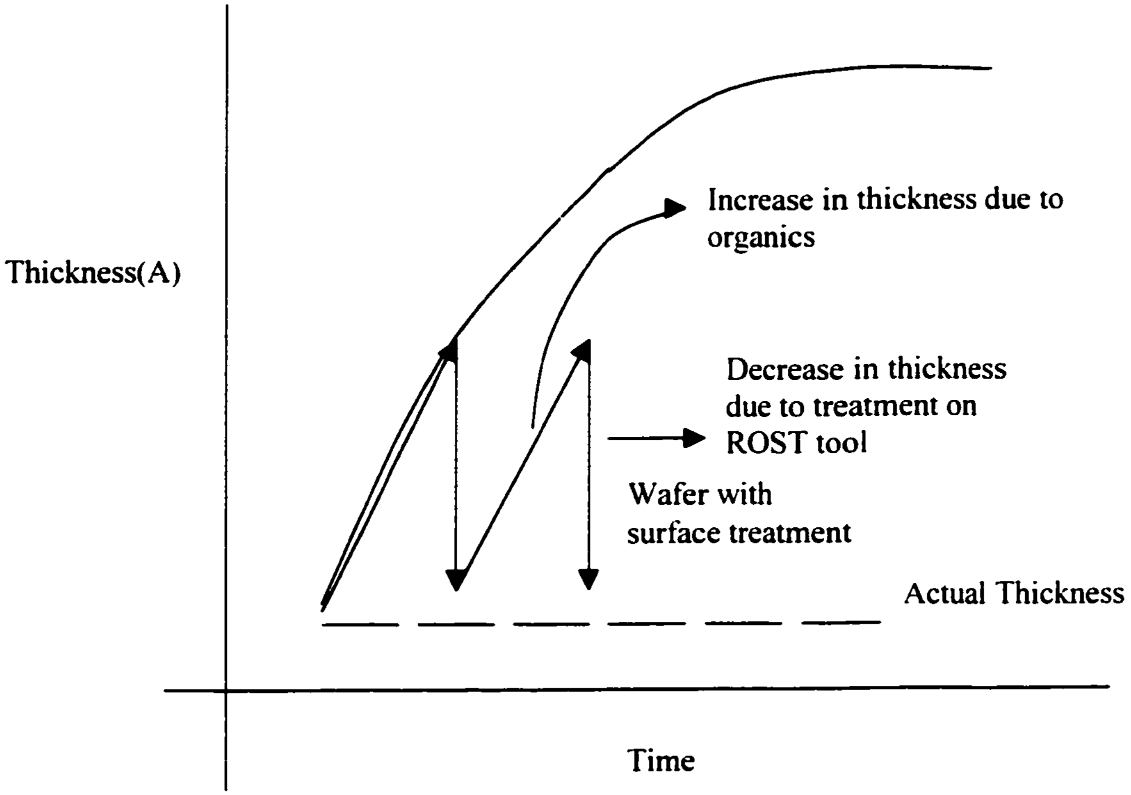

Thickness(A)
Increase in thickness due to organics
Decrease in thickness due to treatment on ROST tool
Wafer with surface treatment
Actual Thickness
Time

Figure 13: Schematic of the effect of surface treatment using ROST

The ROST tool is shown in **Figure 14.**

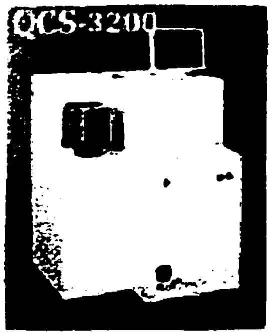


Figure 14: ROST tool. Source: http://www.qcsolutions.com/

FSI Mercury® MP: This tool was used to perform the pre-gate oxidation cleans on the wafers. The FSI Mercury® MP is a spray-processing tool used for cleaning silicon wafers. Depending on the type of clean. the tool uses a variety of chemicals and rinses and dries the wafers. The operation is computer controlled. The FSI Mercury® MP functions as a batch processor. The wafers are placed in cassettes and cleaned in batches. Each cassette can hold up to 25 wafers and up to 4 cassettes can be used in the process chamber. The wafers are sprayed with chemicals to process them as the cassettes are spun on the turntable in the process chamber. After processing. the wafers and chamber are rinsed with deionized (DI) water and dried with nitrogen gas (Source: FSI Mercury® Users Manual). The FSI Mercury® MP is shown in **Figure 15.**

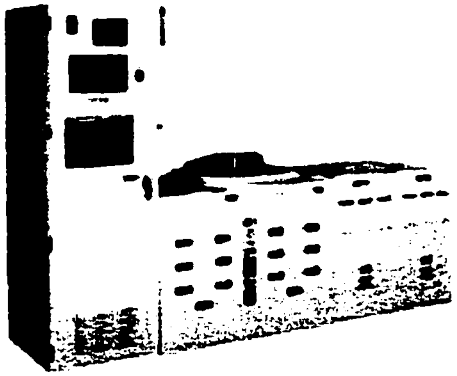


Figure 15: FSI Mercury®MP. Source: http://www.fsi-intl.com

Vertical Thermal Reactor 7000 Series: A schematic of a vertical furnace is shown in **Figure 16.** The heater element usually consists of 3 independent heating zones. By proper control of the zones it is possible to obtain a flat temperature zone of +/- 0.5°C for up to 30 inches in length. Such a long flat zone allows for up to 150 wafers per batch. A water-cooled, stainless steel jacket surrounds the furnace and keeps the exterior cool. The process tube used is usually fused silica. The fused silica tower is used to hold the wafers in a horizontal position. Temperature measurement and control is accomplished by placing thermocouples in the furnace. The gas injection hardware is required to bring controlled levels of process gas into the tube.

The wafers are loaded into the fused silica tower from a cassette by a robotic mechanism. When the loading is complete the tower moves into the furnace. The wafers are inserted into the furnace hot zone at low temperature (600-700°C) to avoid damage due to thermal stress. Once the wafers are in the furnace, the temperature is slowly ramped to the desired process temperature. After reaching the process temperature, the temperature is allowed to stabilize before the process begins. After the process is completed, the wafers are slowly cooled until they reach a safe temperature for removal from the furnace [5].

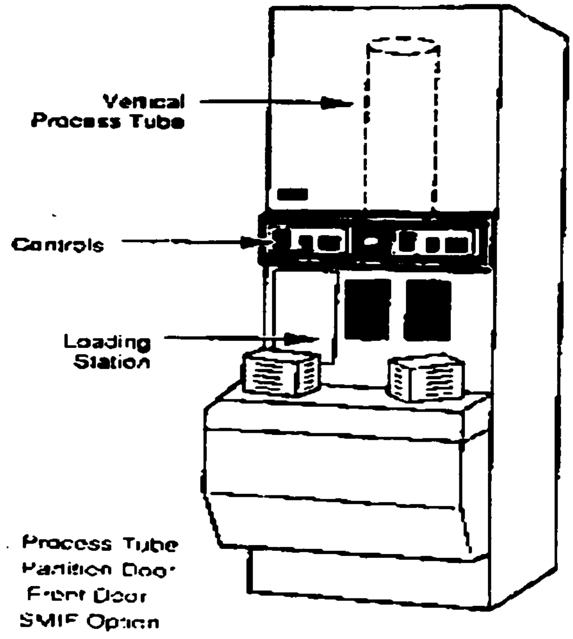

Vertical Process Tube
Controls
Loading Station
Process Tube
Partition Door
Front Door
SMIF Option

Figure 16: Schematic of a vertical furnace. Source: Wolf, S., 2000

Thermawave Opti-Probe: The metrology tool used to measure the thickness of the wafers was the Thermawave Opti-Probe 2600DUV. The Opti-Probe was the first metrology tool to combine ellipsometry with spectrometry to create the industry's most accurate film thickness measurement system. Combining patented Beam Profile Reflectometry (BPR), patented Beam Profile Ellipsometry (BPE), and spectrophotometry the Opti-Probe 2600 delivers accurate multi-parameter measurements on complex film stacks with 0.1-angstrom precision on ultra-thin films. The Opti-Probe-2600DUV uses a Deuterium light source that increases the system's spectrometric capabilities, and measures reflectivity over the full UV wavelength of 190-450 nanometers (http://www.thermawave.com/). The Thermawave Opti-Probe is shown in **Figure 17.**

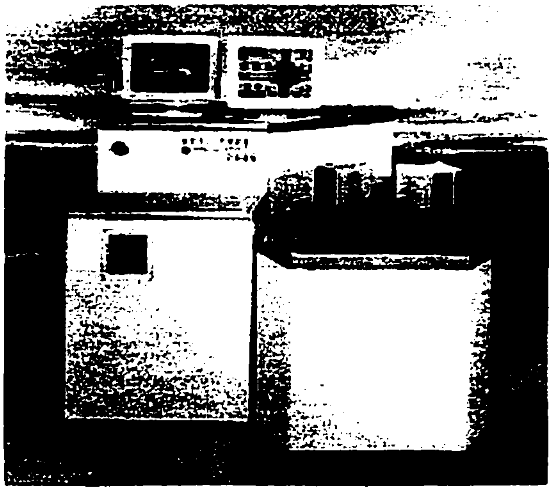


Figure 17: Opti-Probe Source: http://www.thermawave.com/

Opti-Probe Testing Pattern: The wafers were measured at 21 points across the surface as shown in **Figure 18.** This is the standard testing pattern for all the thickness measurements in this work.

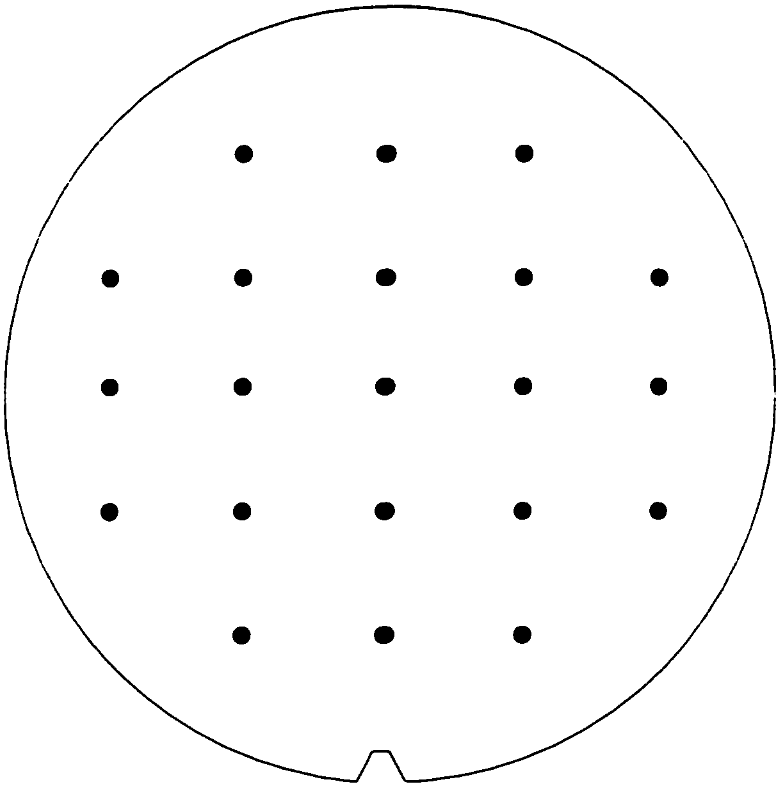


Figure 18: Testing Pattern on the Opti-Probe

STEAG Heatpulse 8800 Rapid Thermal Processor: The Heatpulse 8800 rapid thermal processing system provides a throughput of up to 50 wafers/hr for applications such as oxide densification and reflow, shallow junction activation and silicidation. Designed to meet cleanroom requirements, it features a Class 1 static-free laminar flow environment, a nitrogen curtain to limit oxygen intrusion, a sub-5 second purge time and continuous processing capability. Independent lamp control allows fine-tuning of temperature uniformity, which limits temperature gradients and instantaneous thermal stresses (http://dev.fablink.com/semiconductor/archive/dec97/docs/12best2.html).

Figure 19: STEAG Heatpulse 8800 Rapid Thermal Processor
Source: http://dev.fablink. com/semiconductor/archive/dec97/docs/12best2.html

4.2 Experimental Procedure

Organic contamination on the surface of wafers leads to large standard deviations in thickness and results in errors in measurement. So, experiments were conducted to study the effect of organic contamination on the thickness measurements of ultrathin gate oxides. Screening experiments were performed to determine the recipe parameter ranges for a subsequent DOE and the effect of reoxidation on nitrided gate oxides. The DOE investigated the effect of recipe parameters on the physical characteristics of ultrathin nitrided gate oxides. SIMS was performed on 3 wafers that were oxidized at 850°C. The wafers placed in slots adjacent to the wafers that were analyzed by SIMS were reoxidized. Since the wafers were in adjacent slots during oxidation and anneal steps, they must have nearly the same amount of nitrogen incorporated. The nitrogen concentration obtained from the SIMS data was correlated with the data obtained from reoxidation. In addition, some experiments were conducted to study the effect of NO:N_2 ratio in the anneal step on the amount of nitrogen incorporated in the gate oxide. The overall flow chart of the work done is outlined in **Figure 20.**

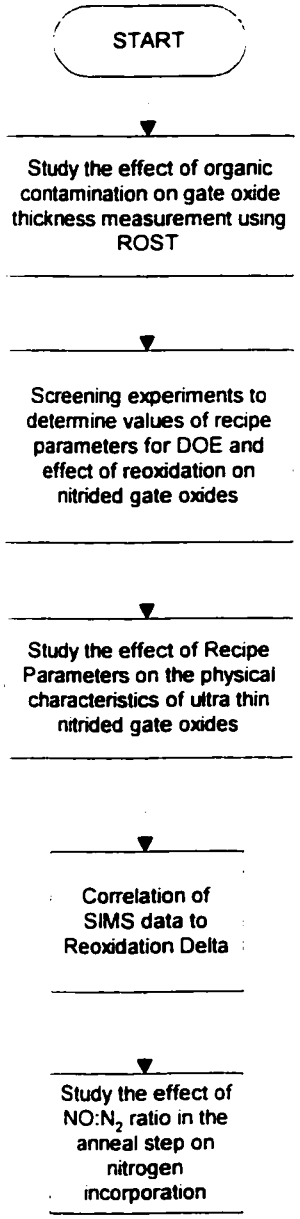

START
Study the effect of organic contamination on gate oxide thickness measurement using ROST
Screening experiments to determine values of recipe parameters for DOE and effect of reoxidation on nitrided gate oxides
Study the effect of Recipe Parameters on the physical characteristics of ultra thin nitrided gate oxides
Correlation of SIMS data to Reoxidation Delta
Study the effect of NO:N2 ratio in the anneal step on nitrogen incorporation

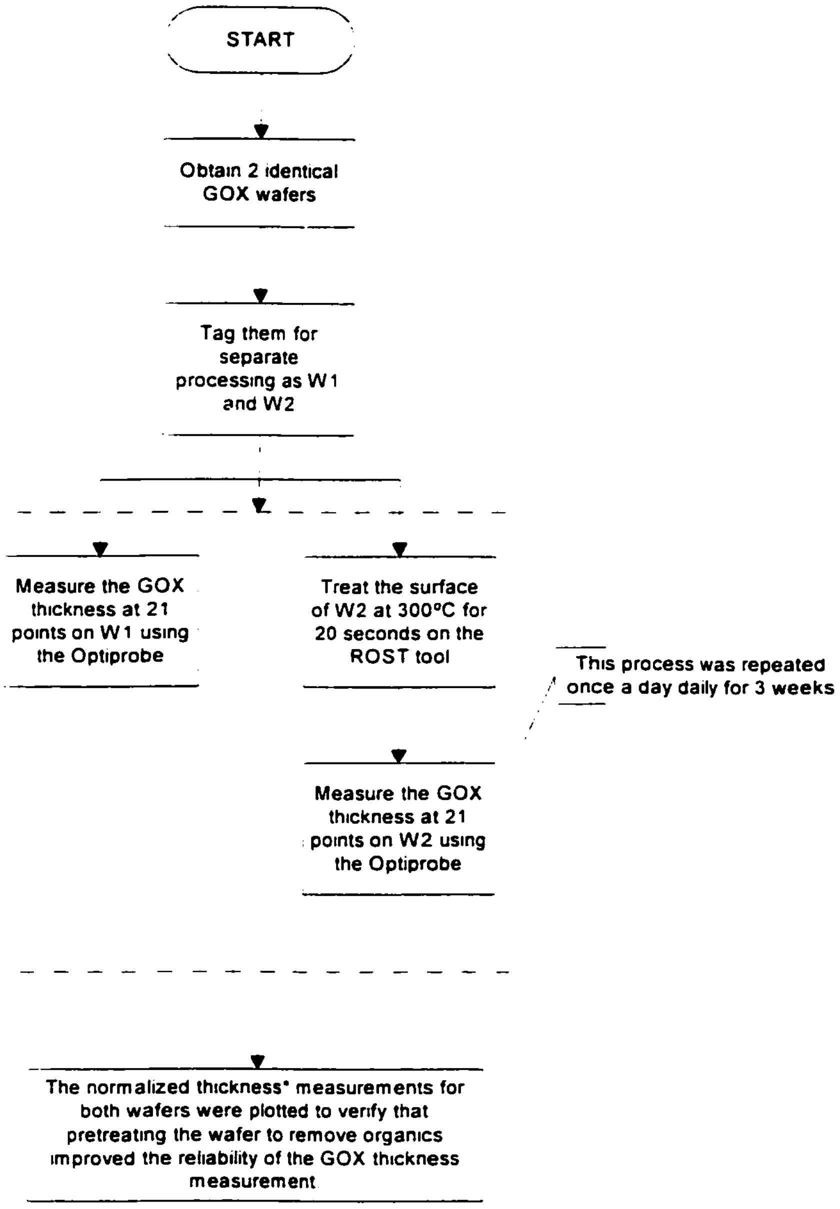
Figure 20: Overview of Experiments

4.3 Reduction of Organic Contamination

Before studying the effect of recipe parameters on the thickness of ultrathin nitrided gate oxides it was necessary to study the impact of organic contamination on thickness measurements. The presence of organic contamination on the wafer surface causes a variation in the thickness of ultrathin oxides and leads to errors in measurement. The presence of organic contamination on the surface becomes unacceptable for such thin films.

It is a well-established fact that heating eliminates organic contamination. Experiments were carried out to study the effect of heating the wafer surface on the removal of organic contamination. This was done using the ROST tool.

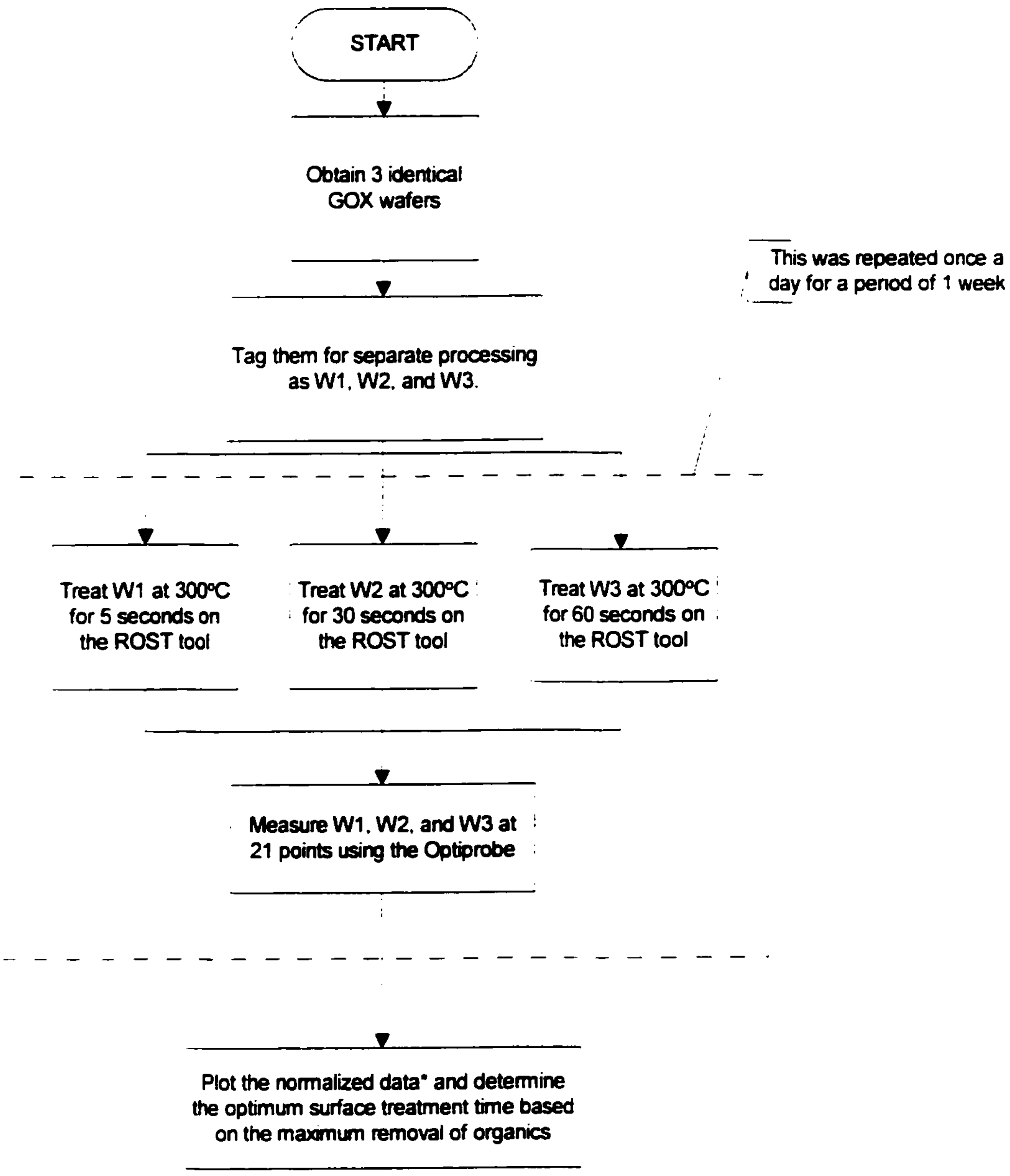
Two sets of experiments were conducted to study the effect of surface treatment on the thickness measurement of ultrathin oxides. In the first set of experiments, a gate oxide wafer was treated on the ROST tool on a daily basis over a period of three weeks. In this experiment the surface of the wafer was treated at 300°C for a period of 20 sec based on the best practicing conditions suggested by QC Solutions, the manufacturer of the ROST tool. The thickness was measured on the Thermawave Opti-Probe before and after treatment. The average thickness was recorded. This was compared with a reference gate oxide wafer that was not subjected to treatment on the ROST tool. Both the wafers were stored in a wafer box after each treatment and measurement. The thickness measured was normalized with respect to the initial oxide thickness. The normalized thickness of the two wafers was compared to verify that pretreatment of the wafers to remove organic contamination improved the reliability of gate oxide thickness measurement. The procedure is outlined in **Figure 21.**


START
Obtain 2 identical GOX wafers
Tag them for separate processing as W1 and W2
Measure the GOX thickness at 21 points on W1 using the Optiprobe
Treat the surface of W2 at 300°C for 20 seconds on the ROST tool
This process was repeated once a day daily for 3 weeks
Measure the GOX thickness at 21 points on W2 using the Optiprobe
The normalized thickness* measurements for both wafers were plotted to verify that pretreating the wafer to remove organics improved the reliability of the GOX thickness measurement

*Normalized with respect to initial oxide thickness

Figure 21: Procedure to characterize the effect of ROST pretreatment

A second experiment was carried out to determine the optimum time for which the wafers should be heated to reduce organic contamination. Three gate oxide wafers were used for this purpose. The wafers were treated once a day on the ROST tool at 300°C for different lengths of time (5 sec. 30 sec. and 60 sec) over a period of one week. The oxide thickness was measured using the Thermawave Opti-Probe. The average thickness was recorded before and after treating the wafers. After treatment on the ROST tool and thickness measurement on the Opti-Probe the wafers were stored in a wafer box. The thickness was normalized with respect to the initial oxide thickness. The optimum time for which the wafers were to be treated would be determined based on the maximum removal of organic contamination from the surface. The procedure is outlined in **Figure 22.**


START
Obtain 3 identical GOX wafers
This was repeated once a day for a period of 1 week
Tag them for separate processing as W1, W2, and W3.
Treat W1 at 300°C for 5 seconds on the ROST tool
Treat W2 at 300°C for 30 seconds on the ROST tool
Treat W3 at 300°C for 60 seconds on the ROST tool
Measure W1, W2, and W3 at 21 points using the Optiprobe
Plot the normalized data* and determine the optimum surface treatment time based on the maximum removal of organics

* Normalized with respect to initial oxide thickness

Figure 22: Procedure for optimizing ROST process time

4.4 Screening Experiments

4.4.1 Growth of Ultrathin Nitrided Gate Oxides

Experiments were conducted to determine the approximate time required to grow nitrided gate oxides in the range of 16-32 Å at 850°C. A temperature of 850°C was selected for the screening experiments since this represented the highest gate oxidation temperature that would be investigated in this research. Based on these results the dry oxidation time was selected for the DOE.

4.4.2 Effect of Reoxidation on Nitrided Gate Oxides

The presence of nitrogen in the gate oxide is known to retard oxidation. An experiment was performed to study how reoxidation affected nitrided gate oxides with respect to non-nitrided ones. Thermal oxides or non-nitrided gate oxides were grown by dry oxidation at 850°C for 30 minutes. The nitrided gate oxides were grown by dry oxidation at 850°C for 30 minutes followed by NO anneal at 900°C for 15 minutes. Both the nitrided and non-nitrided gate oxides were grown in SVG vertical thermal reactors. The thickness of the wafers after oxidation was around 30-32Å. The wafers were reoxidized in a STEAG Rapid Thermal Processor at 1025°C for 2 minutes.

4.5 Effects of Recipe Parameters on 'NO' Nitrided Gate Oxides

An attempt was made to study the effect of recipe parameters such as dry oxidation time. dry oxidation temperature. and anneal temperature on the characteristics of the NO annealed gate dielectrics. Based upon the results of the screening experiments described in Section 4.4. the DOE parameters were set. Experiments were conducted for 3 different oxidation temperatures, oxidation times, and anneal temperatures as shown in **Table 4**. A full factorial experimental DOE was performed. For all the experiments the wafers were cleaned using the standard RCA process in the FSI Mercury® spray processor. All the oxidation and anneal steps were performed in a SVG 7000 series vertical thermal reactor.

Table 4: Variables studied in the DOE

Recipe Parameters			
Dry Oxidation Temp (°C)	800	825	850
Dry Oxidation Time (min)	8	15	30
'NO' Anneal Temp (°C)	800	850	900

It is known that excess nitrogen at the interface could degrade channel mobility. So it is desirable to optimize the anneal temperatures in such a way that it is high enough to relieve the stresses and low enough to prevent degradation of channel mobility. The NO-anneal temperatures selected for the experiments were 800, 850, and 900°C. For all the experiments the anneal time was fixed at 15 minutes. In all the experiments the O_2: N_2 flow rate in the dry oxidation step was 1:10 and the NO: N_2 flow rate ratio in the anneal step was 3:10. The detailed DOE is outlined in **Appendix A.** The recipe names in **Appendix A** are indicated by 3 numbers, which represent the oxidation time, anneal temperature, and 'NO:N_2' ratio in the anneal step.

27 <100> p-type blanket test wafers were used for these experiments. In all the experimental runs the vertical furnace was ramped up to the oxidation temperature. After oxidation, the furnace was ramped to the desired anneal temperature. After the anneal

step, the furnace was ramped down to 650°C and the wafers were allowed to cool to room temperature before unloading into cassettes. After oxidation and annealing in the furnace, the thickness was measured on the Thermawave Opti-Probe. The average thickness was recorded. The wafers were reoxidized in the STEAG rapid thermal processor to determine the amount of nitrogen incorporated as described later. The flow of the experiments for the physical characterization of the ultrathin nitrided gate oxides is shown in **Figure 23.**

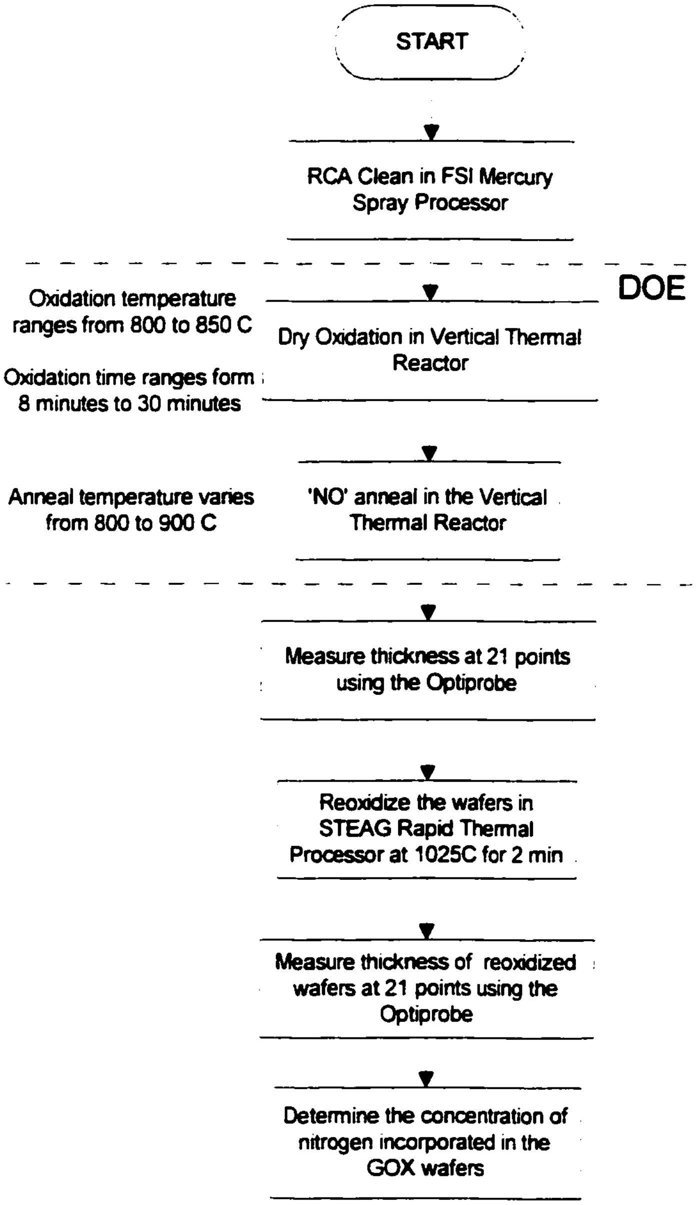

START
RCA Clean in FSI Mercury Spray Processor
DOE
Oxidation temperature ranges from 800 to 850 C
Oxidation time ranges form 8 minutes to 30 minutes
Dry Oxidation in Vertical Thermal Reactor
Anneal temperature varies from 800 to 900 C
'NO' anneal in the Vertical Thermal Reactor
Measure thickness at 21 points using the Optiprobe
Reoxidize the wafers in STEAG Rapid Thermal Processor at 1025C for 2 min
Measure thickness of reoxidized wafers at 21 points using the Optiprobe
Determine the concentration of nitrogen incorporated in the GOX wafers

Figure 23: Flow chart for nitrided gate oxide experiments

4.6 Correlation of Reoxidation Delta of Nitrided Gate Oxides to SIMS

Due to the high costs involved for SIMS, it was not possible to perform analysis on all the wafers. A simple and inexpensive method described in Section 2.2 was used to determine the nitrogen concentration in the gate oxide was used in this work. The wafers were reoxidized and the increase in thickness was related to the wafers that were analyzed by SIMS. For example. in Recipe 15/800/3:10. 2 test wafers were placed in consecutive slots in the top zone of the furnace and both were dry oxidized at 850°C for 15 minutes followed by NO anneal at 800°C. So. both the wafers should have nearly the same amount of nitrogen incorporated. SIMS analysis was performed on one wafer and the other wafer was reoxidized. The increase in thickness after reoxidation. which is hereafter referred to as 'reoxidation delta' in this work. was related to the results obtained from the SIMS analysis.

4.7 Effect of 'NO:N_2' ratio on nitrogen incorporation

In addition to the DOE experiments. two experiments were conducted to study the effects of NO:N_2 ratio in the anneal step on nitrogen incorporation in the ultrathin gate oxides. In the first experiment the wafers were dry oxidized for 30 minutes and annealed in pure 'NO' at 850°C for 15 minutes. In the second experiment the wafers were dry oxidized for 30 minutes and annealed in pure N_2 at 800°C for 15 minutes. All the other parameters were the same as those used in the DOE.

In all the experiments conducted above the thickness was measured on the Thermawave Opti-Probe. The wafers were then reoxidized in the STEAG Rapid Thermal Processor for 2 minutes at 1025°C. After reoxidation the thickness was measured again and the reoxidation delta was determined. From this the amount of nitrogen incorporated was determined.

CHAPTER FIVE
RESULTS AND CONCLUSIONS

Experimental work was carried out to study the effect of organic contamination and recipe parameters on the thickness and properties of ultrathin nitrided gate oxides. The recipe parameters studied in this work include dry oxidation temperature, dry oxidation time, and anneal temperature.

5.1 Reduction of Organic Contamination

A gate oxide wafer was treated on the ROST tool at 300°C for 20 seconds on a daily basis over a period of 3 weeks. The thickness of the wafer was measured on the Thermawave Opti-Probe. This was compared with a reference gate oxide wafer that was not treated on the ROST tool. The normalized thickness of the gate oxide wafer is plotted as a function of time and is shown in **Figure 24.** For normalization, the thickness was divided by the original oxide thickness of each wafer.

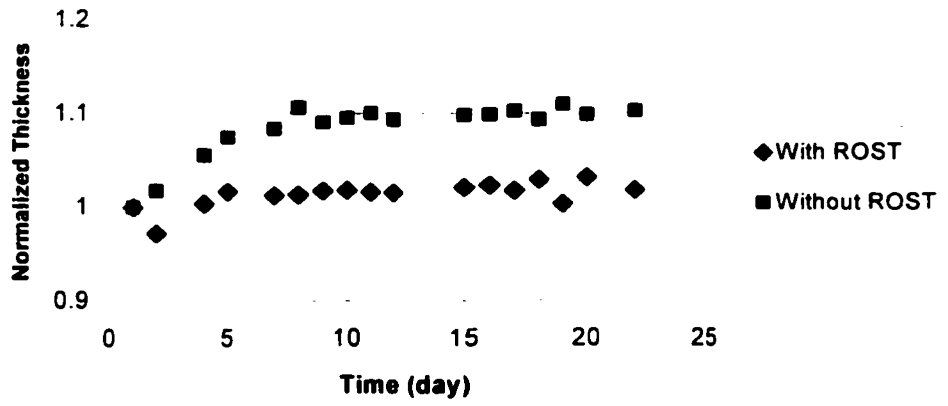


Figure 24: Normalized Thickness data for Gate oxide wafers with and without ROST treatment

From **Figure 24,** it can be seen that without surface treatment the thickness increases by about 10% and saturates. With surface treatment. the thickness initially decreases due to removal of organic contamination from the surface. Then it increases slightly probably due to the surface bonds being affected by the nitrogen ambient in the ROST tool. The thickness remains nearly the same as the original thickness.

The statistical range is the difference between the maximum and minimum thickness of the 21 points measured using the Opti-Probe. The normalized thickness range for the wafers that were surface treated at 300°C for 20 sec and those that were not treated is shown in **Table 5**. We can see that there is a significant difference between the wafer that was treated on the ROST tool and that which was not.

Table 5: Normalized Thickness Range with and without ROST treatment

Type of wafer	Normalized Range (Å)	
	No treatment on ROST tool	With treatment on ROST tool
Gate Oxide	0.109	0.059

Three gate oxide wafers were used to determine the optimum time for which the wafers should be treated on the ROST tool to reduce organic contamination. The wafers were treated on the ROST tool on a daily basis at 300°C for different lengths of time (5 sec. 30 sec. and 60 sec) over a period of one week. The oxide thickness was measured on the Thermawave Opti-Probe. The average thickness was recorded before and after treating the wafers. The thickness data was normalized with the original thickness and plotted as a function of different ROST times as shown in **Figure 25**.

Figure 25 shows that treating the wafer on the ROST tool for 5 seconds seems to be sufficient to remove more organic contamination from the surface than longer treatment periods. It may be that the longer treatment times of 30 sec and 60 sec are also effective in removing organic contamination but treatment of the wafer in a nitrogen ambient in the ROST tool affects the Si surface bonds leading to large standard deviations and increased thickness measurements.

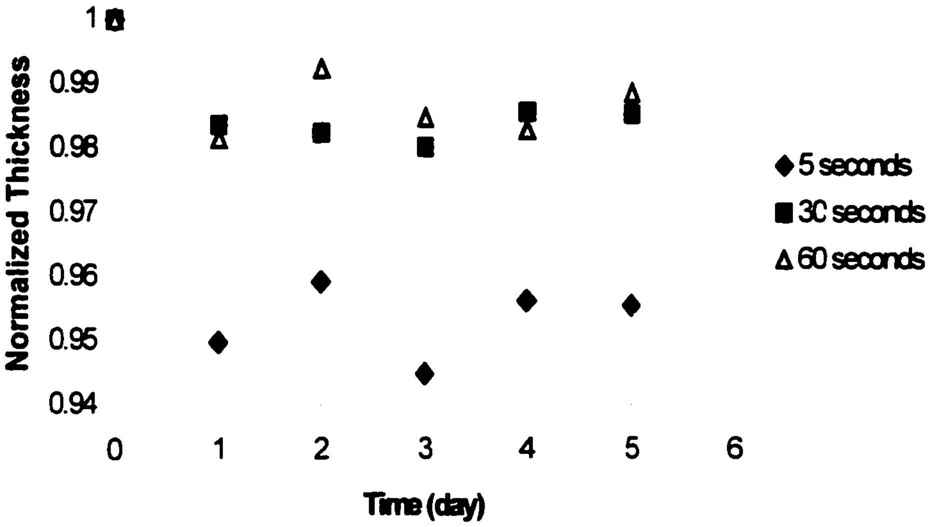


Figure 25: Normalized Thickness data as a function of different ROST times

From these experiments it is seen that by treating ultrathin oxide wafers on the ROST tool for 5 seconds, it is possible to reduce organic contamination and obtain a better estimate of the thickness of thin oxides.

It can be concluded that the presence of organic contamination on the surface of the wafers leads to errors in measurement. In the case of ultrathin oxides where the thickness is really small. this is not acceptable. This error in measurement can be minimized by treating the wafer surface for 5 seconds at 300°C on the ROST tool.

5.2 Results of Screening Experiments

Growth Rate Experiments

Results of the growth rate experiments conducted for nitrided gate oxides at 850°C are shown in **Figure 26.** For the experiments under consideration oxide growth is in the linear range. The error bars represent 3 sigma values of standard deviation.

Based on the thermal oxide growth rate experiments explained in Section 4.4. dry oxidation times of 8. 15. and 30 minutes were selected for the DOE.

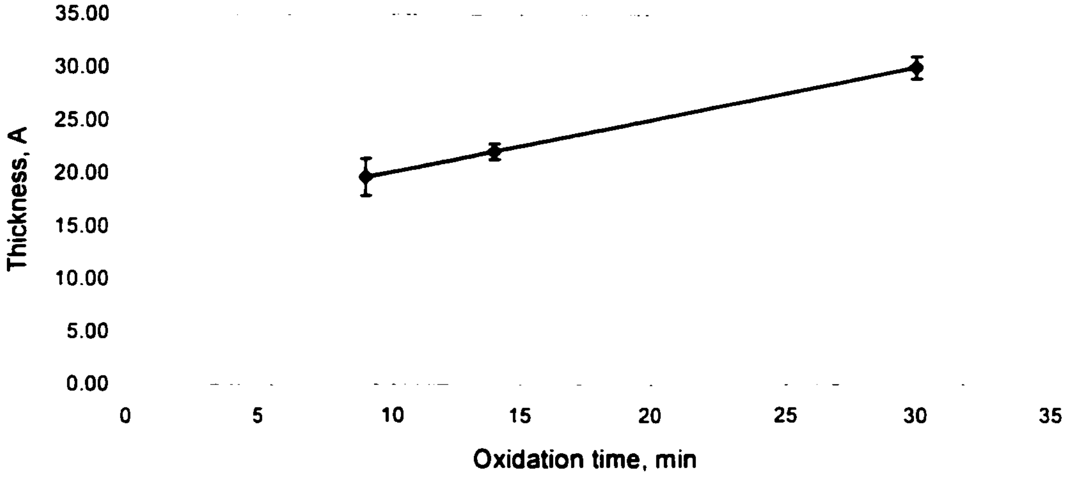


Figure 26: Growth rate of nitrided oxides at 850°C

Effect of Reoxidation on Nitrided Gate Oxides

The results of the effect of reoxidation on nitrided and non-nitrided gate oxides are shown in **Figure 27.**

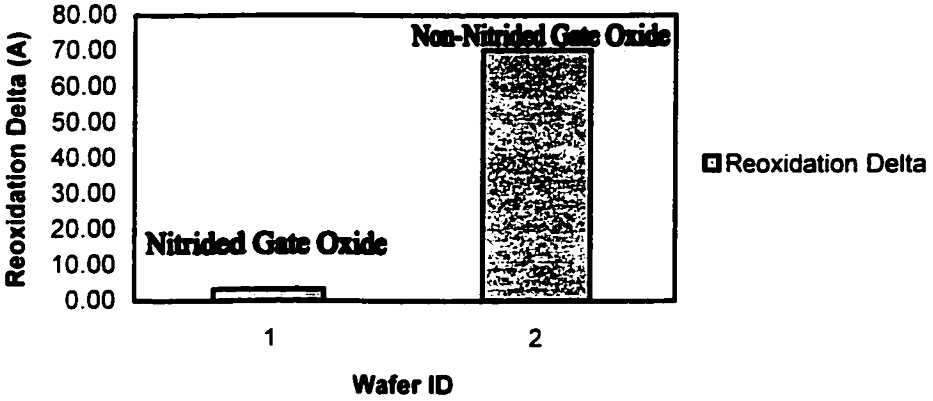


Figure 27: Effect of Reoxidation on nitrided and non-nitrided gate oxides

It can be seen that the presence of nitrogen in the gate oxide slows down further oxidation. There is about 2-3Å increase in oxide thickness after reoxidation for the nitrided gate oxide wafers in the above experiment compared to ~70Å increase in the case of non-nitrided gate oxides.

5.3 Effects of Recipe Parameters on 'NO' Nitrided Gate Oxides

After oxidation and annealing in the furnace, the thickness was measured on the Thermawave Opti-Probe. The average thickness and standard deviation of the nitrided gate oxide wafers were recorded and are reported in **Appendix B.**

From the plots in **Figure 28**, **Figure 29** and **Figure 30**, it can be seen that for a given anneal temperature, the thickness of the nitrided gate oxides in the range under consideration increases linearly with dry oxidation temperature.

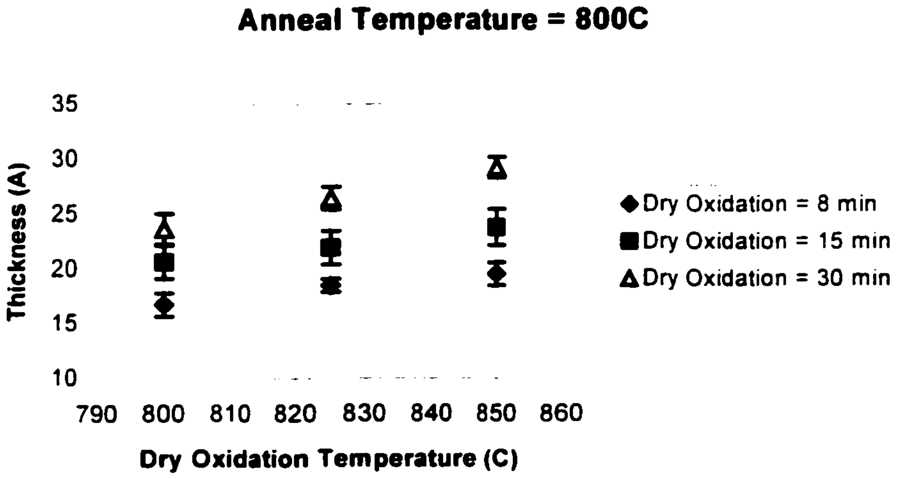


Figure 28: Oxide Thickness as a function of Oxidation Temperature

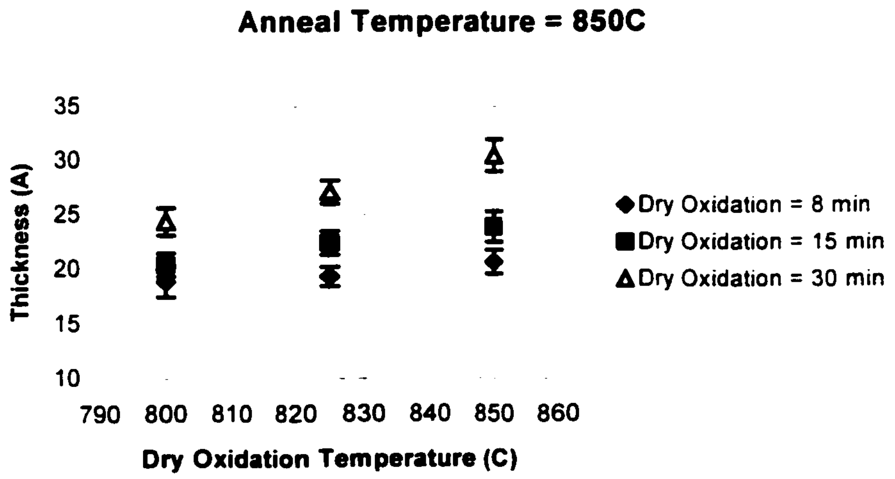


Figure 29: Oxide Thickness as a function of Oxidation Temperature

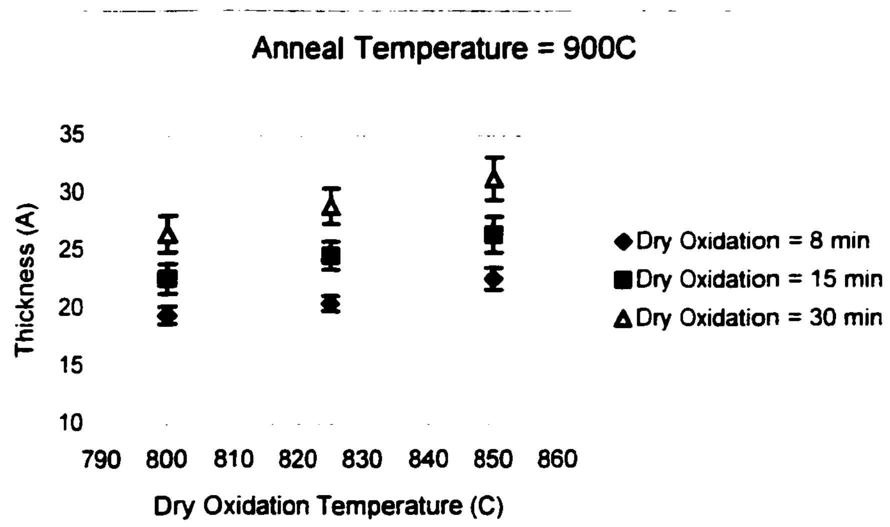


Figure 30: Oxide Thickness as a function of Oxidation Temperature

5.4 Reoxidation of Nitrided Gate Oxides

The wafers from the runs described in the DOE were reoxidized in a STEAG Rapid Thermal Processor for 2 minutes at 1025°C. The thickness was measured on the Thermawave Opti-Probe after reoxidation. The thickness after reoxidation and the reoxidation delta is reported in **Appendix C.**

It has been shown earlier that the presence of nitrogen in the gate oxide slows down further oxidation. So the reoxidation delta is a function of the amount of nitrogen incorporated. Of all the recipe parameters studied, the parameter which has the biggest affect on nitrogen incorporation in the ultrathin gate oxide is the anneal temperature. As the anneal temperature is increased, more nitrogen is incorporated and a smaller change in oxide thickness is observed after reoxidation. The effect of anneal temperature on the reoxidation delta as a function of initial oxide thickness can be seen from the plots in

Figure 31, Figure 32, and **Figure 33.** It is seen that the reoxidation delta is a function of the anneal temperature independent of the starting oxide thickness.

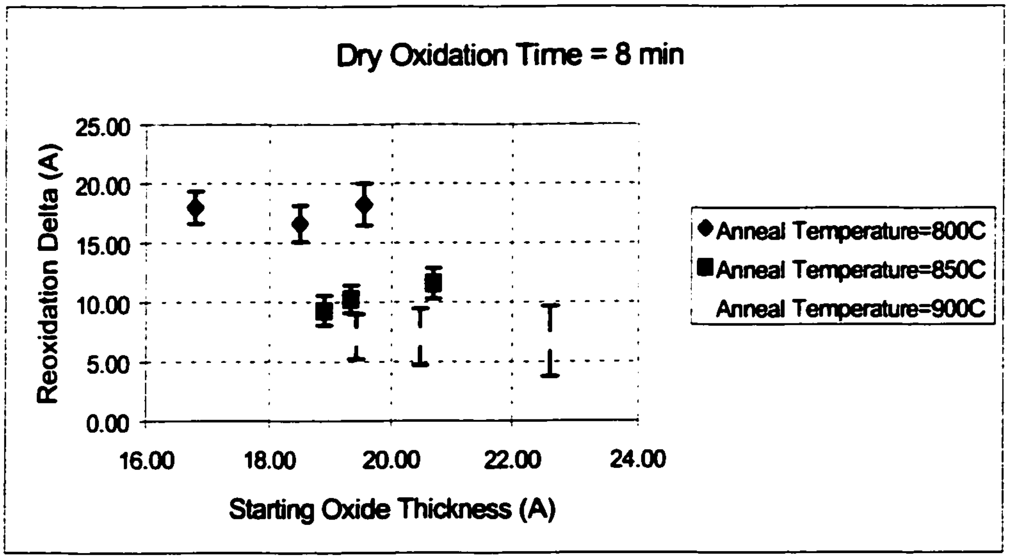


Figure 31: Reoxidation Delta as a function of Starting Oxide Thickness

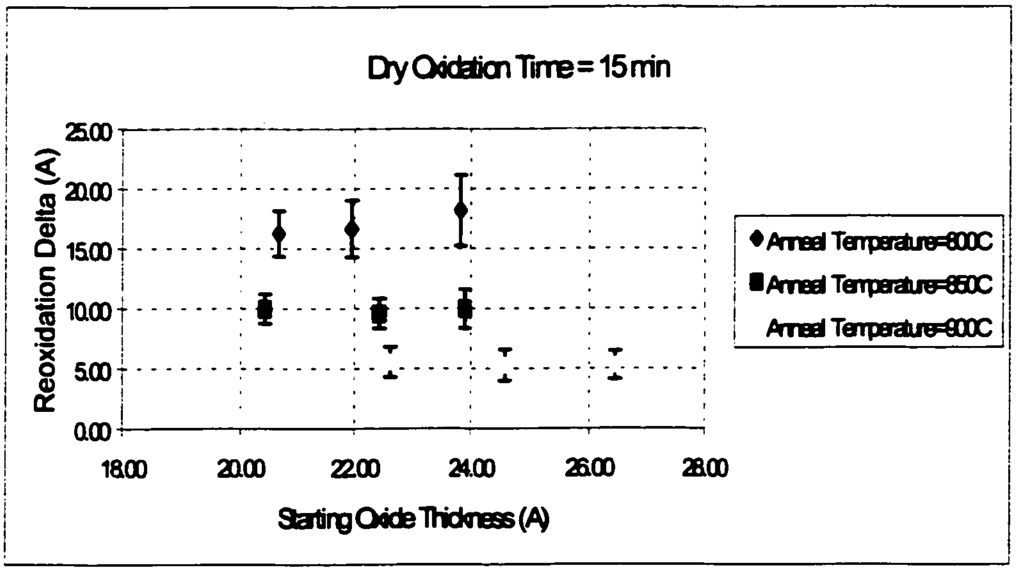


Figure 32: Reoxidation Delta as a function of Starting Oxide Thickness

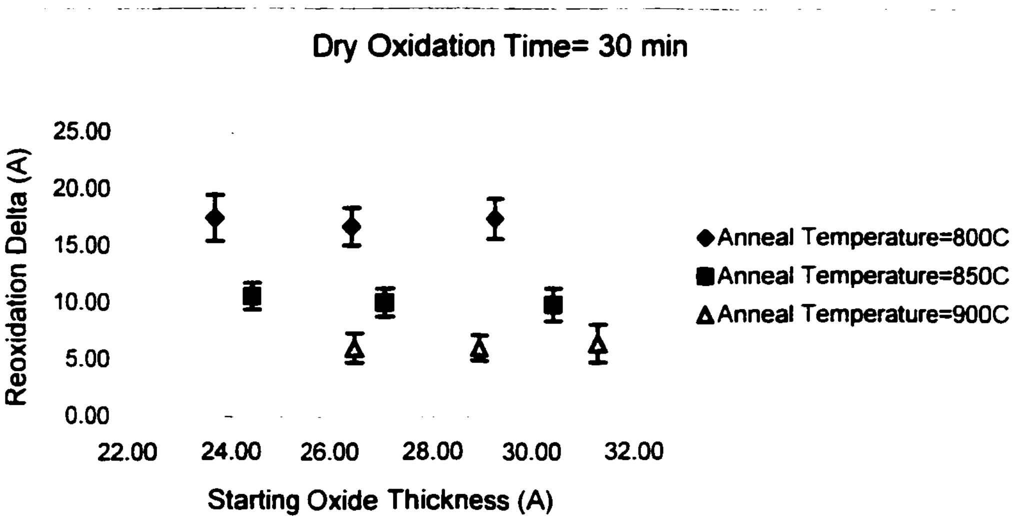


Figure 33: Reoxidation Delta as a function of Starting Oxide Thickness

5.5 Correlation of SIMS data with Reoxidation Delta

SIMS analysis was performed on wafers that were oxidized at 850°C and annealed at different temperatures (800. 850, and 900°C). These samples had different nitrogen profiles due to different anneal times. The test wafers placed adjacent to the SIMS test wafers in the furnace were reoxidized. The thickness of the reoxidized wafers was measured on the Thermawave Opti-Probe. The reoxidation delta values were recorded.

The surface concentration of nitrogen obtained from SIMS analysis is given in **Table 6.**

Table 6: Surface concentration of nitrogen from SIMS analysis

Dry Oxidation Temperature(°C)	Anneal Temperature (°C)	Nitrogen Concentration (atoms/cm^2)
850	800	9.62E+14
850	850	1.43E+15
850	900	1.70E+15

For a given dry oxidation temperature, the reoxidation delta was found to vary linearly with the amount of nitrogen incorporated as shown in **Figure 34.**

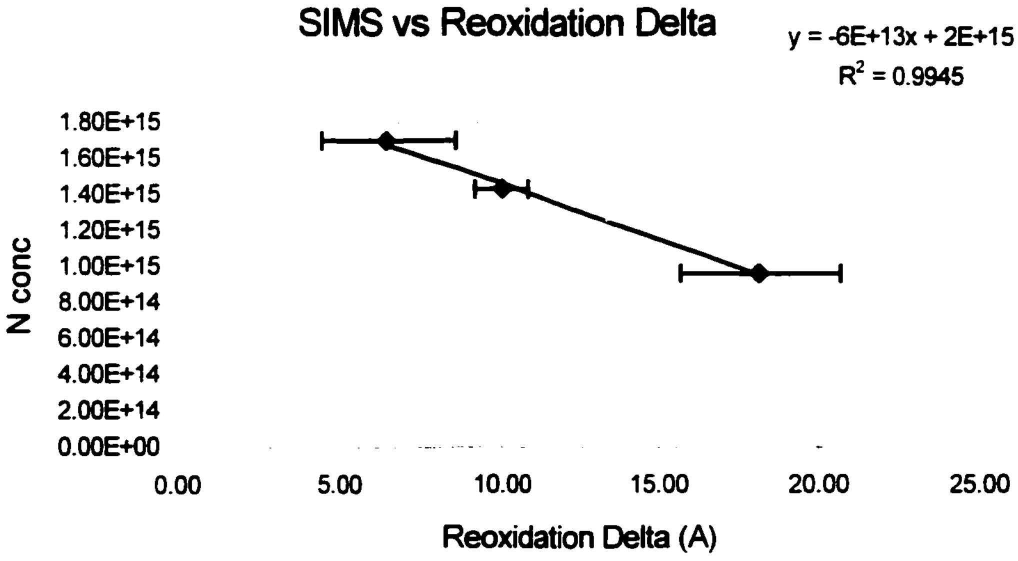


Figure 34: SIMS vs Reoxidation delta for wafers oxidized at 850°C

The amount of nitrogen incorporated in the wafers oxidized at 850°C can be determined from the SIMS vs. reoxidation delta plot. The nitrogen concentration of all the wafers that were oxidized at 850°C was calculated using the relation from the SIMS vs. reoxidation delta plot.

N concentration = -6 * EXP (13*Reox Delta) + 2 * EXP (15).

The results are shown in **Table 7.**

Table 7: Comparison of SIMS data and theoretically calculated data for N concentration

Oxidation Temp	Oxidation	Anneal Temp	REOX DELTA	N conc. From SIMS (atom/cm^2)	Theoretical N conc. from SIMS vs. Reoxidation Delta (Atom/cm^2)	%Difference
850	8	800	18.24		9.06E+14	
850	8	850	11.60		1.30E+15	
850	8	900	6.73		1.60E+15	
850	15	800	18.17	9.62E+14	9.10E+14	5.43
850	15	850	9.98	1.43E+15	1.40E+15	2.01
850	15	900	5.30		1.68E+15	
850	30	800	17.48		9.51E+14	
850	30	850	9.92		1.40E+15	
850	30	900	6.48	1.70E+15	1.61E+15	5.22

The difference between the actual data from SIMS and the theoretically calculated data from the SIMS-Reoxidation delta plot is around 5%, which is within experimental error limits.

5.6 Effect of "NO: N_2" ratio in Anneal step on Nitrogen Incorporation

The effect of NO: N_2 ratio in the anneal step on the amount of nitrogen incorporated in the nitrided gate oxide was studied. In one set of experiments, the wafers were oxidized for 30 min and annealed in concentrated NO (NO: N_2 = 3:0) for 15 min. These results were compared with wafers that were oxidized at 850°C for 30 min and annealed in 3:10 NO: N_2 for 15 minutes and are reported in Appendix D.

From this comparison it is seen that concentrated or pure NO incorporates more nitrogen than diluted NO under similar processing conditions. This can be concluded from the lower reoxidation delta values in the case of annealing in concentrated NO. A plot of this comparison is shown in **Figure 35.**

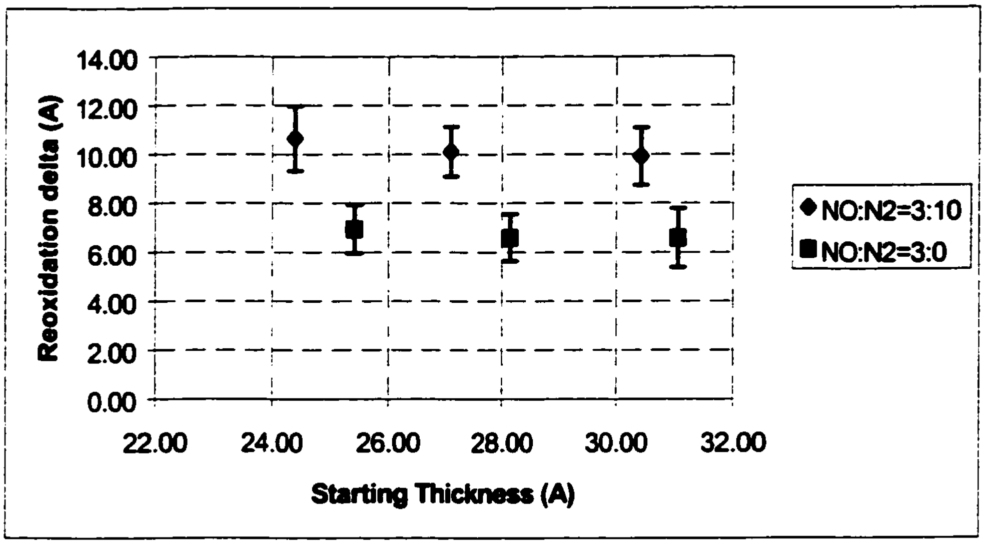


Figure 35: Effect of NO concentration on Reoxidation delta

In another set of experiments the effect of N_2 in the anneal step was studied. In this run the wafers were oxidized at 850°C for 30 minutes and annealed in pure N_2 gas for 15 minutes at 800°C. This shows us the extent to which N_2 gas incorporates nitrogen in the thin oxide film. The results are compared with wafers that were oxidized at 850°C for 30 minutes and annealed in 3:10 NO: N_2 at 800°C and are tabulated in **Appendix E.**

From this comparison it is seen that N_2 gas is hardly involved in nitrogen incorporation at the interface of the ultrathin oxide film. This can be concluded from the large increase in reoxidation delta, which implies that hardly any nitrogen has been incorporated. This is illustrated in **Figure 36.**

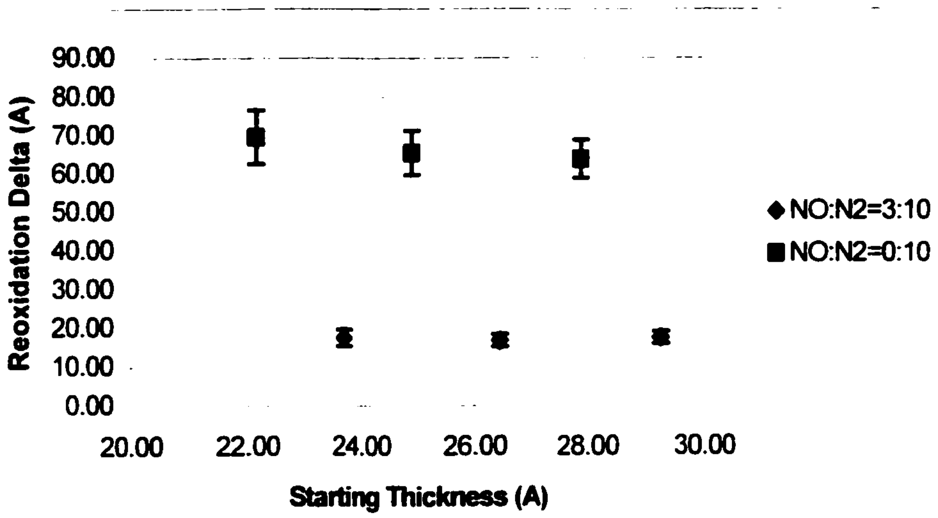


Figure 36: Effect of N_2 anneal on reoxidation delta

CHAPTER SIX
SUMMARY AND FUTURE WORK

6.1 Summary

In this work. the growth. measurement and physical characterization of ultrathin nitrided gate oxides in the thickness range 16-32Å were studied.

The thickness measurement of ultrathin gate oxides can be affected by the presence of organic contaminants. It is seen that the thickness of ultrathin films can increase by up to 10% due to organic contamination and then it saturates. The organic contamination on the surface degrades the standard deviation of the within wafer thickness measurement. This can be reduced to a great extent by treating the wafer surface on the ROST tool for 5 seconds at 300^{0}C.

Nitrided gate oxides have the potential to be the gate dielectric of the future. From all the experiments conducted on nitrided gate oxides it can be concluded that the amount of nitrogen incorporated at the interface is a function of the anneal temperature. As the anneal temperature increases. the amount of nitrogen incorporated increases and is independent of the starting oxide thickness. The amount of nitrogen incorporated also depends on the NO: N_2 ratio in the anneal step. Pure NO incorporates more nitrogen at the interface than NO diluted with N_2.

An alternative method to determine nitrogen concentration in ultrathin gate oxides is by correlating the nitrogen concentration obtained from SIMS analysis with the reoxidation delta. For a given oxidation temperature, the increase in thickness after reoxidation varies linearly with nitrogen concentration. This method has been used to determine the amount of nitrogen present in the gate dielectric.

6.2 Future Work

In this work the growth, measurement, and physical characteristics of ultrathin nitrided gate oxides have been studied. For future work, electrical characteristics of nitrided gate oxides such as leakage, Q_{BD}, Breakdown voltage etc can be studied. The effect of nitrogen in ultrathin gate oxides on Boron blocking, mobility degradation etc. can also be investigated. The effect of Nitrogen position in the gate oxide on reoxidation delta is another area that can be investigated.

APPENDIX A: DETAILED DOE

Recipe	Oxidation Temperature (^{o}C)	Oxidation Time (min)	Anneal Temperature (^{o}C)
8/800/3:10	800	8	800
8/800/3:10	825	8	800
8/800/3:10	850	8	800
8/850/3:10	800	8	850
8/850/3:10	825	8	850
8/850/3:10	850	8	850
8/900/3:10	800	8	900
8/900/3:10	825	8	900
8/900/3:10	850	8	900
15/800/3:10	800	15	800
15/800/3:10	825	15	800
15/800/3:10	850	15	800
15/850/3:10	800	15	850
15/850/3:10	825	15	850
15/850/3:10	850	15	850
15/900/3:10	800	15	900
15/900/3:10	825	15	900
15/900/3:10	850	15	900
30/800/3:10	800	30	800
30/800/3:10	825	30	800
30/800/3:10	850	30	800
30/850/3:10	800	30	850
30/850/3:10	825	30	850
30/850/3:10	850	30	850
30/900/3:10	800	30	900
30/900/3:10	825	30	900
30/900/3:10	850	30	900

APPENDIX B: RESULTS OF DOE

Recipe	Oxidation Temperature (°C)	Oxidation Time (min)	Anneal Temperature (°C)	NGOX Thickness (Å)	NGOX Sigma (Å)
8/800/3:10	800	8	800	16.78	0.36
8/800/3:10	825	8	800	18.52	0.20
8/800/3:10	850	8	800	19.56	0.35
8/850/3:10	800	8	850	18.92	0.47
8/850/3:10	825	8	850	19.35	0.29
8/850/3:10	850	8	850	20.67	0.36
8/900/3:10	800	8	900	19.44	0.25
8/900/3:10	825	8	900	20.46	0.22
8/900/3:10	850	8	900	22.59	0.31
15/800/3:10	800	15	800	20.68	0.50
15/800/3:10	825	15	800	21.95	0.51
15/800/3:10	850	15	800	23.81	0.55
15/850/3:10	800	15	850	20.43	0.35
15/850/3:10	825	15	850	22.42	0.35
15/850/3:10	850	15	850	23.89	0.47
15/900/3:10	800	15	900	22.60	0.43
15/900/3:10	825	15	900	24.60	0.41
15/900/3:10	850	15	900	26.43	0.52
30/800/3:10	800	30	800	23.67	0.46
30/800/3:10	825	30	800	26.43	0.34
30/800/3:10	850	30	800	29.25	0.31
30/850/3:10	800	30	850	24.40	0.42
30/850/3:10	825	30	850	27.08	0.36
30/850/3:10	850	30	850	30.42	0.49
30/900/3:10	800	30	900	26.49	0.53
30/900/3:10	825	30	900	28.93	0.51
30/900/3:10	850	30	900	31.29	0.61

APPENDIX C: REOXIDATION RESULTS

Recipe	Oxidation Temperature (^oC)	Oxidation Time (min)	Anneal Temperature (^oC)	NGOX Thickness (Å)	Thickness after Reoxidation (Å)	Reoxidation Delta (Å)
8/800/3:10	800	8	800	16.78	34.78	17.99
8/800/3:10	825	8	800	18.52	35.19	16.63
8/800/3:10	850	8	800	19.56	37.80	18.24
8/850/3:10	800	8	850	18.92	28.24	9.32
8/850/3:10	825	8	850	19.35	29.20	10.28
8/850/3:10	850	8	850	20.67	30.95	11.60
8/900/3:10	800	8	900	19.44	26.55	7.11
8/900/3:10	825	8	900	20.46	27.56	7.10
8/900/3:10	850	8	900	22.59	29.32	6.73
15/800/3:10	800	15	800	20.68	36.93	16.26
15/800/3:10	825	15	800	21.95	38.61	16.66
15/800/3:10	850	15	800	23.81	41.97	18.17
15/850/3:10	800	15	850	20.43	30.41	9.98
15/850/3:10	825	15	850	22.42	32.00	9.58
15/850/3:10	850	15	850	23.89	33.87	9.98
15/900/3:10	800	15	900	22.60	28.17	5.57
15/900/3:10	825	15	900	24.60	29.89	5.28
15/900/3:10	850	15	900	26.43	31.72	5.30
30/800/3:10	800	30	800	23.67	41.17	17.51
30/800/3:10	825	30	800	26.43	43.23	16.80
30/800/3:10	850	30	800	29.25	46.72	17.48
30/850/3:10	800	30	850	24.40	35.05	10.65
30/850/3:10	825	30	850	27.08	37.20	10.12
30/850/3:10	850	30	850	30.42	40.34	9.92
30/900/3:10	800	30	900	26.49	32.61	6.12
30/900/3:10	825	30	900	28.93	35.05	6.12
30/900/3:10	850	30	900	31.29	37.77	6.48

APPENDIX D RESULTS OF THE EFFECT OF 'NO' ANNEAL

Recipe	Oxidation Temperature (°C)	Oxidation Time (min)	Anneal Temperature (°C)	NGOX Thickness (Å)	Thickness after Reoxidation (Å)	Reoxidation Delta (Å)
30/850/3:10	800	30	850	24.40	35.05	10.65
30/850/3:10	825	30	850	27.08	37.20	10.12
30/850/3:10	850	30	850	30.42	40.34	9.92
30/850/3:0	800	30	850	25.42	32.26	6.94
30/850/3:0	825	30	850	28.14	34.73	6.59
30/850/3:0	850	30	850	31.07	37.66	6.59

APPENDIX E RESULTS OF THE EFFECT OF 'N_2' ANNEAL

Recipe	Oxidation Temperature (°C)	Oxidation Time (min)	Anneal Temperature (°C)	NGOX Thickness (Å)	Thickness after Reoxidation (Å)	Reoxidation Delta (Å)
30/800/3:10	800	30	800	23.67	41.17	17.51
30/800/3:10	825	30	800	26.43	43.23	16.80
30/800/3:10	850	30	800	29.25	46.72	17.48
30/800/0:10	800	30	800	22.12	91.69	69.57
30/800/0:10	825	30	800	24.90	90.43	65.54
30/800/0:10	850	30	800	27.88	91.63	63.80

REFERENCES

1. S.M. Sze. "*VLSI Technology.*" 2nd Edition. McGraw Hill Publication (1988).

2. B.G. Streetman. "*Solid State Electronic Devices.*" Fifth Edition. Prentice Hall Publication (2001).

3. L. Manchanda. *MIT Microsystems Technology Lab VLSI Seminar Series.* April 27 (1999).

4. D.A. Buchanan. "*Scaling the gate dielectric: Materials. integration. and reliability.*" IBM Journal of Research and Development. **43**(3). pp. 245 (1999).

5. S. Wolf and R.N. Tauber. "*Silicon Processing for the VLSI Era.*" 2nd Edition. Lattice Press (2000).

6. *National Technology Roadmap for Semiconductors.* 3rd edition. Semiconductor Industry Association. San Jose. CA (1997).

7. G.D. Leonarduzzi. "*Improving Performance with Oxynitride Gate Dielectrics.*" Semiconductor International. July (1998).

8. Z.Q. Yao. "*The Nature and Distribution of Nitrogen in Silicon Oxynitride Grown on Silicon in a Nitric Oxide Ambient.*" Journal of Applied Physics. **78(5)**. pp. 2906 (1995).

9. S.S. Dang and C.G. Takoudis. "*Rate-limiting steps during nitrogen incorporation in furnace-grown silicon oxynitrides: effects on wafer-to-wafer uniformity.*" Thin Solid Films. **366** (1/2). pp. 225 (2000).

10. E.P. Gusev. H.C. Lu. E.L. Garfunkel. T. Gustafsson and M.L. Green. "*Growth and characterization of ultrathin nitrided silicon oxide films.*" IBM Journal of Research and Development. **43**(3). pp.265 (1999).

11. G. Lucovsky. A. Banerjee. B. Hinds. B. Claflin. K. Koh and H. Yang. "*Minimization of Sub-Oxide Transition Regions at Si-SiO2 Interfaces by 900°C Rapid Thermal Annealing.*" Microelectronic Engineering. **36(1/4)**. pp. 207 (1997).

12. Z. Liu. H. Wann. P.K. Ko. C. Hu and Y.C. Cheng. "*Improvement of charge trapping characteristics of N_2O-annealed and reoxidized N_2O-annealed thin oxides.*" IEEE Electron Device Letters. **13(10)**. pp. 519 (1992).

13. Y. Okada. P.J. Tobin. and S.A. Ajuria. "*Furnace Grown Silicon Oxynitrides Using Nitric Oxide (NO).*" IEEE Transactions on Electron Devices. **41(9)**. pp. 1608 (1994).

14. I.J.R. Baumvol. J.J. Ganem and S. Rigo. "*Incorporation of oxygen and nitrogen in ultrathin films of SiO_2 annealed in NO.*" Applied Physics Letters. 72(23). pp. 2999 (1998).

15. M. Bhat. L.K Han. D. Wristers. J. Yan. D.L. Kwong and J. Fulford. "*Effects of chemical composition on the electrical properties of NO-nitrided SiO_2.*" Applied Physics Letters. **66**(10). pp. 1225 (1995).

16. R.I. Hegde. P.J. Tobin. K.G. Reid. B. Maiti and S.A. Ajuria. "*Growth and surface chemistry of oxynitride gate dielectric using nitric oxide.*" Applied Physics Letters. **66**(21). pp. 2882 (1995).

17. E.P. Gusev. H.C. Lu. T. Gustafsson. E. Garfunkel. M.L. Green and D. Brasen. "*The composition of ultrathin silicon oxynitrides thermally grown in nitric oxide.*" Journal of Applied Physics. **82**(2). pp. 896 (1997).

18. H.C. Lu. E.P. Gusev. T. Gustafsson. E. Garfunkel. M.L. Green. D. Brasen and L.C. Feldman. "*High Resolution Ion Scattering Study of Silicon Oxynitridation.*" Applied Physics Letters. **69(18)**. pp. 2713 (1996).

19. C. Gerardi. M. Melanotte. S. Lombardo. M.Alessandri. B. Crivelli and R. Zonca. "*Effects of nitridation by nitric oxide on the leakage current of thin SiO_2 gate oxides.*" Journal of Applied Physics, **87**(1), pp.498 (2000).

20. M.A. Schmidt. F.L. Terry Jr.. B.P. Mathur and S.D. Senturia. "*Inversion layer mobility of MOSFETs with nitrided oxide gate dielectrics.*" IEEE Transactions on Electron Devices. **35(10)**. pp. 1627 (1988).

21. T. Hori. "*Inversion Layer Mobility under High Normal Field in Nitrided-Oxide MOSFET's.*" IEEE Transactions on Electron Devices. **37(9)**. pp. 2058 (1990).

22. Y. Miura. H. Ono and K. Ando. "*Reoxidation effects on the chemical bonding states of nitrogen accumulated at the oxynitride/silicon interface.*" Applied Physics Letters. **77**(2). pp. 220 (2000).

23. S. Narayanan and K. Ramkumar. "*A Novel Self-Monitoring Process for Ultrathin Gate Oxidation.*" US Patent Docket No 8229-013-27 (Filed 2001).

24. R.M. Patrikar. R. Lal and J. Vasi. "*Net Positive-Charge Buildup in Various MOS Insulators Due to High-field Stressing.*" IEEE Electron Device Letters. **14(11)**. pp. 530 (1993).

25. C. Gerardi. R. Zonca, B. Crivelli and M. Alessandri. "*Nitridation of Thin Gate or Tunnel Oxides by Nitric Oxide.*" Journal of the Electrochemical Society. **146**(8). pp. 3058 (1999).

26. S. Wolf. "*Silicon Processing for the VLSI Era.*" Vol. 3. Lattice Press (1995).

27. W. Kern. "*Handbook of Semiconductor Wafer Cleaning Technology.*" Noyes Publications. Park Ridge NJ. (1993).

28. F. Li. K. Marjorie and B.E. Deal. "*Wafers/Substrates: Thickness measurement of submonolayer native oxide films on silicon wafers.*" Solid State Technology. **43**(2) (2000).

29. J. Guan. G. Gale. G. Bersuker. Y. Jeon. B. Nguyen. J. Barnett. M. Jackson. D. Burkman. P. Peavy. K. Yokomizo. K. Ueno. M. Yamasaka. M. Imai. S. Kitahara and N.Shindo, "*Properties of chemical oxides from pre-gate clean processes and their role in the electrical thickness of thermally grown ultrathin gate oxides*". Electrochemical Society Proceedings. **99-36**.

30. W. Scholl and J. Domaschke. "*Implementation of Modeling and Simulation in Semiconductor Wafer Fabrication with Time Constraints between Wet Etch and Furnace Operations.*" IEEE Transactions on Semiconductor Manufacturing, **13**(3), pp. 273 (2000).

31. T. Ohmi, "*Very high quality thin gate oxide formation technology,*" Journal of Vacuum Science and Technology A. **13(3)**. pp. 1665 (1995).

32. S. De Gendt. D. Martin Knotter. K. Kenis. M. Depas. M. Meuris. P.W. Mertens and M.M. Heyns. "*Impact of Organic Contamination on Thin Gate Oxide Quality.*" Japanese Journal of Applied Physics Part I. **37(9A)**. pp. 4649 (1998).

33. D. Wristers. L.K. Han. T. Chen, H.H. Wang, D.L. Kwong. M. Allen and J. Fulford. "*Degradation of oxynitride gate dielectric reliability due to Boron diffusion.*" Applied Physics Letters. **68**(15), pp. 2094 (1996).

34. R.I. Hegde. M.A. Chonko and P.J. Tobin. "*Effect of silicon substrate microroughness on gate oxide quality.*" Journal of Vacuum Science and Technology B. **14**(5). pp. 3299 (1996).

35. http://www.qcsolutions.com

36. http://www.fsi-intl.com

37. http://www.thermawave.com

38. http://dev.fablink.com/semiconductor/archive/dec97/docs/12best2.html