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DESIGN AND ANALYSIS OF ULTRA WIDE BAND CMOS LNA

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Janmejay Adhyaru

December 2007

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ABSTRACT

DESIGN AND ANALYSIS OF ULTRA WIDE BAND CMOS LNA

by Janmejay Adhyaru

An Ultra WideBand CMOS Low Noise Amplifier (LNA) is presented. Due to really low power consumption and extremely high data rates the UWB standard is bound to be popular in the consumer market. The LNA is the outer most part of an UWB transceiver. The LNA is responsible for providing enough gain to the signal with the least distortion possible.

CMOS 0.18μ TSMC technology has been chosen for the design of the LNA at the transistor level. As many as five on chip inductors are implemented for the proper gain shaping over the frequency range of 3.1GHz to 10.6GHz. A noise figure of 4 dB is achieved to make sure noise contribution of the amplifier is as low as possible.

Agilent's ADS tool has been used to simulate and layout the on chip inductors, and Cadence's Spectre simulator has been used to simulate the behavior of active and passive components.

ACKNOWLEDGEMENTS

I would like to thank my MSEE thesis advisor Dr. Sotoudeh Hamedi-Hagh for his continuous support and encouragement. He worked on strengthening my RF circuit background and provided a lot of support and guidance to the problems that I faced while designing this complicated circuit.

I also appreciate the Electrical Engineering Chairperson and my co-advisor Dr. Avtar Singh and co-advisor Dr. Masoud Mostafavi, for their continuous support. I am grateful to the Department of Electrical Engineering for providing me with all the software tools I need to simulate my design.

Lastly I would like to thank my parents, my friends, and all the people who directly or indirectly helped me in my thesis.

TABLE OF CONTENTS

Chapter 1 Introduction to UWB.....1
1.1 UWB vs. various wireless standards.....1
1.2 UWB applications.....3
1.3 UWB operation.....4
1.4 UWB transceiver.....5
1.5 Choice of technology.....8
1.6 Objective.....9

Chapter 2 Low Noise Amplifier Characterization..... 10
2.1 S-parameters.....10
2.2 Amplifier's gain and stability..... 12
2.3 Noise performance..... 14
2.4 The LNA gain, noise factor, and system sensitivity..... 17
2.5 Large signal behavior.....19

Chapter 3 LNA Design..... 25
3.1 Popular LNA topologies in CMOS technology.....25
3.2 Proposed LNA design..... 31
3.3 Simulations and results..... 36
3.4 On chip inductor using ADS.....41
3.5 Final layout and extraction..... 48

Chapter 4 Conclusion..... 52

References.....54

LIST OF FIGURES

Figure 1.1: Datarates for different wireless standards..... 2
Figure 1.2: ON-OFF pulse keying..... 5
Figure 1.3: Basic block diagram of the UWB transceiver 6
Figure 1.4: Block diagram of receiver..... 7
Figure 2.1: Two-port network..... 11
Figure 2.2: Single stage RF amplifier block diagram 13
Figure 2.3: Two-port representation of noise using the Z-parameters 15
Figure 2.4: Two-port representation of noise using the Y-parameters..... 16
Figure 2.5: Noise factor calculation..... 17
Figure 2.6: Interference from adjacent channel..... 19
Figure 2.7: Two-tone test to measure linearity of the LNA 20
Figure 2.8: 1-dB compression point..... 21
Figure 2.9: SFDR definition..... 22
Figure 2.10: Compression-Free Dynamic Range..... 23
Figure 3.1: Resistive terminated LNA..... 26
Figure 3.2: Common gate LNA..... 26
Figure 3.3: Shunt series feedback LNA..... 27
Figure 3.4: Current reuse LNA..... 28
Figure 3.5: C_{gd} neutralization LNA..... 29
Figure 3.6: Inductive source degeneration LNA..... 30
Figure 3.7: Proposed inductive source degeneration schematic..... 32
Figure 3.8: Gain vs. frequency simulation..... 36
Figure 3.9: LNA schematic with ports..... 37
Figure 3.10: Noise figure simulation..... 37
Figure 3.11: GA, GT and GP simulation..... 38
Figure 3.12: 1-dB compression point..... 39
Figure 3.13: IIP3 simulations..... 40
Figure 3.14: The spiral inductor-Π model..... 42
Figure 3.15: Pi-model generated in ADS..... 43
Figure 3.16: Inductor of 1.6 nH..... 44
Figure 3.17: S-parameter results for the spiral inductor..... 45
Figure 3.18: Generation of the Z-parameters in ADS..... 46
Figure 3.19: Simulated values of Q, L and r from Z-parameter..... 47
Figure 3.20: Layout without capacitors and inductors..... 49
Figure 3.21: Final layout..... 50

LIST OF TABLES

Table 1.1: Typical UWB receiver front-end specifications for LNA..... 7
Table 1.2: The TSMC technology process parameters from MOSIS Service..... 8
Table 2.1: Typical parameters of a UWB receiver..... 24
Table 3.1: Comparison between various topologies..... 31
Table 3.2: Component sizes for the LNA design..... 35
Table 3.3: Comparison between targeted and achieved results..... 40
Table 3.4: Substrate information of the inductor..... 43
Table 3.5: Inductor dimensions..... 44
Table 3.6: Comparison of results before and after inserting pi-models for inductors..... 48
Table 3.7: Comparison between schematic and extracted simulations..... 50
Table 3.8: Summary of comparison of this work with past works in LNA..... 51

Chapter 1 Introduction to UWB

1.1 UWB vs. various wireless standards

Ultra WideBand (UWB) technology has been designed to bring convenience and mobility of high speed wireless communication to homes and offices. It is specifically designed for short range Wireless Personal Area Networks (WPANs). UWB will play an instrumental role in freeing people from wires and enabling video transmission or other high bandwidth data transmission that is rarely possible with a conventional wireless connection.

The short range UWB technology will also complement other wireless standards such as Wi-Fi and Wi-Max. It can transmit data within the radius of 10 meters from the host device. UWB technology is designed to provide a short range, very low power connection with much more bandwidth than cable. Since UWB communicates with short range pulses, it can be used for tracking various objects.

It has been shown that a UWB device can successfully transmit data at a rate of 110 Mbps at a distance of 10 meters [1]. This bandwidth is 100 times faster than Bluetooth and twice as fast as Wi-Fi. This bandwidth is large enough to accommodate three concurrent video streams over a single connection. Designers are promising UWB products that have speeds of up to 1 Gbps [2]. A chart comparing the data-rates of different wireless technologies is shown in Figure 1.1.

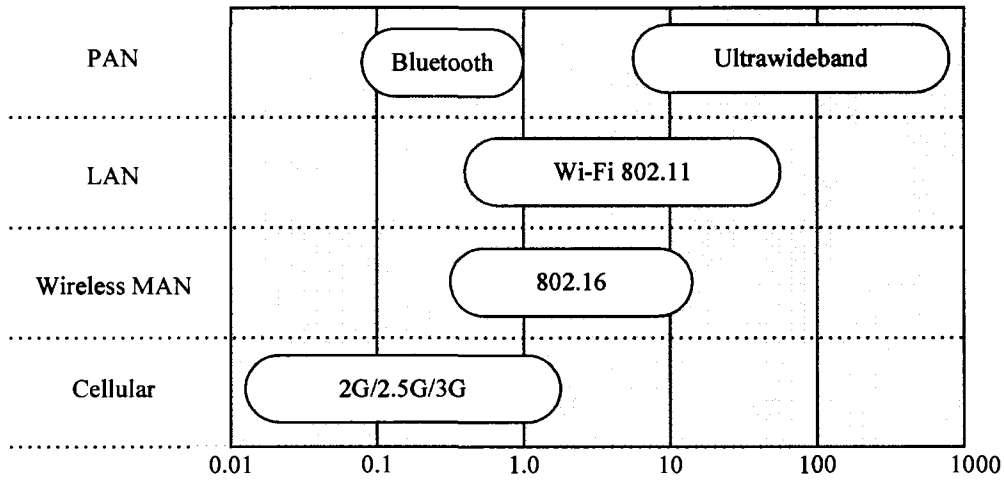


Figure 1.1: Data rates for different wireless standards

The implementation of UWB for data transmission through radio channel has the following advantages compared to narrow-band signals:

- UWB standard consumes very low average radiated power, which is usually expressed in units of miliwatts, though sometimes it depends on distance between the UWB transmitter and receiver.
- Since the spectral power per frequency band is very low, UWB communication is very secure. It is also electromagnetically compatible with narrow-band systems operating within the same frequency band.
- The higher bandwidth of UWB standard provides data rates up to 1 Gbps.
- UWB communication is robust to multi-path signal propagation due to the time selection of direct and re-scattered signals, and the correlation reception.

It is clear that UWB is a growing technology aiming to replace all other narrow-band technologies for short range communication.

1.2 UWB applications

The benefits of low power and high data rate of the UWB standard promises a great range of applications in the military, civilian, and commercial sectors. A brief summary of UWB applications is presented here.

UWB applications are categorized in three major areas: radar, imaging, and communication [2]. Radar is one of the most powerful applications of this technology. Narrow UWB pulses have fine positioning characteristics, and this particular trait enables them to offer higher resolution radar for military and civilian applications. Also, penetration of objects is possible because of the very wide frequency spectrum. In the commercial world, these types of radar systems can be used on construction sites to locate pipes, studs, and electrical wirings. The same technology can be used in medical applications such as a remote heart monitoring system. In the automotive industry it could be used to develop or enhance collision avoidance systems.

The low transmission power of UWB pulses makes UWB system ideally suited for military communication. Low power UWB pulses are extremely difficult to detect or intercept, which makes any UWB system very secure. UWB devices are much simpler as far as circuitry is considered, and can be manufactured in smaller size and at a lower cost than narrow-band systems. Small and inexpensive UWB transceivers are very useful in wireless sensor network applications for both military and civilian use. Such sensor networks can be used to detect physical objects, and transfer the detected information to a chosen destination. For military application a UWB system could provide detection of a biological agent or the location of the enemy on the battlefield. In the commercial sector

UWB applications may include habitat monitoring, environment observation, health monitoring, and home automation.

UWB can also connect Personal Computer (PC) and other entertainment components to a media PC or a mobile notebook PC for editing, compiling, and sending pictures or other multimedia files. UWB provides a fast and high quality connection. With UWB-enabled Wireless Private Area Networks (WPANs), once the devices are within the proximity, they can automatically recognize each other.

1.3 UWB Operation

A UWB signal can be defined as a signal in which the range of the frequency utilization factor changes between 0.25 and 1 and is defined by:

$$\eta = \frac{f_{up} - f_{low}}{f_{up} + f_{low}} \tag{1.1}$$

where f_{up} is the highest frequency of the frequency band and f_{low} is the lowest frequency of the frequency band.

UWB system makes efficient use of the basic behavior of UWB signals. The use of UWB short duration signals helps to maintain the high quality of the data transmitted. A reduction in the radiated pulse duration causes an efficient resistance to multi-path signal propagation, which is often generated by the signal re-scattering from objects located near the communication system antenna and from the line of sight between the signal source and the receiver. If the duration of the signal is 1.0 ns, and the objects

which cause signal re-scattering are located at a distance of more than 30 cm from the line of sight, the result will be undistorted signal detection [2].

Figure 1.2 explains ON-OFF pulse keying for a pulse duration of 1.0 ns. The pulse repetition frequency is 2.0 MHz. This type of modulation is suitable for UWB systems.

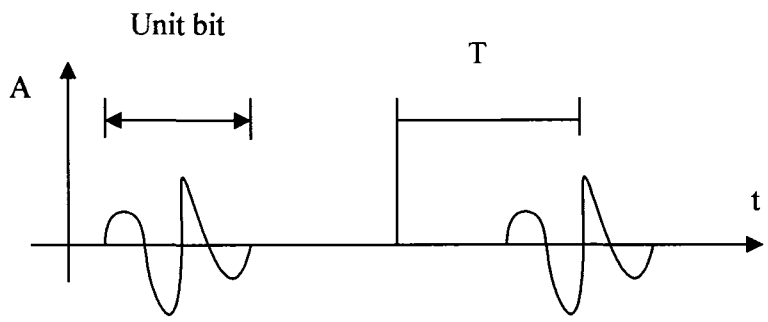


Figure 1.2: ON-OFF pulse keying

There are several methods to implement a UWB system. The next section discusses basic UWB architecture.

1.4 UWB transceiver

A basic block diagram of the UWB transceiver, including a transmitter and a receiver, is shown in Figure 1.3. The baseband Digital Signal Processing (DSP) unit controls the messaging and signaling of information. The DSP unit also synchronizes the system clock. The main function of the receiver is to amplify the signal without amplifying the noise. The principal role of the transmitter is to boost up the signal using some line drivers in order to send high energy signals.

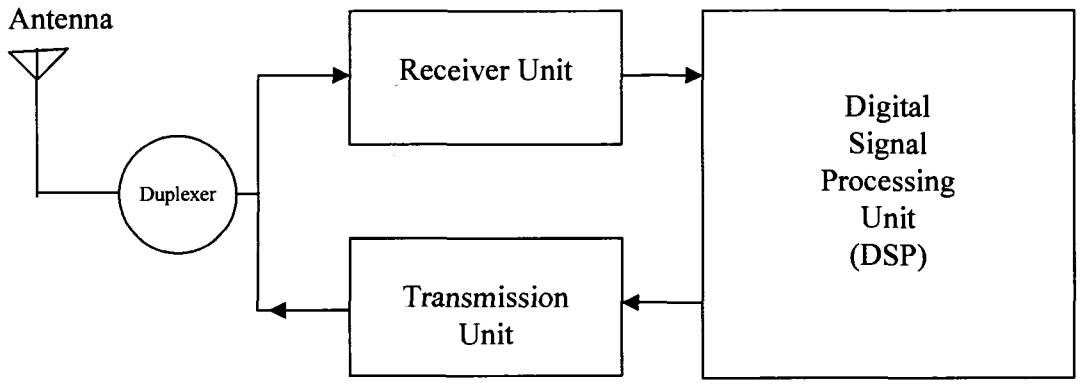


Figure 1.3: Basic block diagram of the UWB transceiver

The block diagram of a UWB receiver is shown in Figure 1.4. The receiver features a Low Noise Amplifier (LNA) followed by a mixer (demodulator). The mixer removes the carrier from the received radio frequency signal. Usually there is an automatic gain control block between the mixer and the Analog to Digital Converter (ADC). The purpose of this block is to balance the amplification or attenuation of the received signal in a way that it utilizes the maximum range of the ADC. The analog to digital converter then converts the analog signals to digital data which is fed to the DSP to process the transmitted data. The signal is then fed to the DSP block for baseband processing. In this context it is clear that an ultra wideband LNA should pass all the frequencies between 3.1 to 10.6 GHz. Such an amplifier must feature wideband input matching to a 50 Ω antenna for noise optimization and filtering of the out-of-band interferers. Moreover, it must show flat gain with good linearity and minimum possible noise figure over the entire bandwidth.

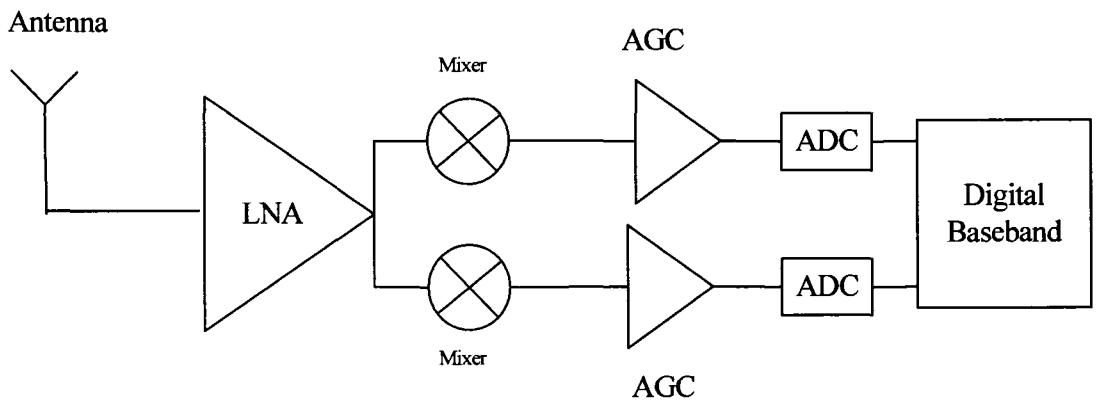


Figure 1.4: Block diagram of receiver

The LNA is an instrumental component of a UWB receiver. The LNA's noise figure has a major impact in deciding the system's overall noise figure, therefore this thesis deals with various aspects of the LNA design for a UWB device. The general specifications of a typical UWB LNA are listed in Table 1.1.

Table 1.1: Typical UWB receiver front-end specifications for LNA

Operating frequency	< 10 GHz
Gain	> 8 dB
Noise figure	< 3 dB
1-dB compression point	-15 to 5 dB
IIP3	-10 to 5 dB

1.5 Choice of technology

CMOS and Silicon Germanium are the main processes to implement RF circuits. Low power consumption and easy availability were the main reasons to choose the CMOS process for this thesis. TSMC 0.18μ CMOS technology was selected to design the LNA. This technology is available to the university lab from Metal Oxide Semiconductor Implementation Services (MOSIS). Table 1.2 shows some of the process parameters.

Table 1.2: The TSMC technology process parameters from MOSIS Service

No. of metal layers	6
Supply voltage	1.8 V
f_t of transistor	40 GHz
Metal 6 Thickness	0.99 μm
Substrate to metal 6 distance	5 μm

The f_t of the transistor is the unity current gain frequency. It is also known as cutoff frequency which is defined as the signal frequency at unity gain when the transistor is used as an amplifier. In other words, all the parasitic capacitors in the transistor become short-circuited at this frequency. TSMC 0.18μ CMOS technology consists of 6 metal layers and 1 poly-silicon layer which is designed for high speed low voltage applications. Metal 6 is the outer most of all the layers, and it is used for laying out the inductors.

1.6 Objective

This thesis mainly focuses on all five band groups of the UWB standard, and discusses different aspects of the LNA design. The basic objective of the LNA design is to get good gain with minimum noise generation for the entire UWB operating frequency. The gain aimed for this UWB LNA is greater than 8 dB, and the noise figure targeted is less than 3 dB for the entire band of 3 to 10 GHz. Along with good gain and noise figure, good linearity is also required for the LNA to operate properly. The1-dB compression point and IIP3 point are the characteristics measuring the linearity of the RF components. The objective is to get –10 dB of 1-dB compression point and IIP3 of –12dB. The targeted power dissipation is less than 20 mW.

Chapter 2 mainly focuses on the different characteristics of the LNA and how these traits affect the overall design. Chapter 3 discusses some popular topologies and the proposed LNA architecture along with providing simulation results. Chapter 3 also discusses implementation of the on-chip inductors using Advance Design System (ADS). Finally, Chapter 4 concludes the thesis.

Chapter 2 Low Noise Amplifier Characterization

The Low Noise Amplifier (LNA) is the first gain stage of a receiver. It must meet several specifications at the same time, which makes its design challenging. The signals coming from the receiver antenna are very small, usually from -100 dBm (3.2 V) to -70 dBm (0.1 mV), therefore signal amplification is needed before it is fed into the mixer. This process sets the requirement of a certain gain to the LNA. The received signal should have a certain Signal to Noise Ratio (SNR) in order to allow proper detection. Therefore, noise added by the circuit should be reduced as much as possible. A large signal or blocker can occur at the input of LNA. The circuits should be sufficiently linear in order to have a reasonable signal reception. For portable and mobile applications, reasonable power consumption is another constraint.

The gain, stability and noise figure of the LNA are usually measured using the scattering parameters (S-parameters), which will be studied in the next section.

2.1 S-parameters

The scattering parameters or S-parameters are widely used in microwave and RF circuit analysis. S-parameters are used to model and characterize an n-port linear network [3]. The linear equations describing the behavior of the two-port network using S-parameters are:

$$b_1 = S_{11}*a_1 + S_{12}*a_2 \tag{2.1}$$

$$b_2 = S_{21}*a_1 + S_{22}*a_2 \tag{2.2}$$

where b_1, b_2, a_1 and a_2 are traveling waves representing incident voltages at the ports.

The S-parameters S_{11}, S_{22}, S_{21} and S_{12} are defined by:

$$S_{11} = (b_1 / a_1) \text{ where } a_2 = 0 \tag{2.3}$$

$$S_{22} = (b_2 / a_2) \text{ where } a_1 = 0 \tag{2.4}$$

$$S_{21} = (b_2 / a_1) \text{ where } a_2 = 0 \tag{2.5}$$

$$S_{12} = (b_1 / a_2) \text{ where } a_1 = 0 \tag{2.6}$$

For most measurements and calculations, it is convenient to assume that the port reference impedances Z_S and Z_L are positive and real. I_1 and I_2 are currents referring to the input and output ports, respectively. One such model is shown in Figure 2.1. Each port can have distinct reference impedance, but the same reference impedance Z_0 will be used for all the ports here.

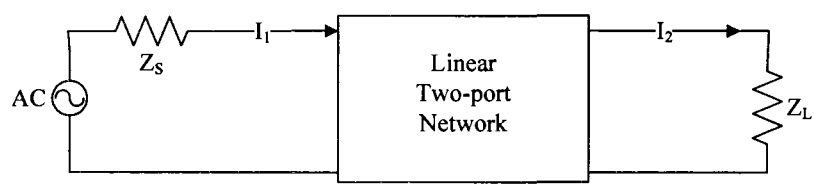


Figure 2.1: Two-port network

The independent variables a_1 and a_2 can also be related to port voltages (V_1, V_2) and currents (I_1, I_2) as follows:

$$a_1 = (V_1 + I_1 Z_0) / (2 \sqrt{Z_0}) \tag{2.7}$$

$$a_2 = (V_2 + I_2 Z_0) / (2 \sqrt{Z_0}) \tag{2.8}$$

Similarly, the dependent variables b_1 and b_2 can also be related to port voltages and currents as follows:

$$b_1 = (V_1 - I_1 Z_0) / (2 \sqrt{Z_0}) \tag{2.9}$$

$$b_2 = (V_2 - I_2 Z_0) / (2 \sqrt{Z_0}) \tag{2.10}$$

From the above explanation of a_1, a_2, b_1, and b_2, the four S-parameters are simply related to power gain and mismatch loss:

$|S_{11}|^2 =$ (Power reflected from the input) / (Power incident on the input) (2.11)

$|S_{22}|^2 =$ (Power reflected from the input) / (Power incident on the output) (2.12)

$|S_{21}|^2 =$ (Power delivered to the load) / (Power available at the source) (2.13)

$|S_{12}|^2 =$ Reverse transducer power gain with Z_0 load and source (2.14)

2.2 Amplifier's gain and stability

There are two criteria that affect the gain performance of any RF amplifier: the RF transistor itself and the input output matching network. A simplified block diagram is shown in Figure 2.2. The amplifier is characterized by its S-parameters and terminated by the source and load impedance Z_s and Z_L, respectively. S_{11} and S_{22} are the input and output reflection coefficients. The load of the next stage follows the output matching network. The input and output reflection coefficients Γ_{in} and Γ_{out} for a two-port network are [4]:

$$\Gamma_{in} = (b_1 / a_2) = S_{11} + (S_{12} S_{21} \Gamma_L / (1 - S_{22}\Gamma_L)) \quad (2.15)$$

$$\Gamma_{out} = (b_2 / a_2) = S_{22} + (S_{12} S_{21} \Gamma_s / (1 - S_{11}\Gamma_s)) \quad (2.16)$$

where

$$\Gamma_L = (Z_s - Z_0) / (Z_s + Z_0) \quad (2.17)$$

$$\Gamma_s = (Z_L - Z_0) / (Z_L + Z_0) \quad (2.18)$$

where Γ_L is source reflection coefficient, Γ_s is load reflection coefficient, and Z_0 is reference impedance.

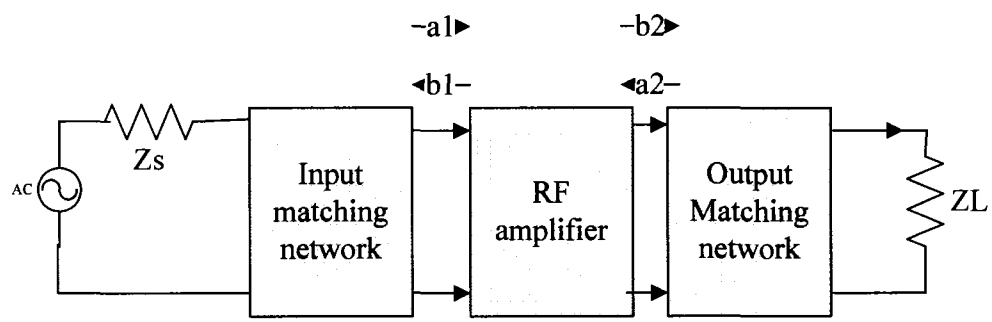


Figure 2.2: Single stage RF amplifier block diagram

If the input and output are simultaneously complex conjugate matched, i.e. $\Gamma_{in} = \Gamma^*_s$ and $\Gamma_{out} = \Gamma^*_L$, the amplifier has maximum power transfer. Achieving the simultaneous complex conjugate matching condition is not easy. A special case is for a unilateral device where S_{12} is practically zero, then $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. If the input and output are decoupled from each other, matching can be done at the input and output separately.

Several gain definitions exist for an amplifier. Power gain (G) characterizes the actual power amplification of an amplifier, and it is defined by:

$$\text{Power gain} = \frac{\text{Available power at output}}{\text{Power at the input}} \tag{2.19}$$

Available power gain (GA) shows the maximum possible power amplification of the amplifier. For IC implementations, the LNA input is interfaced off-chip and is usually matched to specific impedance (50 Ω or 75 Ω). An LNA's output is not

necessarily matched when it is directly driving on-chip blocks such as mixers [5]. This situation is usually characterized by LNA's voltage gain or transducer power gain.

The voltage gain (A_V) is defined as the voltage at the output port divided by the voltage at the input port of the amplifier and is given by:

$$A_V = (V_2 / V_1) = [S_{21} (1 + \Gamma_L)] / [(1 - S_{22}\Gamma_L) (1 + \Gamma_{in})] \quad (2.20)$$

The transducer gain (GT) is defined as power delivered to the load divided by the power available at the source [6]:

$$G_T = (P_L / P_{AVS}) \quad (2.21)$$

where P_L equals the power incident on load minus the power reflected from load. P_{AVS} is the power available at the source.

$$P_L = |b_2|^2 (1 - |\Gamma|^2) \quad (2.22)$$

2.3 Noise performance

The noise performance of an RF amplifier is represented by its noise factor or noise figure. The noise factor accounts for the degradation of the signal's SNR due to the amplifier. It is defined as the SNR at the input of the network divided by the SNR at the output of the network [7]:

$$F = (SNR_{in} / SNR_{out}) \quad (2.23)$$

where SNR_{in} and SNR_{out} are the SNRs at the input and output of the amplifier, respectively. The noise factor represents the signal's quality in terms of noise before and after the network. The noise figure is the same as the noise factor expressed in dB.

$$NF\ (dB) = 10 \log F \quad (2.24)$$

It would be complex if one tried to use a transistor's equivalent noise circuit to analyze the whole amplifier or network. A two-port network noise model can simplify the calculation of its noise factor of a network. An effective way to analyze noise in a given circuit is to assume that the circuit is noiseless, and to model its internal noise by external noise sources at the input and output ports of the circuit. These noise sources must have the same noise power appearing at the circuit's terminals as the original noisy circuit. The noiseless network can be represented by its Z- and Y-parameters. In the following discussions, it is assumed that port 1 is the input port and port 2 is the output port.

Using the Z-parameters in Figure 2.3, the voltage-current relationship among ports can be written as:

$$V_1 = Z_{11}I_1 + Z_{12}I_2 + V_{n1} \tag{2.25}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 + V_{n2} \tag{2.26}$$

The equivalent noise source V_{n1} and V_{n2} can be measured from the open-circuited measurements as:

$$V_{n1} = V_1 \text{ where } i_1=i_2=0 \tag{2.27}$$

$$V_{n2} = V_2 \text{ where } i_1=i_2=0 \tag{2.28}$$

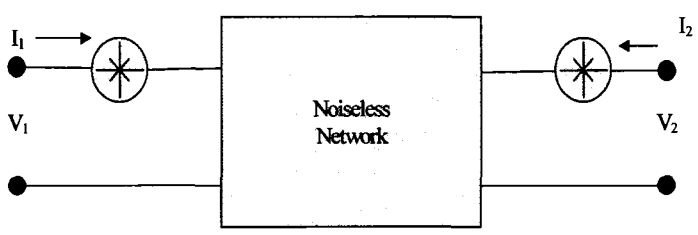


Figure 2.3: Two-port representation of noise using the Z-parameters

Using the Y-parameters in Figure 2.4, the voltage-current relationships among ports can be written as:

$$I_1 = Y_{11}V_1 + Y_{12}V_2 + I_{n1} \tag{2.29}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 + I_{n2} \tag{2.30}$$

The equivalent noise source I_{n1} and I_{n2} can be obtained from the short-circuited (s.c.) measurements as:

$$I_{n1} = I_1 \text{ where } V_1=V_2=0 \tag{2.31}$$

$$I_{n2} = I_2 \text{ where } V_1=V_2=0 \tag{2.32}$$

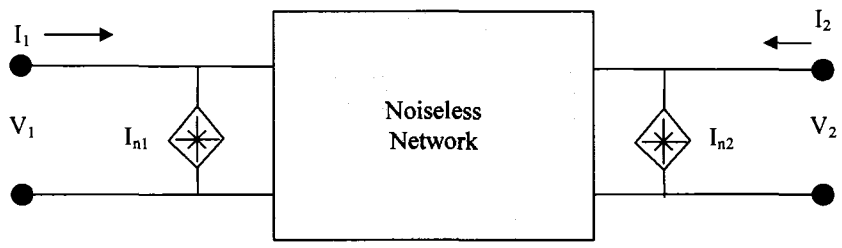


Figure 2.4: Two-port representation of noise using the Y-parameters

Referring the noise sources to the input port is convenient for the noise analysis. Therefore, the noise factor of a two-port network can be calculated using the noise representation in Figure 2.5. Consider a general network with a noise current source connected at its input port as shown in Figure 2.5. It is assumed that the noise of the source and the noise of the network (I_n and V_n) are uncorrelated, but the possibility exists for cases where V_n and I_n may be correlated.

The total output noise power is proportional to the mean square value of the short-circuited current ($I_{s.c}$) at the input port, whereas the input noise power is proportional to the mean square value of the source current (I_s). The noise factor is then calculated by:

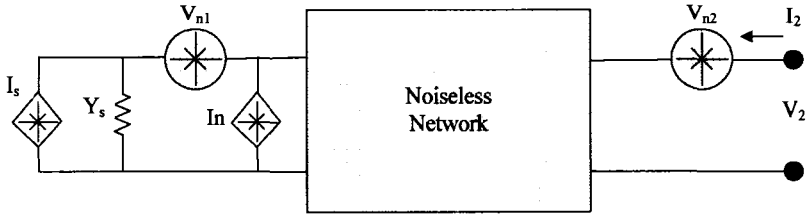


Figure 2.5: Noise factor calculation

$$F = [(\text{mean square of } I_{s.c.}) / (\text{mean square of } I_s)] \tag{2.33}$$

where $I_{s.c.}$ = [mean square of I_s + mean square of $(I_n + V_n Y_s)$] and Y_s is the source admittance.

So, it is clear from the above discussion that it is easier to analyze the noise when the circuit under analysis is assumed to be noiseless and noise is seen as an external effect. The next section describes the system sensitivity and its dependence on the gain and noise factor.

2.4 The LNA gain, noise factor, and system sensitivity

The importance of the gain and noise factor specifications on an LNA can be discussed further from the receiver's system sensitivity aspect. The smallest input signal power that can be reliably detected by the system is called the system sensitivity (P_s):

$$P_s = 174\text{dBm} + 10 \log BW + SNR + 10 \log F_{tot} \tag{2.34}$$

The first two terms in equation 2.34 are usually referred to as the noise floor. BW is the system bandwidth and is determined by a specific application. For UWB application BW should be approximately 7.5 GHz. The SNR is determined by the Bit Error Rate (BER) requirement of the system. For example, for a UWB receiver, simulation shows that an 8 dB SNR is needed for a BER lower than 10^{-4}, and for an

802.11b receiver, an 11.4 dB SNR is required to achieve better than 10^{-5} BER. F_{tot} is the system's total noise factor, and it is directly affected by the LNA's gain and noise factor. F_{tot} can be calculated by:

$$F_{tot} = F_{LNA} + [(F_{afterLNA} - 1) / G_{LNA})] \tag{2.35}$$

where F_{LNA} is noise figure of the LNA, G_{LNA} is the current gain of the LNA, and $F_{afterLNA}$ is noise figure of the system excluding the LNA.

Equation 2.35 shows that the LNA's noise factor F_{LNA} appears directly in the system's noise factor. For high sensitivity a low system noise factor is required, therefore F_{LNA} should be made as small as possible. The second term of equation 2.35 shows that noise coming from the stages following the LNA will be suppressed by the LNA's gain; hence a high gain LNA is desirable for high sensitivity. For example, in a UWB receiver, if the LNA's noise figure is 3 dB, its available power gain G_{LNA} is 8 dB and the overall noise figure of the circuits following the LNA is 18 dB, then the system's total noise figure can be found using equation 2.35 to be 7.4 dB. If the LNA's gain is increased to 15 dB, the total noise figure will be reduced to 4.1 dB, and the system sensitivity will be improved by 3.3 dB. If the 7.4 dB noise figure is a fixed system specification, the noise figure requirement on the circuits after the LNA can be relaxed to 24 dB. On the other hand, a high gain of the first stage, which is the LNA in this case, will put a more stringent linearity requirement on the following stages. Therefore a trade off must be made amongst gain, noise, and linearity.

2.5 Large signal behavior

The RF amplifier is a non-linear system in nature. If the input signal is small enough, the circuit can be modeled using a linear model around its operating point. But if the signal level is relatively high, due to the non-linearity, the amplifier's dynamic operation point will be changed and will become a function of the signal level. The LNA's proper operation must be checked by using a large signal input. On the other hand, although the signal itself is small, large interferers may come together with the signal. This situation is shown in Figure 2.6, where f_a and f_b are upper and lower bound frequencies of the desired spectrum and f_1 and f_2 are external interferers. The interferers can come from the adjacent channel or can be generated by an intentional jamming system.

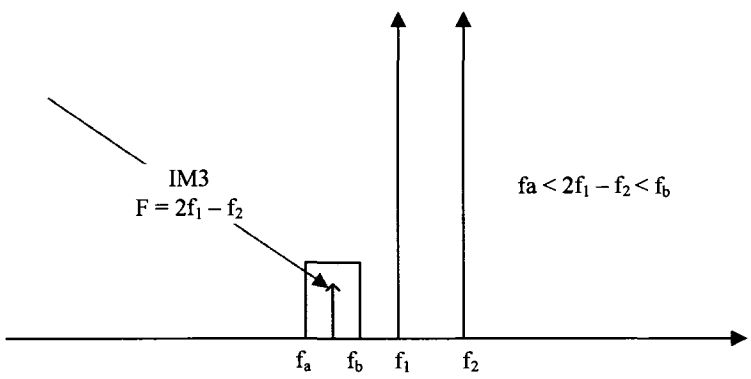


Figure 2.6: Interference from adjacent channel

Interference specifications are usually provided by the system standards. The non-linearity of performance is characterized by the two-tone test (f_1, f_2) as depicted in Figure 2.7. Usually, the distortion terms ($2f_1$ - f_2) and ($2f_2$ - f1) fall in-band, and are characterized by 3rd order non-linearity. For example in a UWB receiver, the desired

signal channel in Figure 2.7 has a bandwidth of 7.5 GHz and is centered at 6 GHz. Two large blockers are located at 12 GHz and 18 GHz, which are separated by 6 GHz. Thus the lower side IM3 component will be at $(2f_1 - f2) = 6$ GHz, which is directly upon the center of the channel. A large in-band blocker tends to desensitize the circuit. The 1-dB compression point measures the effects of intermodulation.

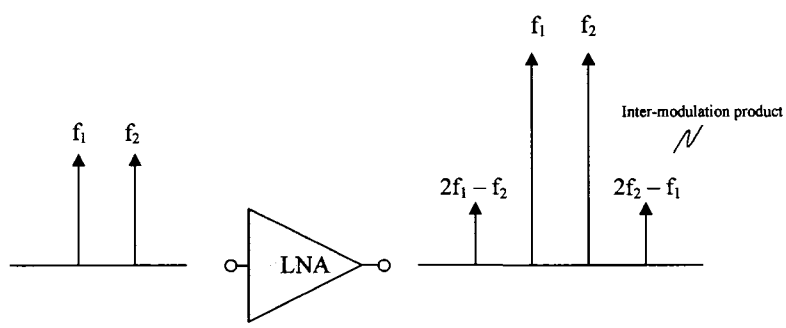


Figure 2.7: Two-tone test to measure linearity of the LNA

2.5.1 1-dB compression point

The 1-dB compression point (P1dB) is the point (input or output) where the fundamental gain is reduced by 1 dB from the ideal small signal gain at a certain frequency. Assuming that the non-linear system can be approximated by the Taylor series:

$$Y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \text{-----} \tag{2.36}$$

The 1-dB compression point can be calculated as:

$$P_{1dB} = \sqrt{[0.145\ (\alpha_1 / \alpha_3)]} \tag{2.37}$$

where α_1 and α_3 are the 1st-order and 3rd-order coefficients of the Taylor series expansion of the system's input/output characteristics as in equation 2.36. The 1-dB compression point is illustrated in Figure 2.8.

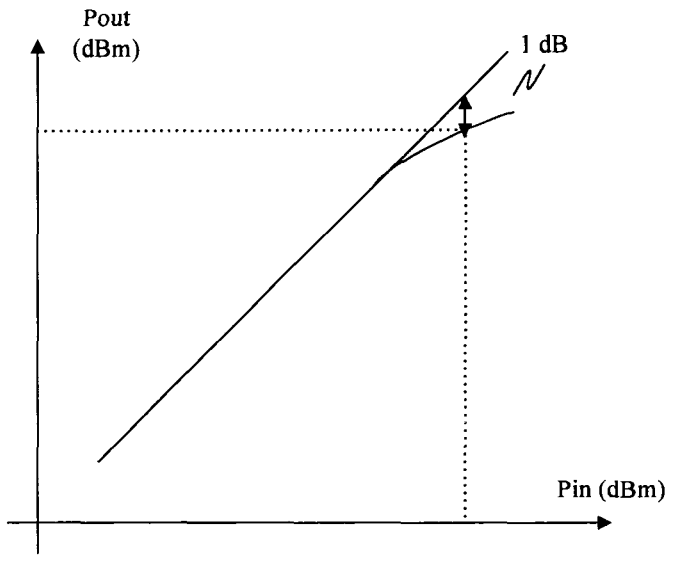


Figure 2.8: 1-dB compression point

2.5.2 Intercept point

The two-tone test can also show the impact of a potential interferer on the desired signal. Due to the non-linearity of the circuit, the 2nd and 3rd order inter-modulation products will appear at the output and may lie within the pass band, which can degrade the quality of the output signal.

Typically, the desired output (fundamental), the 2nd order inter-modulation output (IM2), and the 3rd order inter-modulation output (IM3), are plotted as a function of the input signal level. The 2nd order intercept point (IP2) is the extrapolated intersection of the fundamental curve and the IM2 curve. The 3rd order intercept point (IP3) is the extrapolated intersection of the fundamental and IM3 curves. For the system described by equation 2.36, the input-referred IP3 (IIP3) is given by:

$$\text{IIP3} = \sqrt{1.33\,(\alpha_1 / \alpha_3)} \tag{2.38}$$

2.5.3 Dynamic range

In simple words, dynamic range can be defined as the ratio of maximum to minimum input levels at which the circuit operates with reasonable distortion and output signal quality. Two different definitions are usually used: Spurious-Free Dynamic Range (SFDR) and Compression-Free Dnamic Range (CFDR).

Figure 2.9 shows the definition of SFDR. The upper bound of SFDR is based on inter-modulation behavior, and is defined as the maximum input level in a two-tone test for which the 3rd order inter-modulation (IM3) products do not exceed the noise floor. It can be shown that the input level for which the IM3 products become equal is:

$$P_{in,max} = (2 * IIP3 * N_{floor}) / 3 \tag{2.39}$$

where N_{floor} = 174 dBm + NF + 10 logBW, is the noise floor. All the quantities are expressed in dBm. The lower bound of SFDR is limited by the system sensitivity. If for a certain required signal quality the minimum SNR is SNR_{min}, then the minimum detectable signal level in dBm at the input is:

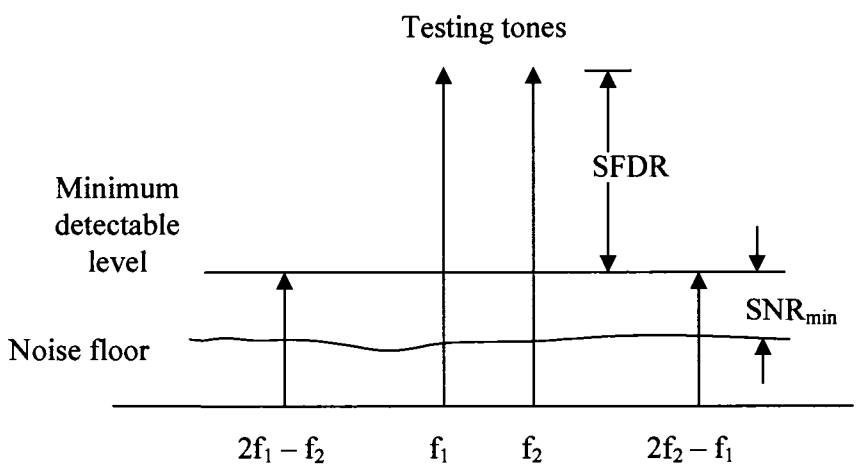


Figure 2.9: SFDR definition

$$Pi_{n;min} = SNR_{min} + N_{floor} \tag{2.40}$$

This process is also shown in Figure 2.9. The SFDR is then calculated by the difference between $Pi_{n;max}$ and $P_{in;min}$:

$$SFDR = 0.66\ (IIP3 - NF - 10\log B + 174\ dBm) - SNR_{min} \tag{2.41}$$

Compression-Free Dynamic Range (CFDR) is the difference, in dB, between the input-referred 1-dB compression point and the noise floor as shown in Figure 2.10:

$$CFDR = P1dB - N_{floor} \tag{2.42}$$

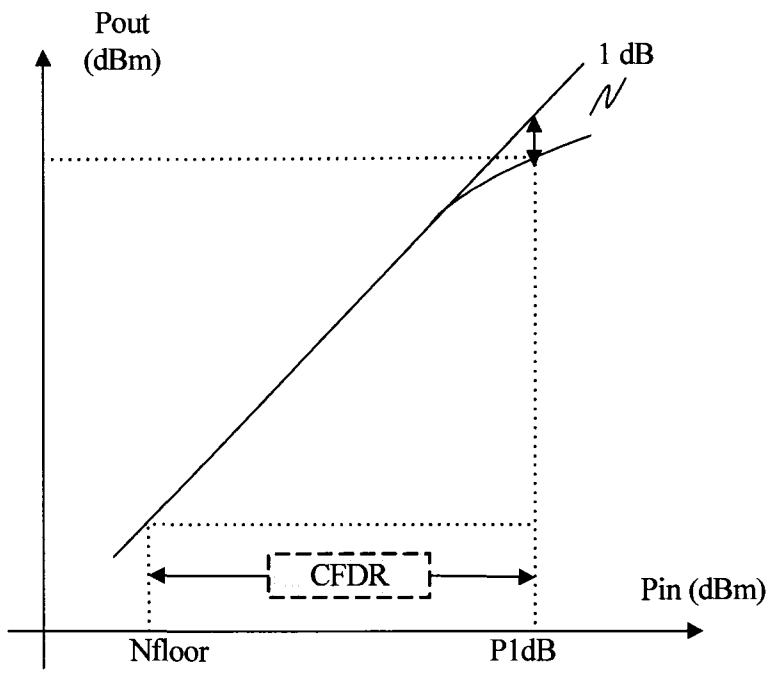


Fig. 2.10: Compression-Free Dynamic Range

Here is a numerical example. Suppose an UWB receiver has the system specifications as shown in Table 2.1.

Table 2.1: Typical parameters of a UWB receiver

Parameter	Value
SNR_{min}	3 dB
BW	7.5 GHz
IIP3	-13 dBm
NF	4 dB

The noise floor N_{floor} calculated from the above data is -40 dBm. From equation 2.39 and 2.40, $P_{in;max}$ and $P_{in;min}$ are -22 dBm and -37 dBm, respectively. Thus SFDR is 42 dB. The 1-dB compression point can be estimated from the IIP3, which is usually 10 dB larger than P1dB, therefore CFDR is about 46 dB.

In this chapter of the thesis different parameters of the LNA were discussed. These parameters can affect the functionality of the LNA. Careful consideration of all these parameters can result in a fully working LNA. The next chapter discusses various popular LNA topologies along with a proposed LNA with results.

Chapter 3 LNA Design

3.1 Popular LNA topologies in CMOS technology

The LNA usually only involves one or two transistors to achieve low noise operation. The performance of the LNA circuits is very dependent on process technology. CMOS technologies are the best choice to design an LNA because they offer high speed operation, simplicity in fabrication, and low power consumption. The following discussion presents several popular LNA structures possible in a CMOS integrated circuit. The LNA input is directly connected to a filter for impedance and noise matching. Therefore, different LNA structures have different methods to achieve impedance matching.

The structure shown in Figure 3.1 achieves input impedance matching by directly placing a 50 Ω resistor (R_S) in parallel with the gate of transistor M1. This is the most straightforward method but the noise figure will be exceptionally high. The lower bound of the LNA noise factor is given by:

$$F \geq 2 + (4\gamma / \alpha g_m R_s). \tag{3.1}$$

where $\alpha = g_m/g_{do}$, g_{do} is the drain source conductance, and γ is a constant with a value of 0.66. Since the term $(\gamma / \alpha g_m R_s)$ is larger than 1, the noise figure is readily larger than 6 dB. The primary contribution of noise comes from the termination resistor R_S and the drain of the transistor. Due to the noise performance limitations this LNA structure is rarely used [3].

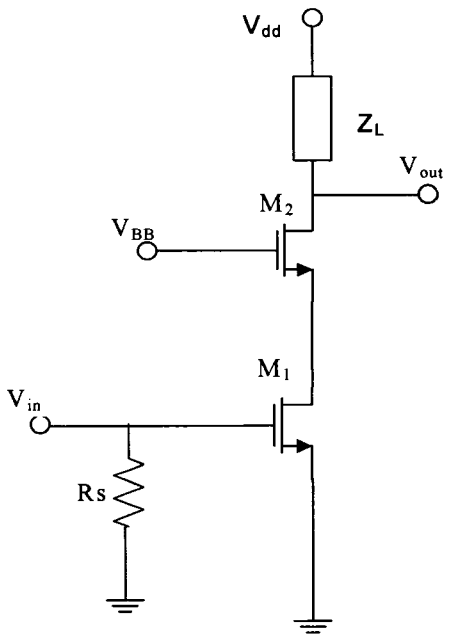


Figure 3.1: Resistive terminated LNA

A Common gate amplifier structure, shown in Figure 3.2, has better input impedance than a common source structure [6]. For the first order approximation, the essential part of input impedance is just $1/g_m$.

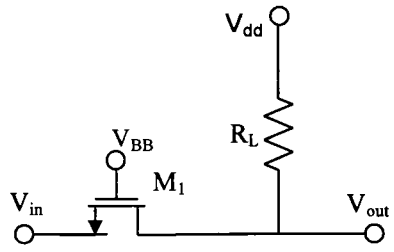


Figure 3.2: Common gate LNA

By carefully choosing the size of the transistor and biasing conditions, the 50 Ω impedance matching can be easily obtained. Ignoring the gate current noise, a lower bound of noise factor for this topology is represented by $F \geq 1 + (\Upsilon/\alpha)$. This minimum noise factor is about 2.2 dB and 4.8 dB for a long and short channel device, respectively

[3]. The gate current noise will make the noise factor larger, but the drain noise will still be the dominant factor.

The shunt series feedback LNA, shown in Figure 3.3, uses negative shunt feedback to modify the input impedance of a common source stage. Its input impedance can be approximately calculated by:

$$Z_{in} = R_F / (1 + A) \tag{3.2}$$

where A is the voltage gain which is approximately in the order of R_L/R_1 assuming the g_m of M_1 is very large.

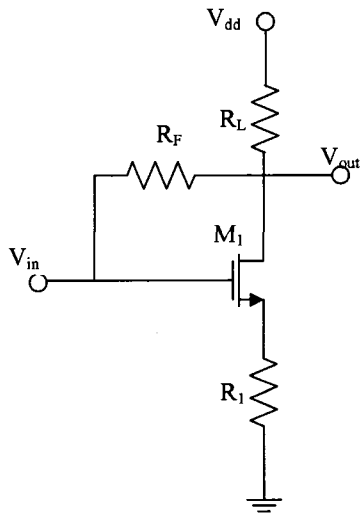
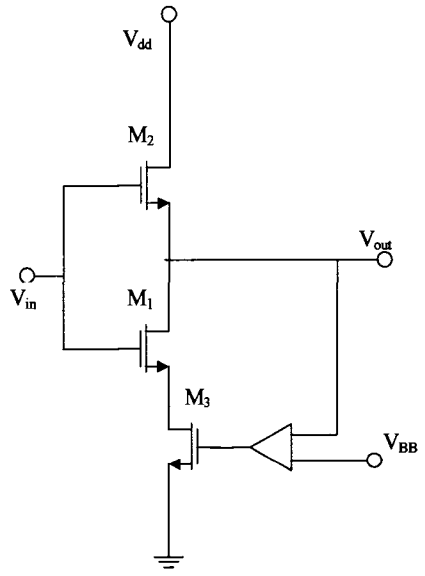


Figure 3.3: Shunt series feedback LNA

The noise figure of this structure is better than that of the resistively terminated LNA structure but it is still too high to use in applications such as a UWB receiver. The gate noise is the largest noise contributor in the shunt series feedback LNA structure. This is because the gate noise current experiences high impedance due to the resonance of the input matching network. Therefore, in order to reduce the noise figure, the quality

factor of the input matching network should be reduced leading to an impact on the signal quality and filtering.

The basic issue with using a CMOS transistor for the LNA is its inherently low transconductance and hence low gain. However, if the current reuse technique is employed, transconductance could be increased as much as two-fold. Figure 3.4 shows a simplified schematic of the current reuse LNA. The key point is that given the same bias current the effective transconductance is $gm_1 + gm_2$, while it is simply gm_1 in the case of the topologies mentioned previously. A major drawback of this design is its high input and output impedances, thus requiring external impedance matching networks. This prevents the use of this LNA in fully integrated applications. Due to the high gain property, the strong Miller effect reduces the reverse isolation of this LNA. In the actual design, two identical stages are cascaded to improve the reverse isolation.



Fugure 3.4: Current reuse LNA

The reverse isolation of the LNA is limited by the drain-source parasitic capacitor C_{gd}. In order to improve the reverse isolation of the LNA, a C_{gd} neutralization technique can be used as shown in Figure 3.5. An inductor L_F is added in parallel with this capacitor to provide a different feedback polarity to cancel the effect of C_{gd}. The inductive feedback may incur some potential stability issues because of the negative feedback. During the design of a C_{gd} neutralization LNA, the instability issue must be avoided.

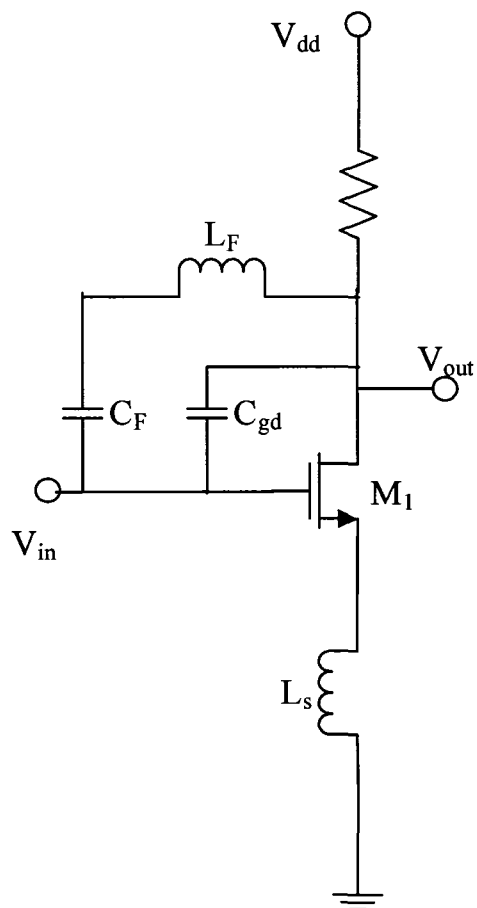
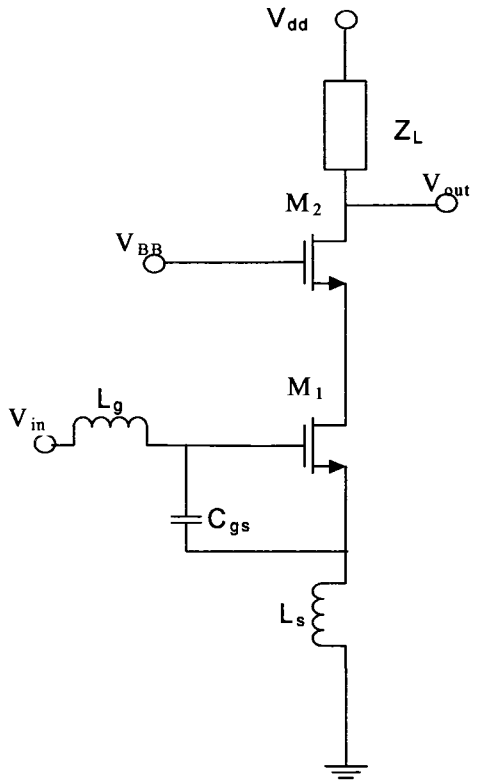


Figure 3.5: C_{gd} neutralization LNA

Figure 3.6 shows the structure of the inductive source degeneration LNA which is used for the design of LNA for this thesis. Transistor M_1 is in the common source configuration and M_2 is in the common gate configuration, which has a benefit of higher input impedance. Degeneration inductor L_s provides negative feedback to the amplifier and stabilizes the gain.



3.6: Inductive source degeneration LNA

Table 3.1 compares all the topologies discussed before. As shown in Table 3.1 it can be proven that inductive source degeneration LNA has a good narrowband match and a very small noise figure. Good input output match and noise figure are essential requirements for any UWB LNA design. Since UWB is such a low power technology, one cannot afford to add too much noise into the system. Research has shown that the

source degeneration is the best suitable topology for the UWB related LNA [7]. The next section discusses proposed design and simulations for the source degeneration LNA.

Table 3.1: Comparison between various topologies

Topology	Plus Point	Minus Point
Resistive termination	Good input match	Large NF
Common gate	Excellent input match	Huge NF and power
Series shunt feedback	Broadband i/o match	Stability issues
Inductive degeneration	Good narrowband match, Small NF	Large area
Current resue	High gain low power	External matching network required
Inductor neutralization	Good reverse isolation (S_{22})	Increased area, stability concerns

3.2 Proposed LNA design

The proposed schematic is shown in Figure 3.7. A Chebyshev filter is used to achieve resonance in the reactive part of the input impedance over the whole frequency range of 3.1 to 10.6 GHz. Typically the Chebyshev filter consists of two capacitors and two inductors. The Chebyshev filter works as a passband filter if the sizes of L_1, C_1, L_2 and C_2 are selected correctly.

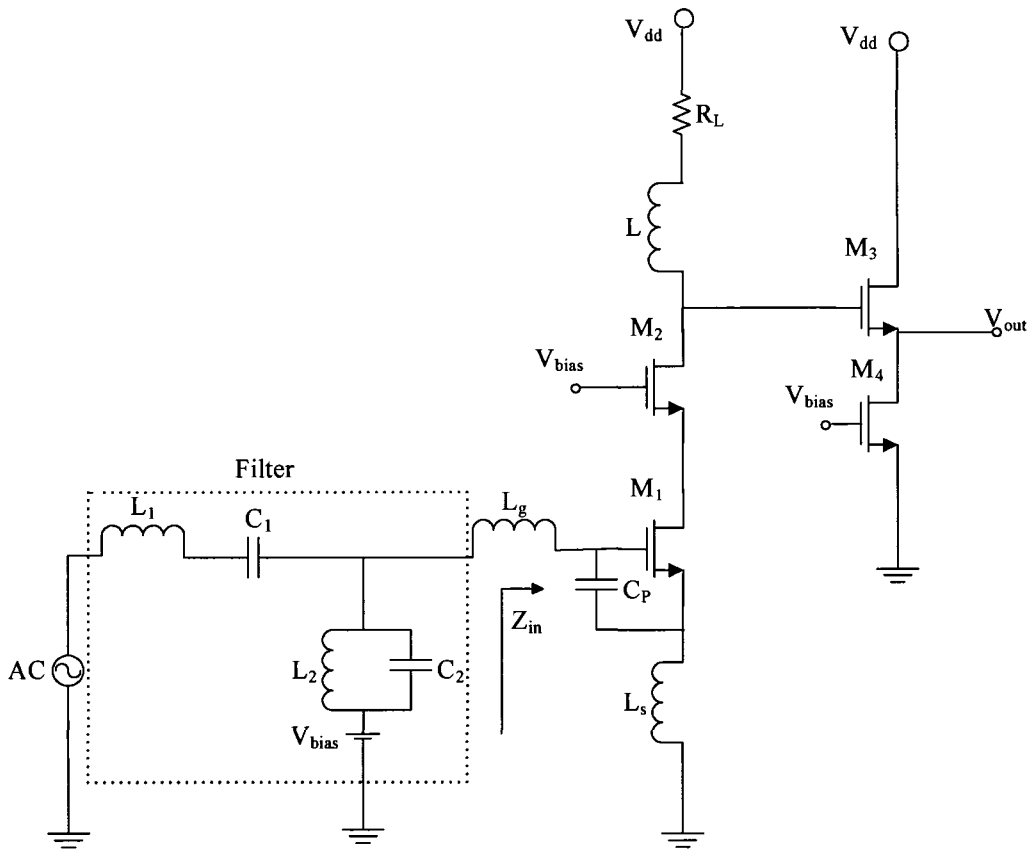


Figure 3.7: Proposed inductive source degeneration schematic

The proposed solution expands the basic inductively degenerated common source amplifier by inserting an input multi section reactive network, so that the overall reactance can be resonated over a wider bandwidth. This input matching network is shown in the Figure 3.7 by a dotted square. An inductor (L_g) is placed in series with a capacitor (C_p) to add flexibility to the design. Different values of L_g and C_p would give different matching conditions. The cascade connection of M_1 and M_2 improves the input output reverse isolation and the frequency response of the amplifiers. The source follower stage (M_3 and M_4) is used for measurement purposes.

3.2.1 Input match analysis

As seen in the circuit, the input impedance of transistor M_1 is a series RLC circuit given by:

$$Z_{in}(s) = (1/(C_{gs}+C_p)) + s(L_s+L_g) + W_T L_s \tag{3.3}$$

where W_T is given by:

$$W_T = g_m/(C_{gs} + C_p) \tag{3.4}$$

In order to get good input impedance matching, the real part of Z_{in} should match with source resistance in the circuit. In the passband of the filter, the power loss is 0 dB with a ripple ρ. There is a nonzero power loss for the frequencies not included in the passband, and that is how band rejection works. The choice of reactive elements in the filter determines the bandwidth of the in-band ripple. The input reflection coefficient Γ is related to ρ by:

$$|\Gamma|^2 = 1 - (1/\rho) \tag{3.5}$$

The input reflection coefficient (Γ) is a good measure of the input matching. The lower the reflection coefficient the better input matching is achieved.

3.2.2 Gain analysis

The input network impedance is equal to $R_s/W(s)$ where W(s) is the Chebyshev filter transfer function given by:

$$W(s) = \omega L_1 + (1/\omega C_1) + \omega L_2 \tag{3.6}$$

Note that W(s) is approximately unity in the in-band and tends to zero at out-of-band. The impedance looking into the amplifier is therefore equal to R_s in the in-band, and it is very high out-of-band. At high frequency the MOS transistor acts as a current

amplifier because of the channel length modulation effect. The current gain is given by $\beta(s) = g_m/(sC_t)$ [6]. The current flowing into M_1 is $[V_{in}\ W(s)]/R_s$ and therefore the output current is $V_{in}W(s)/(sC_tR_s)$.

The load of the LNA is a shunt peaking transistor used as a resistor. The overall gain is:

$$\frac{V_{out}}{V_{in}} = \frac{[G_m W(s)]\quad[R_L\,(1+sL/R_L)]}{[SC_tR_s]\quad[1+sR_LC_{out} + sLC_{out}]} \tag{3.7}$$

where, R_L is the load resistance, L is the load inductance, and C_{out} is the total capacitance between the drain of M_2 and ground. That means $C_{out} = C_{db2}+C_{gd3}$, where C_{db2} is the drain and bulk capacitance and C_{gd3} is the gate and drain capacitance of transistor M_3. Equation 3.7 shows that the current gain roll is compensated by L because it is directly connected to the drain of transistor M_2. Moreover, it shows that C_{out} introduces a spurious resonance with L, which must be kept out of the band.

Table 3.2 shows the sizes of the transistors, inductors, capacitors, and resistor used in the design. The width of M_1 is optimized for noise. It is chosen in order to strike a balance of thermal and induced gate noise for a given current budget of 5 mA. This value of M_1 is appropriate for noise reduction but it is not appropriate for the impedance matching [7]. L_g, L_s, and C_p combine with M_1 to achieve appropriate Z_{in}. Simulation helps in choosing the final values of these components: L_g=1.4 nH, L_s=1 nH and C_p=100 fF. The value of M_2, which is in cascode connection to M_1, is chosen to be as small as possible in order to reduce the parasitic capacitance [7]. But there is a lower limit to this

value because of the noise contribution of the device. The value selected for M_2 is 60 μm. The length of all the transistors used in the design is the minimal length (0.18 μm).

The load (L and R_L) is designed to get flat gain over the whole bandwidth. The value of L has a trade off between large gain and resonance frequency [8]. The goal is to get a large enough gain over the entire frequency range with its resonance out of the band. R_L is chosen to improve the gain at lower frequencies. A very large value of R_L (higher than 200 Ω) could result in reduction of the headroom. Keeping all these criteria in mind, the value chosen for R_L and L are 90 Ω and 2 nH, respectively. The buffer stage (M_3 and M_4) must drive a 50 Ω load. Both transistors are required to be in saturation for the chosen biased current (5 mA). The calculated values for M_3 and M_4 are 60 μm and 20 μm, respectively.

Table 3.2: Component sizes for the LNA design

Transistors width	M_1=240 μm, M_2=90 μm, M_3=60 μm, M_4=20 μm
Transistor length	0.18 μm for all the transistors
Resistor	R_L= 90 Ω
Capacitors	C_p=100 fF,C_2=490 fF, C_1=650 fF
Inductors	L_1=1.3 nH, L_2= 1.6 nH, L_g=1.4 nH, L_s=1 nH, L=2nH
Supply voltage	1.8 V
Power Dissipation	9 mW

The gain and input matching analysis of the design provide a better view about the design procedure of the LNA. The next section describes simulation results.

3.3 Simulations and results

3.3.1 Gain vs. frequency simulation

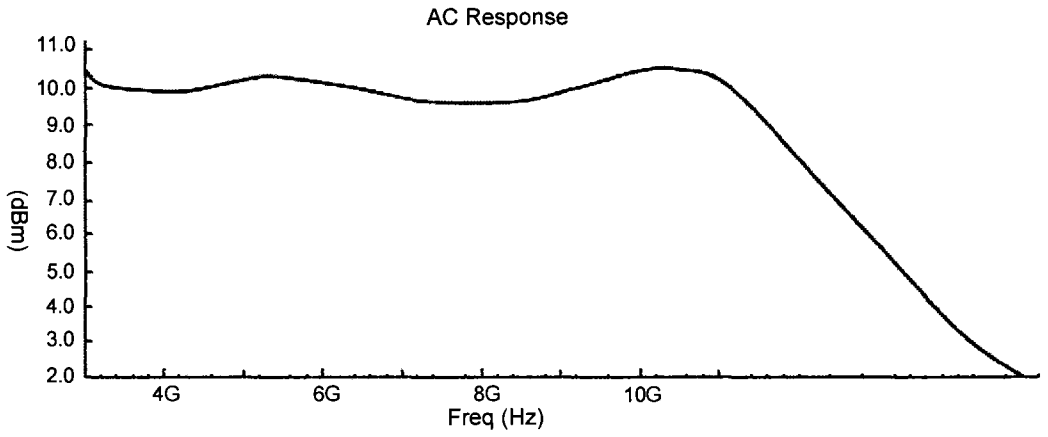


Figure 3.8: Gain vs. frequency simulation

As clearly seen from Figure 3.8, the circuit has a gain of 10 to 11 dB between the frequency range of 3 to 10 GHz. The SpectreS simulator was used to simulate the gain versus frequency chart. This design gives good gain over the entire UWB frequency range because selection of the topology and the sizes of the components were correct. In the inductor source degeneration topology (which is used in the design) the inductor is connected between the source of M_1 and ground provides the negative feedback. This negative feedback is essential to stabilize the amplifier for the entire frequency range. The phase margin for the design is approximately 40 degrees.

A two-port network is essential in RF design simulations. For the rest of the simulations a two-port network design was used, the model of which is shown in Figure 3.9. Port 1 is the input port and Port 2 is the output port.

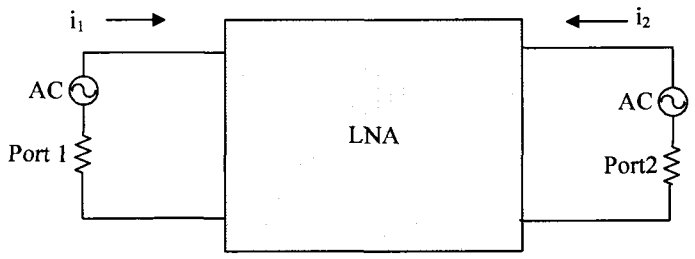


Figure 3.9: LNA schematic with ports

3.3.2 Noise figure simulation

The noise figure is defined by amount of noise contributed by the circuit. For any LNA design it is ideal to have our noise figure as low as possible. As mentioned in the abstract, the targeted noise figure for this project was 4 dB and the design gives us a noise figure of less than 4 dB for the entire UWB frequency band which is 3 GHz to 10 GHz. The noise figure was simulated using the SpectreS simulator. An S-parameter simulation window was used to achieve the plot show in Figure 3.10.

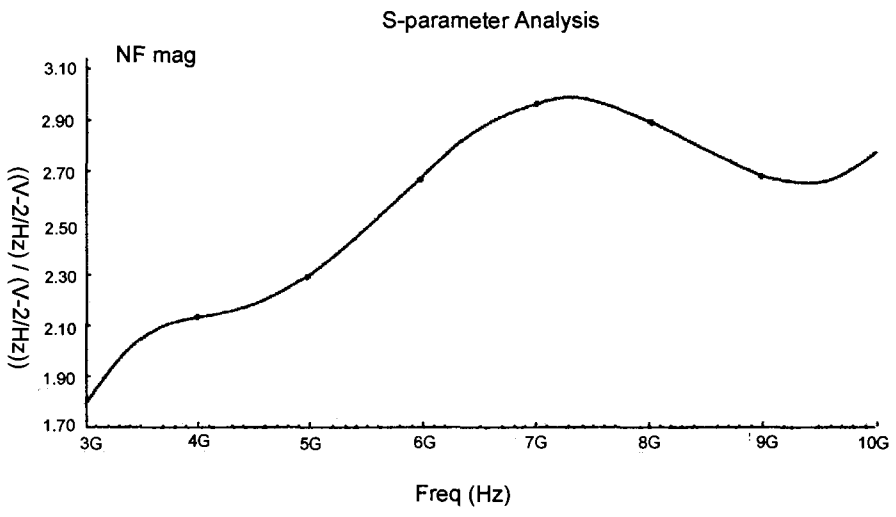
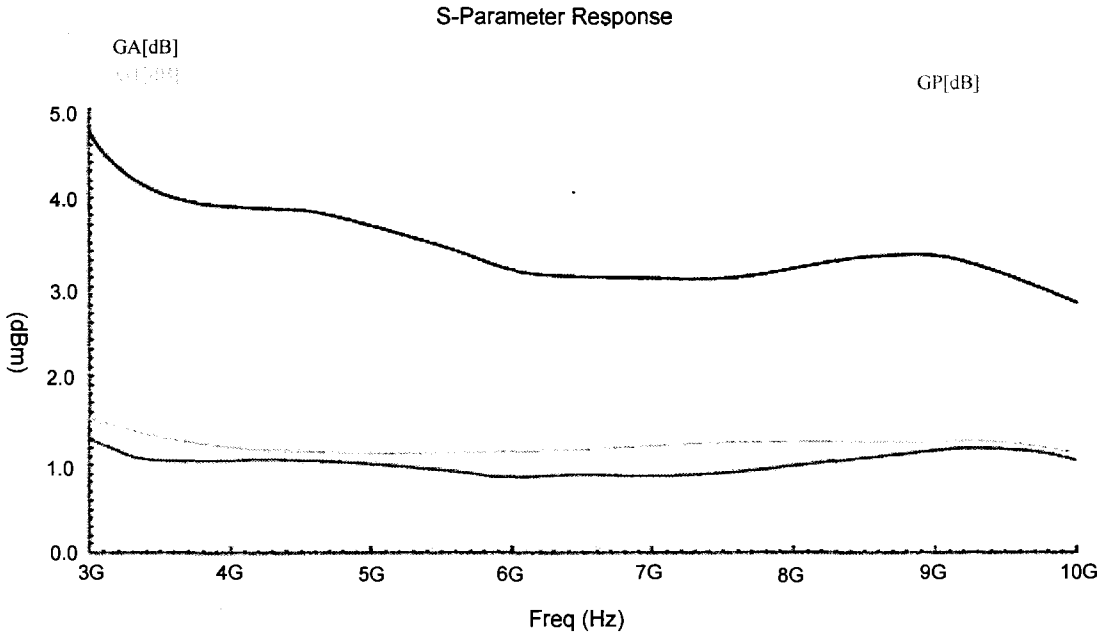


Figure 3.10: Noise figure simulation

3.3.3 GA, GT and GP simulations

GA, GT and GP are different kinds of small signal gain simulations. There were no set criteria as to what these results should be. GA stands for amplification gain, GT stands for transducer gain and GP stands for power gain. Simulation steps similar to the noise figure simulation in Section 3.3.2 were followed for the S-parameter simulations.



3.11: GA, GT and GP simulation

3.3.4 1-dB compression curve

As described in Chapter 2, the 1-dB compression point is a good measure of the linearity of the LNA. The Spectre simulator was used for the 1-dB compression and IIP3 point simulation, unlike the SpectreS simulator for the gain and noise figure simulations. Periodic Steady State (PSS) response was the chosen analysis method. The plot shown in

Figure 3.12 was created using two tones, 8 GHz and 9 GHz. As seen in the Figure 3.12 the 1-dB compression point is -8 dB which is well within the range.

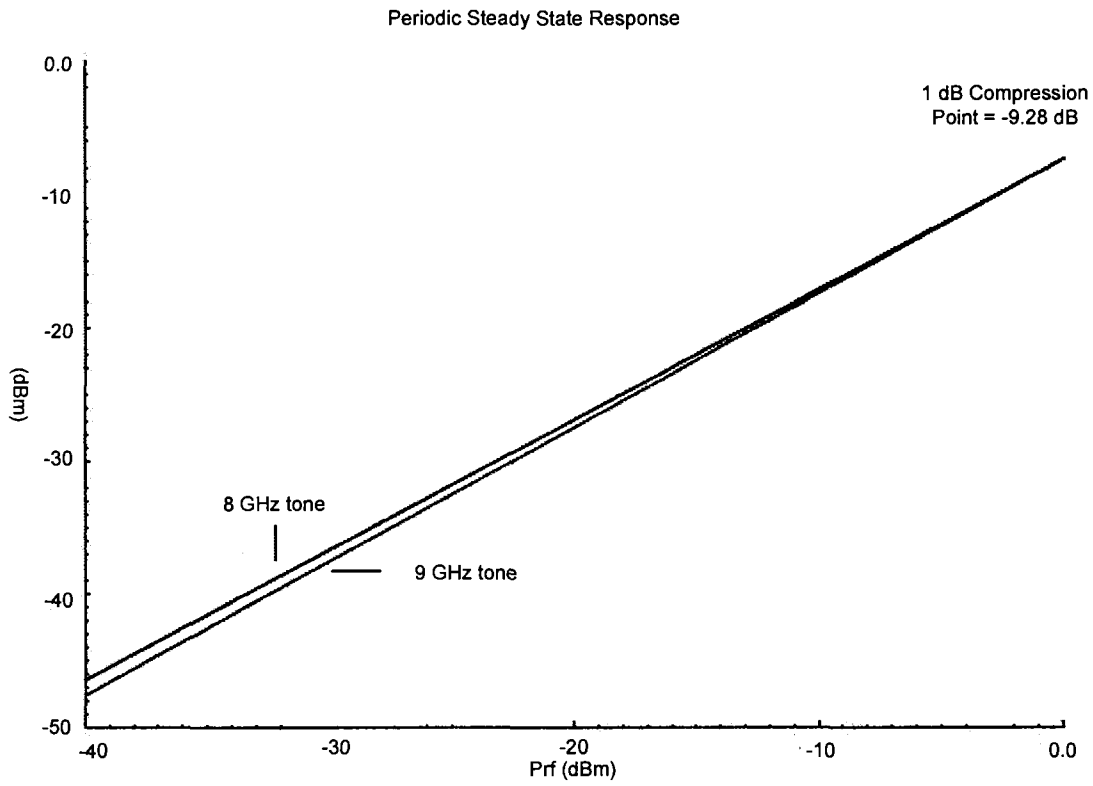


Figure 3.12: 1-dB compression point

3.3.5 IIP3 results

The IIP3 results were used to summarize the LNA linearity with two different frequencies on the RF input. Figure 3.13 shows one such result. The two different frequencies are 8 GHz and 9 GHz. Because of the LNA non-linearity, the 3rd order and the 1st order harmonics of 8 GHz and 9 GHz, respectively, were produced at the output of the LNA.

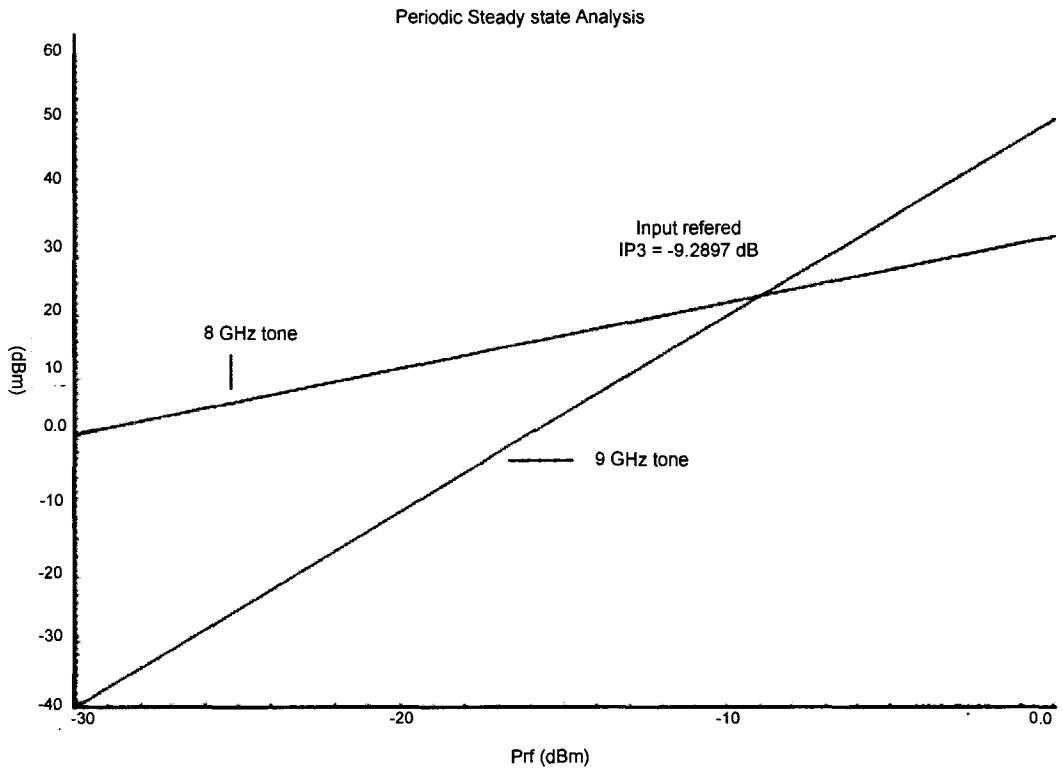


Figure 3.13: IIP3 simulations

Table 3.3 tabulates the comparison between target and achieved results.

Table 3.3: Comparison between targeted and achieved results

	Targeted	Achieved
Gain	>8 dB	10 – 11 dB
S_{11} Input Matching	<-5 dB	<-5 dB
Bandwidth	3-10 GHz	3-10 GHz
Noise figure	<5 dB	3 –5 dB
IIP3	-12 dB	-10 dB
Power dissipation	< 20 mW	15.4 mW

It is evident from the Table 3.3 that most of the parameters were achieved as predicted in Chapter 1. There is always a trade off amongst gain, noise and linearity in RF circuits, and that is why the IIP3 is 2 dB off of the targeted value. The 1-dB compression point and the IIP3 test were conducted at 8 GHz with a beat frequency of 1 GHz.

3.4 On-chip inductor using ADS

This section discusses the design and the analysis of on-chip spiral inductors. The on-chip inductors have a significant effect in the design of the radio frequency integrated circuits (RFICs), which can be modified to enhance the bandwidth of the system. This section describes the design and optimization of the on-chip inductor.

The Figure 3.14 shows the spiral inductor-Π model. In this model, L defines the nominal inductance, and R_s defines the series resistance. The sheet resistance of the metal layer can be used only for calculating the DC resistance of the spiral. The resistance of the spiral increases at higher frequencies because of the skin effect and the Eddy current effect. The skin effect is caused by the greater current flow near the surface of the inductor than at its core. The Eddy current is caused by the induced current flow into the lossy substrate. The series capacitance (C_s) results from the spacing capacitor between the two inductor turns as well as from the capacitance between the spiral and the metal under-pass. The oxide capacitance C_{ox1} and C_{ox2} presents the parasitic capacitor between the substrate and inductor. The substrate resistance (R_{si}) and capacitance (C_{si}) of the silicon are shown in the inductor-Π model.

Ideally, the adjacent turns are almost equipotential, so the effect of the interterm fringing capacitance is neglected. However, there is a relatively large potential difference between the spiral and the center-tap under-pass allowing this type of overlap capacitor to be considered for use.

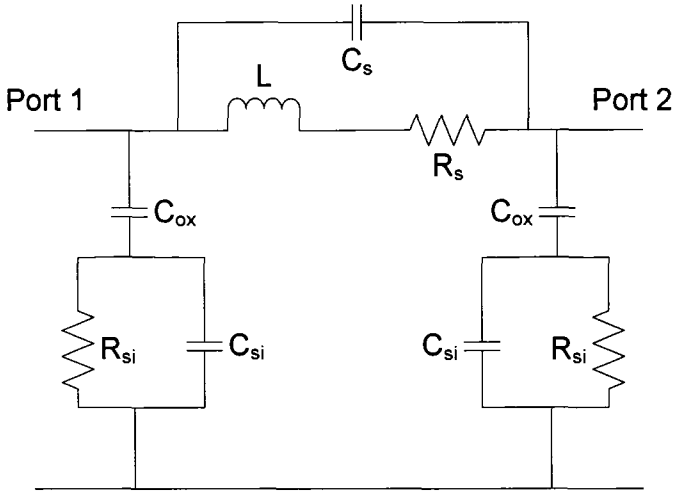


Figure 3.14: The spiral inductor-Π model

The performance of an inductor is known as the Quality factor (Q), which is expressed as:

$$Q = 2\pi * \frac{\text{Engergy Stored}}{\text{Energy Loss in one Oscillation Cycle}} \tag{3.7}$$

where the energy stored is the difference between the peak magnetic energy $E_{peak\ (magnetic)}$ and the peak electric energy $E_{peak\ (electric)}$ stored in any parasitic capacitance. At higher frequencies, the energy dissipation occurs in the silicon substrate, which degrades the inductor quality factor. As the inductor requires significant space on the chip, it is susceptible to collecting and transmitting noise. Therefore, decoupling the inductor from the substrate can improve the overall performance, improve the quality factor, enhance

isolation, and simplify modeling. The spiral inductor-Π model schematic and layout were done in the Advanced Design Systems (ADS) tool as shown in the Figures 3.15 and 3.16, respectively.

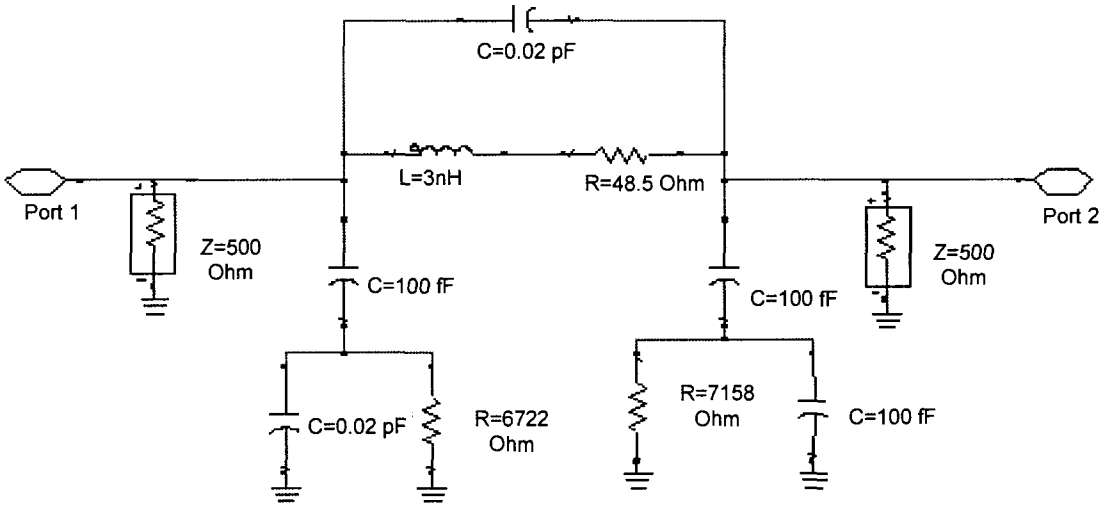


Figure 3.15: Pi-model generated in ADS

The substrate material used for the layout and the layer, which is being used to fabricate the inductor, will determine the actual value of the inductor. Table 3.4 shows parameters of the substrate that are used for the inductor layout in ADS.

Table 3.4: Substrate information of the inductor

Layer	Metal layer	Silicon Dioxide	Silicon
Thickness (μm)	0.5	7	400
Permittivity (Er)	-	3.8	0
Conductivity (Siemens/m)	$2.8E^{07}$	0	10

Figure 3.16 shows the on-chip inductor used in the design. A metal layer is chosen and it is laid out in a spiral fashion [9]. Any polygon shape can be used for the design. A simple square design is chosen for all the layouts. Table 3.5 shows the dimensions of all the inductors used in the LNA design.

Table 3.5: Inductor dimensions

Value	# of turns	Turn spacing	Turn width	Outer diameter
1 nH	3.5	1 μm	2 μm	50 μm
2 nH	3.5	2 μm	4 μm	100 μm
1.6 nH	3.5	2 μm	2 μm	71 μm
1.3 nH	4	2 μm	2 μm	60 μm
1.4 nH	3.5	3 μm	2 μm	72 μm

Figure 3.16 is an image of a inductor of 1.6 nH.

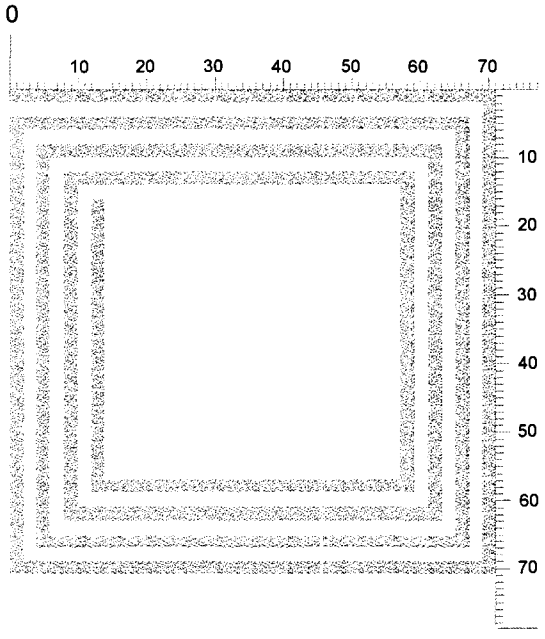


Figure 3.16: Inductor of 1.6 nH

The goal here was to simulate the inductor for its S-parameters and use those results to generate the pi-model for every inductor in the design [10]. Figure 3.17 shows the S-parameter result for the inductor in Figure 3.16.

The S-parameter result can be used to generate the pi-model using the "Spice Model Generator" feature in the ADS tool. After opening the "Spice Model Generator", it was necessary to browse the S-parameter result file and specify the name of the result file. The result is a text file which looks like a table mentioning the values of the resistors, capacitors and inductors of the pi-model.

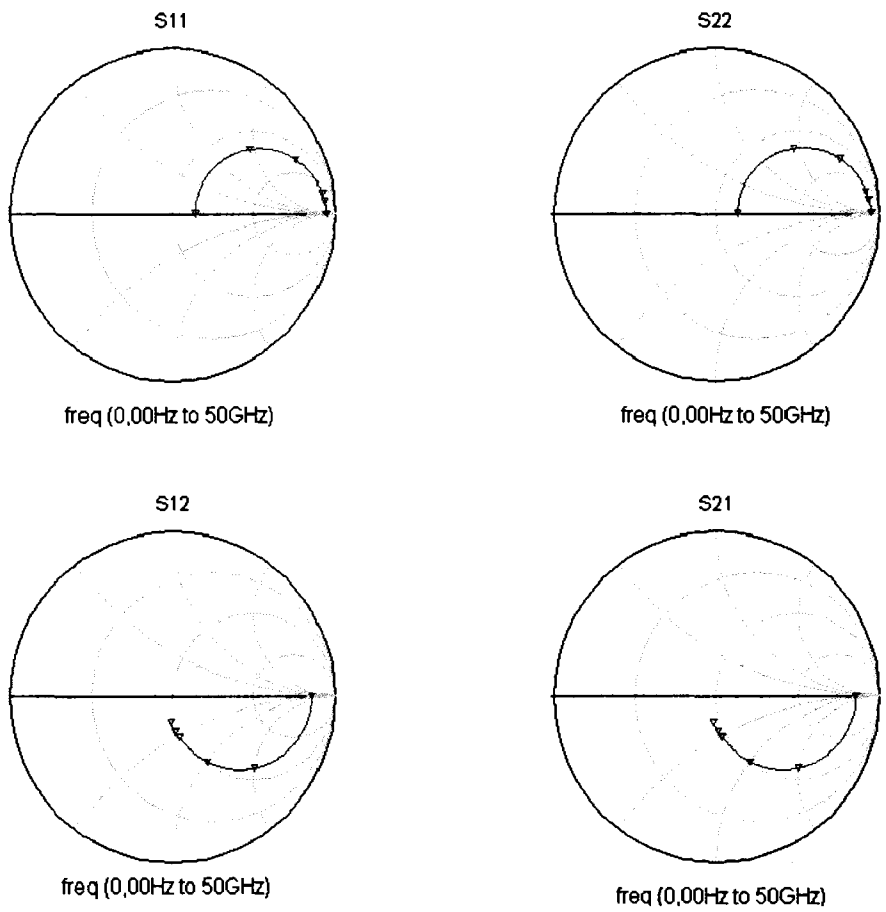


Figure 3.17: S-parameter results for the spiral inductor

Next, the S-parameter results in Figure 3.17 were converted into the Z-parameters in order to get the Q analysis of the inductor. Figure 3.18 shows the equations that assisted in creating the Z-parameter.

```
Eqn zin7=1-S(2,2)
Eqn zin3=1-S(2,2)        Eqn zin5=1+S(2,2)
Eqn zin2=1+S(1,1)        Eqn zin6=1-S(1,1)
Eqn Z_11=50*(zin11_num/zin_den)      Eqn zin11_num=(zin2*zin3)+(S(1,2)*S(2,1))
Eqn Z_22=50*(zin22_num/zin_den)      Eqn zin22_num=(zin6*zin5)+(S(1,2)*S(2,1))
Eqn Z_12=50*(2*S(1,2)/zin_den)       Eqn zin_den=(zin7*zin6)-(S(1,2)*S(2,1))
Eqn Z_21=50*(2*S(2,1)/zin_den)
Eqn Zin=Z_11-((Z_12*Z_21)/Z_22)
```

Figure 3.18: Generation of the Z-parameters in ADS

The actual values of L, r and Q can be obtained from the Z-parameters. Figure 3.19 shows the simulated values of L, r and Q for the inductor over the frequency from 0 to 50 GHz.

Table 3.6 shows a comparison between the simulated results before and after inserting the pi-model. It was observed that there was slight degradation in the gain and noise figure of the design. All the inductors were optimized for the area [11]. All the parasitic parameters, which were not considered in the simulation without the pi-model, come into affect when the pi-model was included in the LNA design. The insertion of extra parasitics caused degradation in the gain and noise figure.

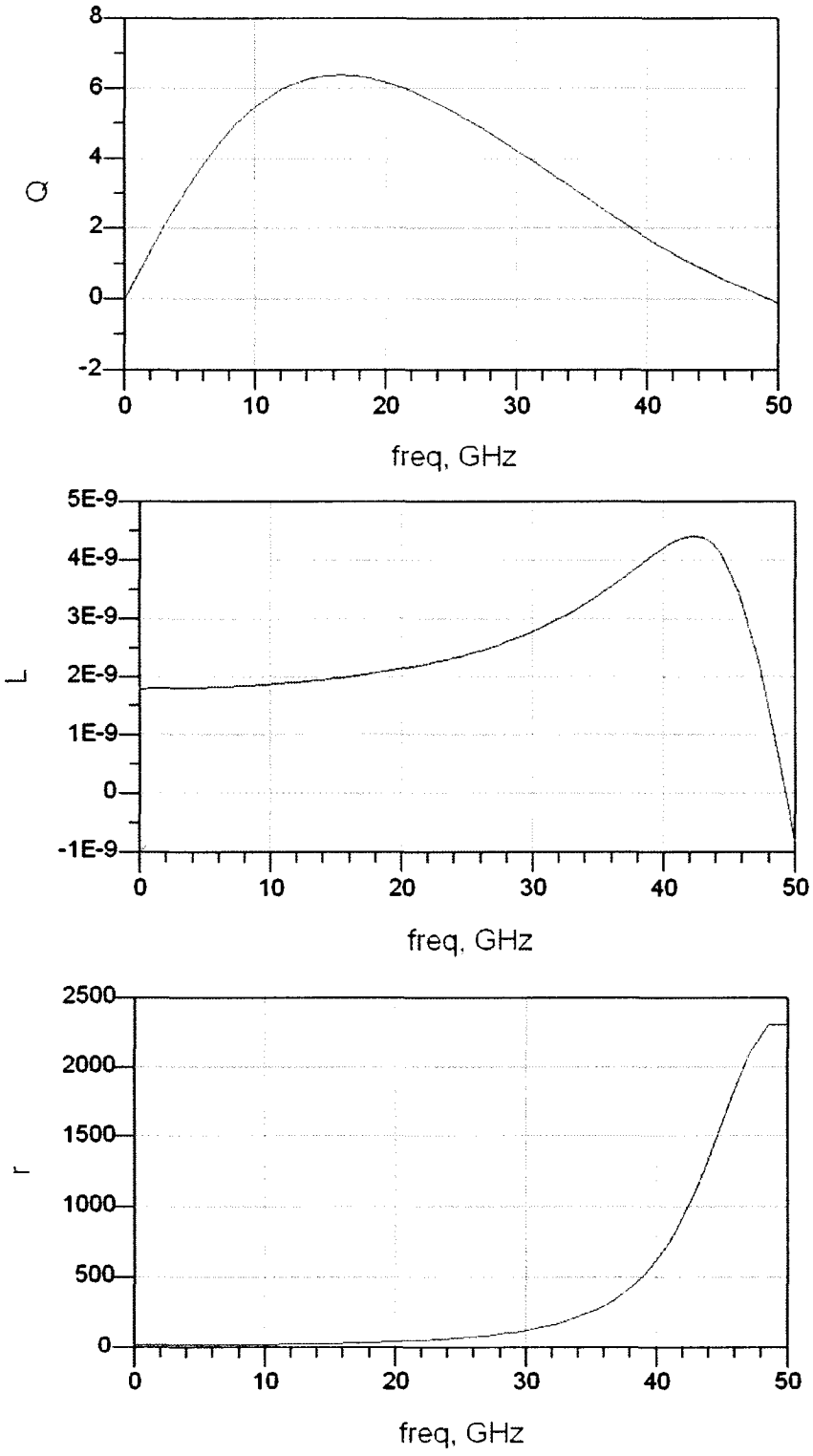


Figure 3.19: Simulated values of Q, L and r from Z-parameter

Table 3.6: Comparison of results before and after inserting pi-models for inductors

	Schematic with inductors	Schematic with pi-models
Gain	10 – 11 dB	7 dB
S_{11} Input Matching	<-5 dB	< -6 dB
Bandwidth	3-10 dB	3-10 dB
Noise figure	3-5 dB	5-7 dB
IIP3	-10 dB	-9 dB
1-dB compression point	-8 dB	-8 dB

3.5 Final layout and extraction

The layout of the entire schematic was done using Cadence's Virtuoso tool. TSMC 0.18μ technology has been used to design and implement the transistor level design. The minimum channel length for this technology is 0.18μm. Apart from the inductor (which was discussed in the previous section), the schematic has 3 capacitors and one resistor. A rectangle of poly layer was used to fabricate the resistor. The poly layer makes a good resistor because of its high resistance and low parasitics. Rectangles of the metal 1 and 2 layers were used to create capacitors of various values. Resistor IDs and capacitor IDs were added to the resistors and capacitors to let the tool treat them as a resistors and capacitors and not just any metal layer.

Figures 3.20 and 3.21 show the layout of the design and give an overall idea of how the different components have been arranged in the layout. A Design Rule Check

(DRC) and a Layout Versus Schematic (LVS) comparison were performed on the layout. The DRC checks for potential errors in the layout. The LVS checks the layout against the schematic and verifies that all the nets are matching.

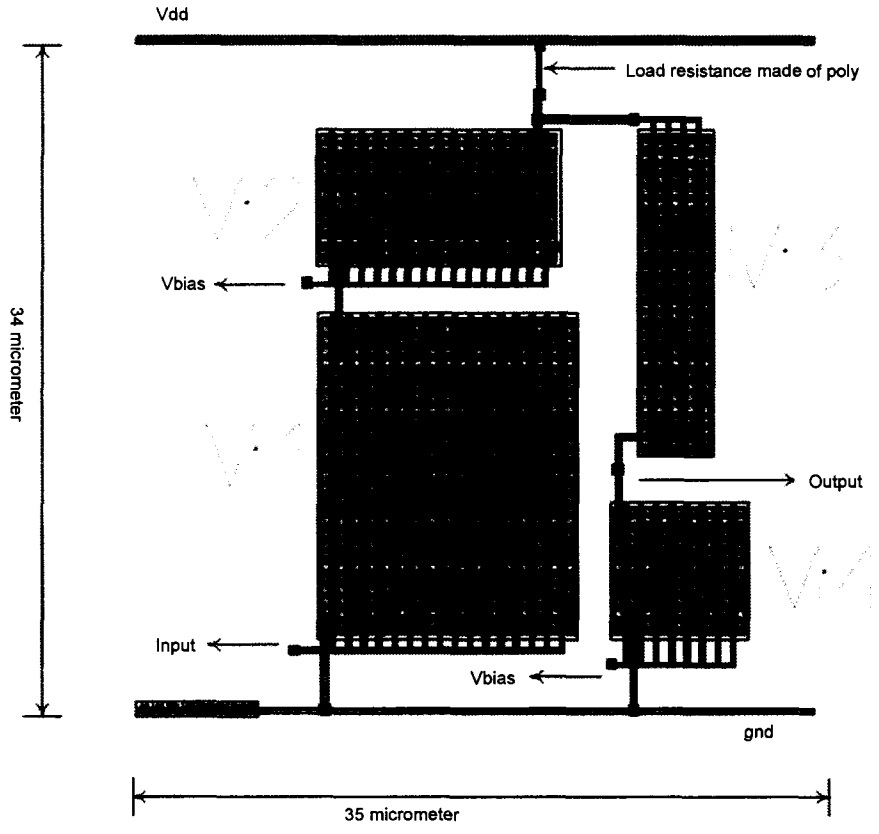


Figure 3.20: Layout without capacitors and inductors

After the DRC and LVS were completed successfully, layout extraction was done. The extraction gives an overall idea about the parasitics of the design. Since the metal layers 1 and 2 have been used, the design has quite a few parasitics. Special care has been taken to implement them into the design.

Finally, post layout simulations were carried out to check the functionality of the design. Table 3.7 shows a comparison between the simulated and extracted results.

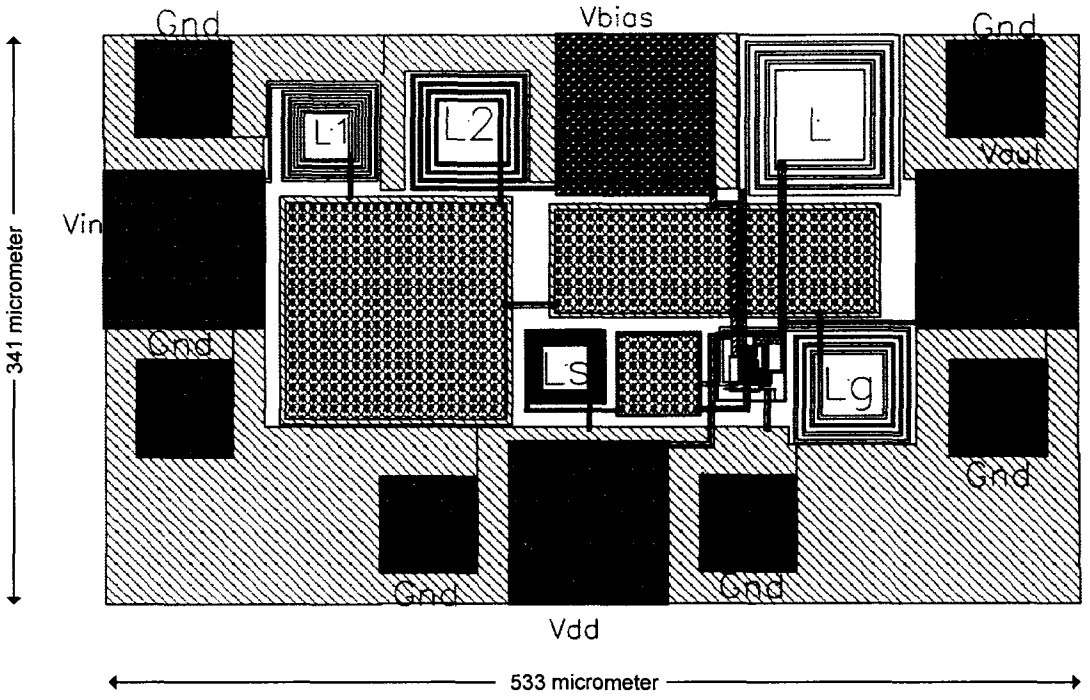


Figure 3.21: Final layout

Table 3.7: Comparison between schematic and extracted simulations

	Schematic simulation	Extracted simulation
Gain	10 – 11 dB	7 dB
S_{11} Input Matching	<-5 dB	< -6 dB
Bandwidth	3-10 dB	3-10 dB
Noise figure	3-5 dB	4-6 dB
IIP3	-10 dB	-9 dB
1-dB-compression point	-8 dB	-9 dB

The extracted results show little degradation in the gain and noise figure because the design has large capacitors in it. Better matching of the capacitors would have given results closer to the schematic results.

In summary, it could be said that a successful and functionally working LNA has been designed for UWB application. Although there is some degradation in the result parameters after extraction, the design still meets the specifications and is ready to be tapped out. Table 3.8 presents a comparison of this work to other works in similar areas. If one compares this thesis to other works presented in Table 3.8 one understands that the proposed design has a significantly lower noise figure than other works.

Table 3.8: Summary of comparison of this work with past works in LNA

	Technology	S_{11} dB	G_{max} dB	B GHz	NF_{min} dB	IIP_3 dBm	P_{diss} mW
This Work	0.18μ CMOS	<-5	11	3 – 10	3	-10	15.4
[12]	0.18μ CMOS	<-9.9	10.4	2.4 – 9.5	4.2	-8.8	9
[13]	0.18μ CMOS	<-8	8.1	0.6-22	4.3	N/A	52
[14]	0.6μ CMOS	<-7	7.4	0.5 – 4	5.4	N/A	83
[15]	0.6μ CMOS	<-6	6	1.5 –7.5	8.7	N/A	216
[16]	0.25μ CMOS	<-8	13	0 – 1.6	3.9	N/A	35

Chapter 4 Conclusion

The primary objective of the thesis was to design a Low Noise Amplifier (LNA) that could be used for UWB applications. It was intended to have the LNA be capable of providing enough gain within the frequency range 3 to 10 GHz with minimal noise.

In Chapter 1, various aspects of the UWB standard were studied. Chapter 2 explains LNA characterization along with presenting in-depth analysis of LNA gain, noise, sensitivity, and linearity. Chapter 3 describes various useful and popular LNA topologies. This chapter also gives good understanding of the proposed design, schematic of the design, and simulated results. Chapter 3 also describes pi-model generation of the inductor and illustrates the layout of the design.

The TSMC 0.18μ CMOS technology was used for the project. The LNA is different from the conventional LNAs because it has a high pass band of 7.5 GHz. The proposed design has a gain of 10 dB from 3 to 10 GHz after which it starts decreasing. The target noise figure was less than 4 dB and simulations show that the proposed architecture has succeeded in achieving that. The noise figure is well below 3 dB for the entire frequency range.

Apart from those basic tests, the linearity of the design has been checked by using the 1-dB compression point and IIP3 tests. The design has a -8 dB of 1-dB compression point and -9dB of IIP3. The power supply voltage of TSMC 0.18μ technology is 1.8V, which plays a significant role in the generation of a design with low power dissipation. Power dissipation for the proposed design is 15.4 watts.

The primary goal of any LNA is high gain with very low noise. Use of the ADS generated pi-model is one of the reasons that the proposed design has such a low noise figure. In comparing the schematic and extracted simulations, the input matching parameter S_{11} is slightly different in the proposed design. Better matching of capacitors in the input matching network could provide better S_{11}.

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