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PARTITION NOISE EXTRACTION USING TCAD SIMULATIONS

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Carol Cui Lan Lin

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The Designated Thesis Committee Approves the Thesis Titled

PARTITION NOISE EXTRACTION USING TCAD SIMULATIONS

by

Carol Cui Lan Lin

APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

SAN JOSÉ STATE UNIVERSITY

August 2010

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ABSTRACT

PARTITION NOISE EXTRACTION USING TCAD SIMULATIONS

by Carol Cui Lan Lin

As Complementary Metal Oxide Semiconductor (CMOS) technology scales down, partition noise may start to play a bigger role in reducing the signal-to-noise ratio (SNR) in sample-and-hold circuits and other capacitive sensing circuits that reset the voltage across a capacitor. Previous studies on partition noise lack a reliable and accurate measurement method to quantify partition noise. In our study, we have developed a method using Technology Computer Aided Design (TCAD) simulations to estimate partition noise. Through simulation, we determined the transistor dimensions and sense capacitance required to measure partition noise. Furthermore, we designed a test circuit based on our simulation results with the flexibility to study partition noise. The test circuit has a buffer that allows us to measure partition noise without interference from test measurement equipments. Finally, we presented a method to measure and extract partition noise using our test circuit.

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CHAPTER ONE: INTRODUCTION

1.1 Statement of the Problem

One of the major obstacles of designing analog and mixed-signals circuits is in maintaining signal integrity by reducing noise. Noise in analog and mixed-signal circuits can degrade signals and cause issues in aspects such as accuracy and performance. Consumer electronics such as digital cameras and personal music devices use mixed signal circuits to convert analog signals such as light and sound into digital signals as bits. Any type of noise that distorts the signal will limit the performances of these devices. For example, noise introduced to a signal in an active pixel sensor will reduce the signal to noise ratio (SNR). These problems are more apparent now as technology scales down. As we scale down the technology, we must lower the power supply level, which in turn reduces the dynamic range of the signal stored and results in a lower SNR.

In particular, reset noise is a major problem in modern analog and mixed signal circuits. For example, sample-and-hold circuits use a transistor as a switch to set a voltage across a capacitor. Therefore, reducing reset noise directly affects these types of circuits. Specific circuits that are especially limited by reset noise are sample-and-hold circuits, CMOS active pixel sensors (APS), switch capacitor circuits, and analog to digital converters (ADC), to name a few, require setting a signal of a capacitor. Ideally, when a capacitor (charge storage device) is reset to a specific voltage, the voltage across the capacitor should be the same each time. However, because of the random distribution of charge under the reset transistor gate, that is not the case. Instead, it causes random variation of the voltage across the capacitor. For circuits such as APS, which is found

commonly in digital cameras, variation in the charge transferred to the sense node causes fixed pattern noise, which translates to poor picture quality output.

1.2 Objectives

In this work, we studied partition noise of a reset transistor. Due to the nature of partition noise's small quantity, it is very difficult to distinguish partition noise from other noise sources. Therefore, we attempted to measure partition noise by designing a circuit to amplify the partition noise such that it is a measurable quantity through technology computer aided design (TCAD) simulations. We designed a circuit and a method to extract partition noise.

1.3 Research Question

Partition noise is relatively small compared to the Johnson noise theory of modeling reset noise of a series RC circuit. What are the design and test setup requirements to study and extract partition noise in a short channel N-channel Metal Oxide Semiconductor (NMOS)?

1.4 Research Significance

In order to reduce reset noise, we tried to reduce all aspects of reset noise, that is, Johnson thermal noise and partition noise. In general, the only way to reduce reset noise is by increasing the capacitance. However, that is not always an option in technologies such as active pixel sensors where signal to noise ratio is crucial. In this study, we

developed the design requirements to amplify partition noise so that it is a measurable quantity to characterize it further.

1.5 Relevant Definitions/Glossary

Some definitions of terms used in the paper include:

Charge injection: Charge pump from inversion channel to the source or drain as the transistor changes from an on-state (i.e., saturation or linear operating region) to the off-state (i.e., sub-threshold operation region). Charge injection is the resulting voltage difference between the desired reset-voltage to the final voltage across the capacitor to be charged.

Fall-time: The time it takes the transistor gate to switch from on-state to the transistor's threshold voltage.

Partition noise: The variation in charge injection across the sense capacitor upon reset.

Reset noise: The variation in charge across a capacitor from successive charge-up through a non-ideal switch such as a transistor.

Signal to noise ratio (SNR): It is the ratio of signal power to total noise power. It is expressed in decibels.

Thermal noise: Current fluctuation from thermal agitation in a resistive path.

1.6 Methodology

In this study, we used TCAD simulations to estimate the number of residual electrons in the reset transistor channel when transitioning to sub-threshold operation. Based on previous partition noise models, we can estimate the partition noise from the residual

electrons. We simulated a range of transistor lengths and capacitances to determine the length and to sense the capacitance required to generate a measurable amount of partition noise. A second stage source follower is used to isolate the sense capacitance from any load from measurement instruments.

1.7 Scope/Limitations

To simplify the problem at hand, our simulations on TCAD assumed a noiseless system-ideal transistor and voltage source. Our transient simulation of the transistor from the on-state to the off-state assumed a quasi-static operation. Using a typical 0.18um process, the simulation results serve as a rough estimate of the residual charge under the channel at the verge of operating at sub-threshold.

In our partition noise calculations, we assumed the inversion channel is uniform before operating below sub-threshold region. When the transistor is operated in the linear region, the voltage across the drain and source should be zero, given that enough time has passed by to charge up the sense capacitance to the same voltage as the drain. The channel profile is uniform until the gate voltage is below threshold voltage. Therefore, we can safely assume a uniform channel profile in our calculation.

1.8 Overview of Remaining Chapters

In the following chapters, we will discuss previous studies on partition noise, the simulation environment, design architecture, and results. In Chapter Two, we will discuss the relationship of partition noise to reset noise and the derivation of partition noise. In Chapter Three, we will describe our methodology, simulation environment and,

circuit design. In Chapter Four, we will discuss in detail the design of our partition noise test circuit. In Chapter Five, we will discuss our findings and results. In Chapter Six, we provided a method of measuring and extracting partition noise from the partition noise test circuit. In Chapter Seven, we will discuss our conclusions and future work.

CHAPTER TWO: OVERVIEW OF PARTITION NOISE

2.1 Introduction

In this section, we discuss reset noise derivation based on Nyquist Theory of Johnson Noise and the derivation of partition noise. We present the most recent studies on partitioning noise, and reset noise reduction techniques. Finally, we will summarize partition noise derivation using basic statistics.

2.2 Overview of Noise

An extensive amount of research on reducing reset noise exists. Most literature on reset noise characterizes the dependence on capacitance and focuses on circuit design solutions that use negative feedback to reduce reset noise such as capacitive control, bandwidth control, and charge control method [1]. Correlated double sampling is another technique used to reduce reset noise with an added improvement of reducing 1/f noise and charge injection error [2]. However, the study on Charged Coupled Devices (CCD) reset noise by Carnes and Kosonoscky [3] shows that reset noise also depend on the reset transistor's channel length that was later proven by Teranishi and Mutoh [4]. This aspect of reset noise is known as partition noise.

Traditionally, reset noise is derived using Johnson Noise Theory that attributes to a thermal noise source. The reset noise in a series resistor and capacitor (RC) circuit is due to the thermal noise from the resistor. By treating the resistor and capacitor as impedance as shown in Figure 1, the RC circuit looks similar to a resistive divider. Equations 1 to 5 show the derivation for reset noise of a RC circuit.

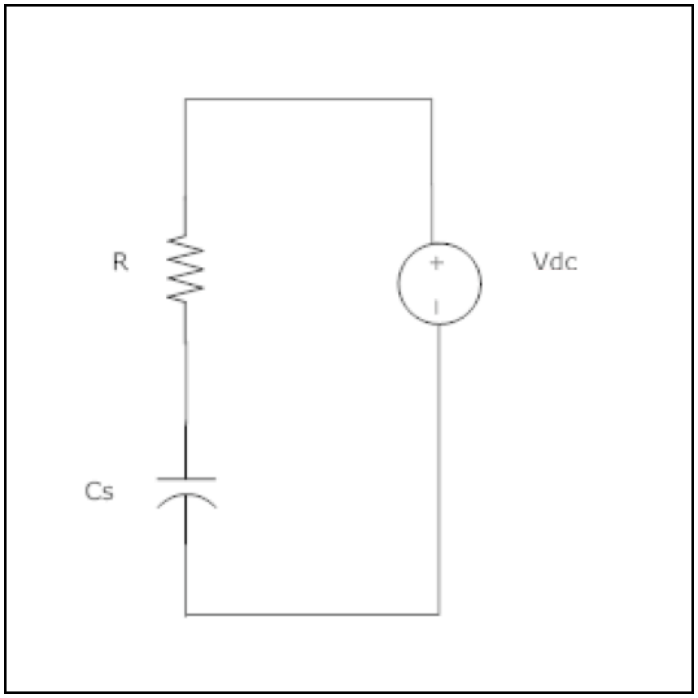

Figure 1-Capacitive reset circuit.

$$V_{onoise}^{2}(f) = \sqrt{4kTR}\,\frac{\frac{1}{jwC}}{\frac{1}{jwC}+R} = \frac{\sqrt{4kTR}}{1+j\frac{f}{f_{3dB}}} \tag{1}$$

$$V_{onoise}^{2}(f) = \frac{4kTR}{\left|1+j\frac{f}{f_{3dB}}\right|} = \frac{4kTR}{1+\left(\frac{f}{f_{3dB}}\right)^{2}} \tag{2}$$

Since thermal noise is a white noise, the noise equivalent bandwidth (NEB) is

$$NEB = f_{3dB}\frac{\pi}{2} \tag{3}$$

So that the spectral density root mean square can be re-written as

$$V_{onoise,RMS} = \sqrt{f_{3dB}\frac{\pi}{2}}\sqrt{V_{onoise}^2} = \sqrt{\frac{1}{2\pi RC}\frac{\pi}{2}4kTR} \ , \ f_{3dB} = \frac{1}{2\pi RC} \tag{4}$$

$$V_{onoise,RMS} = \sqrt{\frac{kT}{C}} \tag{5}$$

The resulting reset noise is a function of capacitance [5]. When the reset circuit MOSFET is used as an on-off switch, the inversion channel acts as the resistor in a series RC circuit. That means the Johnson Noise Theory Derivation of Reset Noise does not take into account the transistor size in its calculation. However, empirical data by Kosonoscky [4] shows the reset noise increases with transistor length, and the term partition noise was coined to represent this unknown noise source.

An explanation of the transistor length affecting reset noise was not given until Nobukazu Teranishi and Nobuhiko Mutoh [6] performed a study on charge-coupled detector (CCD) reset noise. In their study, they discovered another noise source on top of the reset noise due to thermal noise of the resistive inversion channel. This noise source is from the variation in charge injection as the transistor changes from the on-state to the off-state, specifically, from the linear region to sub-threshold, and partition noise is the variation in charge injection. Their study provided a derivation of partition noise by modeling the charge injection as a binomial distribution with a uniform inversion channel charge profile. In doing so, the resulting partition noise is a function of channel length, and the total reset noise is the sum of both the reset noise derived from the Johnson Noise Theory and the partition noise.

Since Teranishi and Mutoh's study, only one other study on partition noise has surfaced. The study by Lai et al. [6] found that the transition rate of the MOSFET's

switch from on to off state also affects partition noise. At a faster transition rate, the residual charger in the inversion channel is larger than that of a slower transition rate because of the charge profile. Teranishi and Mutoh [4] used a uniform and a sinusoidal charge profile to calculate the expected residual charge. Lai showed that by accurately modeling the channel charge profile, we would have a more accurate residual charge. With Teranishi and Mutoh's derivation of partition noise, they showed the expected partition noise is within 10% of the measured values.

In the following sub-section, we will explore the derivation of partition noise theory.

2.3 Partitioning Noise

Partition noise is caused by the variation in charge distribution from the inversion channel when a transistor is used as a switch to charge up a capacitor. The way the charge distributes depends on the electron transport mechanism, and the two mechanisms of carrier transport are drift and diffusion. When the transistor turns off and the gate voltage is above the threshold voltage, carrier movement is mainly caused by self-induced drift. Below the threshold voltage, diffusion is the dominant carrier transport mechanism.

To illustrate, Figure 2 shows how the channel profile changes as the reset transistor changes from the on-state to off-state. The resulting charge will either settle to the source, drain, or recombine with the substrate. To simplify the model, we neglected the channel charge recombination with substrate in our study. This is a valid assumption

when the fall-time is much slower than the carrier transit time [7]. With this assumption, we used probability theory to derive the expected partition noise.

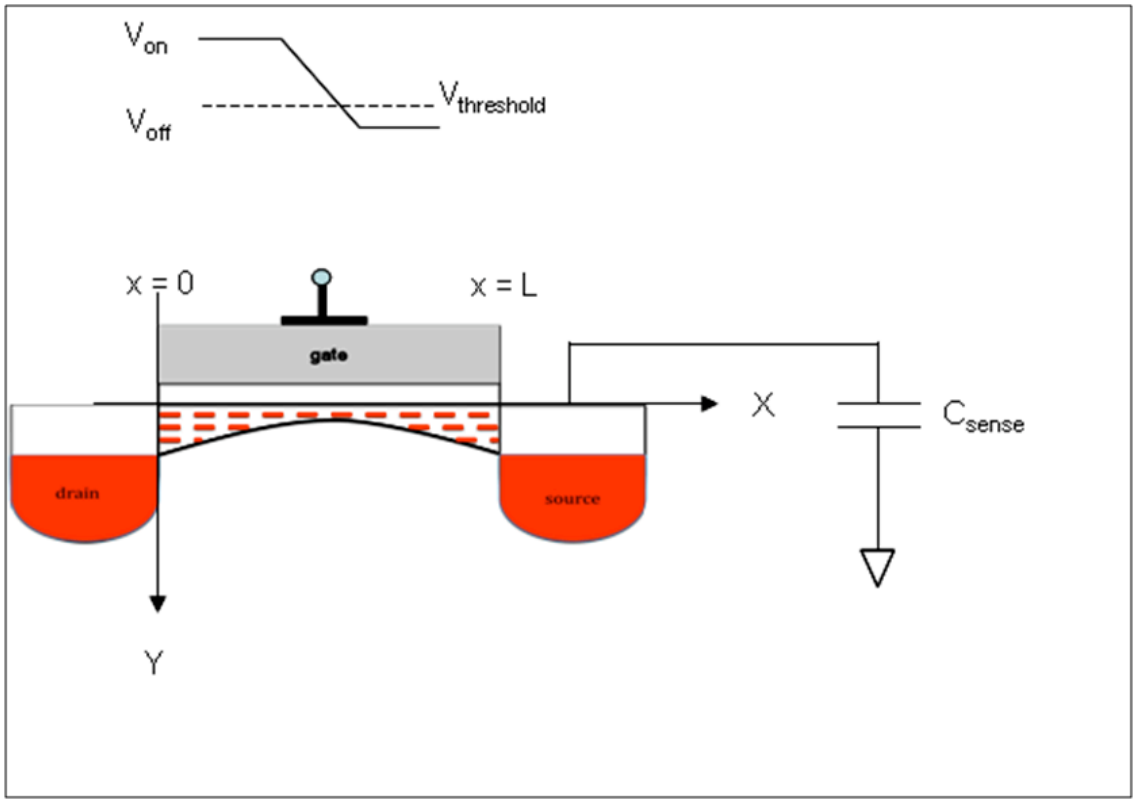

Figure 2-Channel profile changes as the reset transistor changes from on-state to off-state.

From the probability theory, carrier distribution can be modeled as a binomial process in which the event of a carrier settling to the capacitor has probability

$$P_{source}(x) = \frac{x}{L} \tag{6}$$

and settling to the drain has probability

$$P_{drain}(x) = 1 - \frac{x}{L} \tag{7}$$

then the event of carrier distribution is a binomial random variable. Partition noise can be modeled as the variance of the binomial random variable, x, the event of carrier distribution. The amount of charge transferred to the capacitor, then, is the product of the probability of charge moving to the capacitor, the probability of not moving to the capacitor, and the total number of carriers in the channel when dominant mechanism for electron transport switches from drift to diffusion. Since the number of carriers can be obtained by integrating the carrier profile in the channel over length of the channel, partition noise is proportional to the channel length. The partition noise voltage can be represented by Equation 8

$$\overline{V_n^2} = W \int_0^L n(x) P_{drain}(x) P_{source}(x) dx \tag{8}$$

where W is width, L is length, $n(x)$ is the charge profile of one unit area, $p_{source}(x)$ is the probability of charge moving to the capacitor, and $p_{drain}(x)$ is the probability of charge moving to the source [8]. $p_{source}(x)$ is a function of the electron's distance from the capacitor. Since the total probability should equal to 1, $p_{drain}(x)$ is the difference of 1-$p_{source}(x)$.

Assuming that the channel is uniform, and diffusion is the only mechanism that contributes to partition noise, partition noise can be expressed as a function of the transistor dimensions and the initial charge density, n_0 [8]

$$\overline{V_{pn}^2} = \frac{1}{6} W L n_0 \tag{9}$$

$\overline{V_{pn}^2}$ is our partition noise voltage, while W and L are the width and length of the transistor. The accuracy of this model depends on a realistic charge profile, and hence a better estimate of the total charge in the inversion layer.

Modeling partition noise as a binomial distribution has been shown to match empirical data. The accuracy of this model depends on the initial calculation of channel charge. The more accurate model of the inversion channel profile, the more accurate the model is in determining partition noise.

Previous studies have also shown that partition noise is sensitive to the operating frequency and transistor size. Furthermore, operating at higher frequencies and larger transistor lengths have shown to increase partition noise. This can be explained by diffusion as the dominant mechanism for charge movement in sub-threshold operation. Diffusion is gradient-based, so that the ratio of capacitance on the source and drain node will affect $p_{source}(x)$ and $p_{drain}(x)$ as well. In addition, the initial residual inversion channel charge will affect the resulting partition noise added to the sense capacitor. Hence, for faster transition rate from linear to sub-threshold operation, the residual inversion channel charge is larger, and thus, a larger partition noise.

2.4 Summary

In this section, we have shown that there are two contributing noise sources to reset noise: thermal noise from the inversion channel and partition noise from residual inversion channel charge when the reset transistor is operated in sub-threshold. A majority of reset noise is due to thermal noise. Partition noise is minuscule compared to

the thermal noise component of reset noise, but it takes into account the reset transistor length's effects on reset noise.

CHAPTER THREE: SIMULATION

3.1 Introduction

In this section, we provide details on our TCAD simulations. Our simulations of the active reset circuit in Figure 2 will determine both the size of the capacitor and the transistor. Our simulations provide an estimate on the number of electrons in the inversion channel for different transistor lengths. Simulation results are used to design the reset transistor and sense capacitor size and test setup requirements.

Based on previous studies in [4][6], a linear increase in residual electrons in the inversion channel is expected with increasing transistor length while the width is held constant. In general, we can assume that the channel is uniform when the MOSFET is operating in the linear region. Thus, scaling the transistor length is the same as scaling the gate area when the width stays the same. Based on [6], we can also expect partition noise to scale linearly with transistor length. We neglect varying the transistor width to maintain the same overlap capacitance between gate to source and drain.

Although TCAD can simulate noise, it is limited to flicker noise, shot noise, thermal noise, and reset noise. These noise sources have been studied in-depth and well modeled in most circuit simulators. However, partition noise has yet to be significant source of noise, and no known circuit simulators that have incorporated its affect. Our TCAD simulations assume all voltage sources are ideal and noiseless to simplify results, which are only used as an approximation.

3.2 Simulation Setup

Simulation is performed on Synopsis TCAD. A NMOS is designed with a typical 0.18 µm process. From the TCAD device simulator, we can generate the current and voltage characteristics that will be used to extract the transistor's threshold voltage and the total number of charge in the channel when the device is operating at the threshold voltage. Our goal is to extract the total channel charge that will contribute to partition noise.

3.3 MOSFET Fabrication Process

In the process of fabricating our NMOS with a threshold voltage of 550 mV, we used a typical 0.18 µm CMOS process flow. We will begin with the formation of the P-well, followed by the gate oxide and the poly gate.

First, we define the p-well for an N-channel MOSFET by doping the silicon bulk with boron at $10^{16}/cm^3$ concentration. Next, a 50 Å of silicon oxide (SiOx2) layer is deposited on top of the bulk through thermal oxidation at 1000°C for 90 minutes. Orientation is <100>. The poly gate is deposited with a thickness of 210 nm. A 70 Å of poly oxidation is deposited for 8 minutes at 900°C to smooth out the poly gate surface. Then, a 10^{14} dose of arsenic is implanted in the source drain at 15 keV and annealed at 1000°C as Lightly Doped Drain (LDD). The Shallow Trench Isolation (STI) is created with 400 Å of Nitride and etched. The Source and Drain are created with 10^{15} dose of Arsenic at 25 keV. This is followed by a 10 second anneal at 1000°C follows. Finally, 30 nm of Aluminum is deposited for the contacts.

3.4 Extract NMOS Threshold Voltage and Channel Charge Density

For our purposes, we must first characterize the voltage and current characteristics of our NMOS. To do so, we extracted the threshold voltage that will allow us to estimate the contribution of electrons to partition noise. The threshold voltage of the MOSFET is extracted by setting the source to drain voltage to 250 mV. The gate is swept from 0 V to 3 V, and the drain to source current is measured. Using a linear extrapolation from the I_d-V_{GS} curve to extract the threshold voltage result in a threshold voltage of 587 mV [9]. A further analysis of the threshold voltage with body effect uses the charge injection voltage results to figure out the correct bias on the source while the drain is held at 1 V. The gate is swept from 0 V to 3 V and the drain current is measured. The resulting threshold voltages will be discussed in Chapter Five.

The electron density in the channel is integrated as the gate of the reset transistor is ramped down from 3.0 V to 0 V. The total electron density will be integrated from the source to drain. We wanted to integrate the total electron density when the gate is at the threshold voltage. In our case, we used the threshold voltage extracted with body effect. Please see appendix for process and simulation files.

3.5 Summary

Partition noise, unlike other noise sources, depends on the initial count of electron charge in the inversion channel when the gate voltage is the same as the threshold voltage. Our simulations on Synopsis TCAD have extracted the threshold voltage and integrated the total channel charge when the reset transistor is operated at the threshold

voltage. This allowed us to calculate the expected partition noise on the sense capacitor for different transistor lengths. With this information, we are able to design the partition noise test circuit and the correct test setup required to measure partition noise.

CHAPTER FOUR: RESEARCH DESIGN

4.1 Introduction

In this section, we discuss the design architecture required to amplify partition noise such that it is large enough for us to measure. Our design will focus on the reset transistor size, sense capacitance, and the test circuit as a whole. The design needs to be flexible enough for us to vary the way we test the circuitry. A source follower is added at the output stage to drive a larger load from the test setup. A combination of transistor size and sense capacitors are used to extract partition noise from total reset noise.

In the following sub-sections, we will go through the need for each design elements; this includes the capacitive reset circuit, the source follower, and the sense capacitor. The design will directly affects how much partition noise will be generated, and the test setup required to measure partition noise accurately.

4.2 Capacitive Reset Circuit

A typical capacitive reset circuit consists of a resistor and a capacitor as shown in Figure 1. The purpose of a reset circuit is to set the voltage across the capacitor. Based on the Nyquist Theory of Johnson Noise [1], thermal noise from the resistor is stored in the capacitor as reset noise.

Active reset circuits use a transistor as a switch as shown in Figure 3. The transistor acts as a switch between the voltage source and the capacitor to set the capacitor voltage.

The resistance in the transistor inversion channel contributes thermal noise to the sense capacitor.

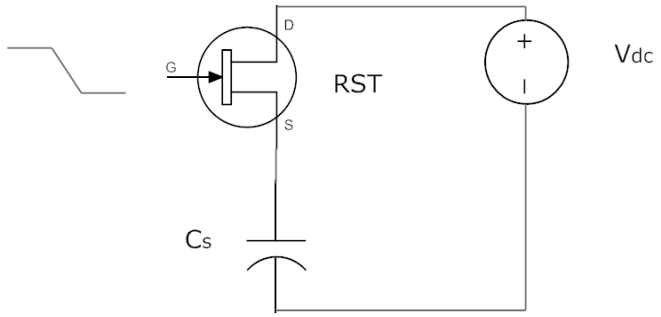

Figure 3-Capacitive reset circuit with transistor as switch.

We have developed a test circuit to study active reset circuits such as the one in Figure 3. Figures 4 and 5 are the schematic and layout diagram of the capacitive reset circuit that we developed to study partition noise. Designed with three reset circuits, each of the reset circuits is modified to add more flexibility. The reset circuits on the left and right are used to reset the source and drain voltage of the reset circuit of interest located at the

center of the circuit, M8. The left and right reset circuits also allow us to isolate the source and drain from the input. Various permutations of our test circuit with different transistor lengths and sense capacitances were designed and listed in Table 1. Our test-circuits share common supply voltages- VDD, VRST1, and VRST2-, reset signals-RST1, RST2, and INPUT-, and a DC bias voltage for the source follower-V_{BIAS}.

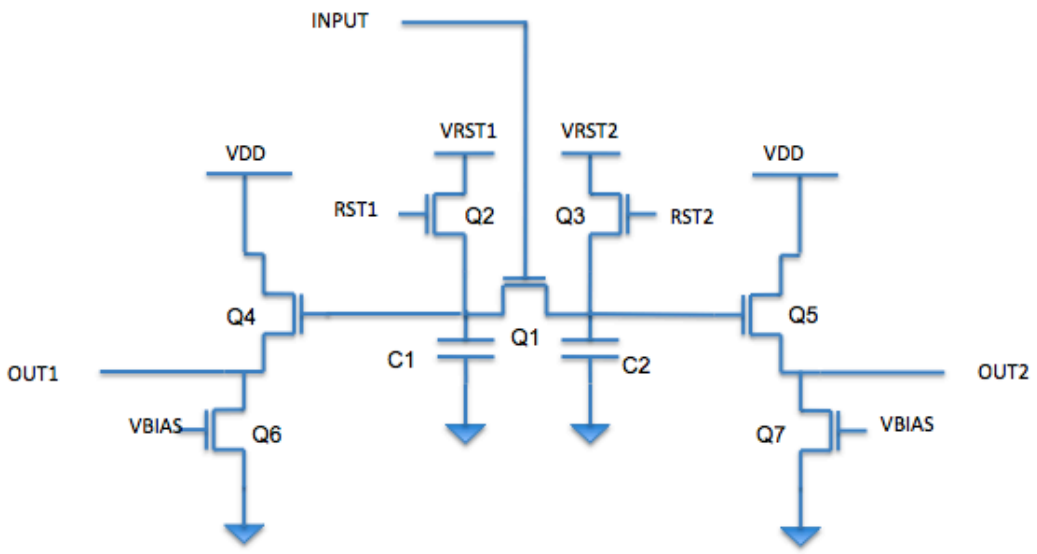

Figure 4-Schematic of partition noise test circuit.

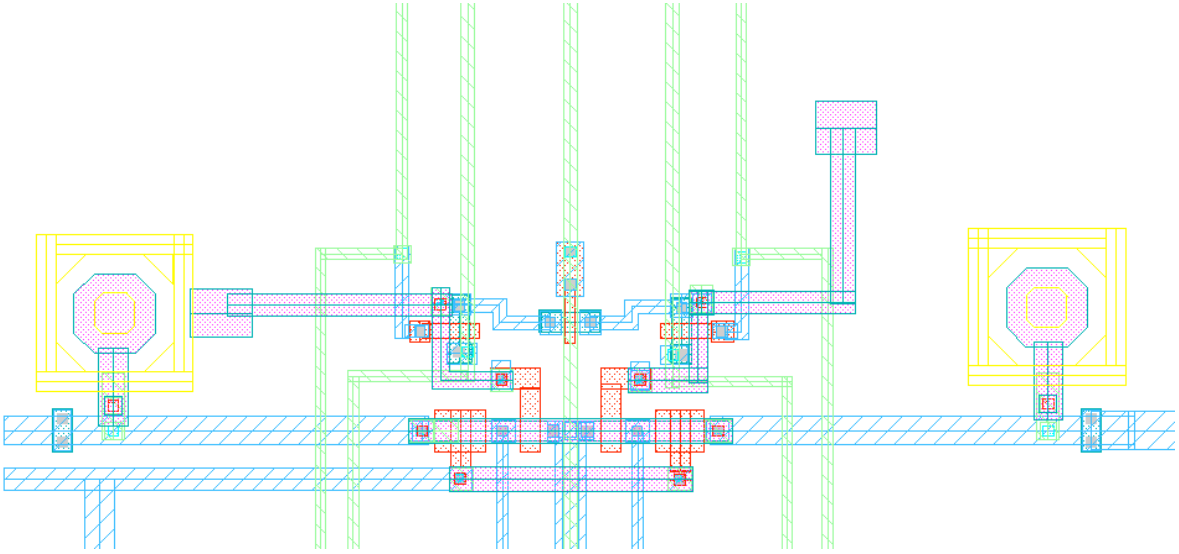

Figure 5-Layout of test circuit we designed. It has a 1 fF sense capacitor connected to the source and drain of the transistor Q1 from Figure 3.

Table 1-Partition noise test circuit permutations listed with gate length of transistor Q1 from Figure 3 and sense capacitances values.

Test type	cell name	Pin function	pin #
		Psub	1
		RST1	2
		VRST1	3
		VRST2	4
		RST2	5
		VDD	6
		INPUT	7
L=0.18 μm, C1=1 fF, C2=0.5 fF		OUTA1	8
		OUTA2	9
L=0.4 μm, C1=1 fF, C2=0.5 fF		OUTB1	10
		OUTB2	11
L=0.8 μm, C1=1 fF, C2=0.5 fF		OUTC1	12
		OUTC2	13
L=1.6 μm, C1=1 fF, C2=0.5 fF		OUTD2	14
			15
L=1.6 μm, C1=1 fF, C2=0.5 fF		OUTD1	16
L=1.6 μm, C1=0.5 fF, C2=0.5 fF		OUTE1	17
		OUTE2	18
L=1.6 μm, C1=2 fF, C2=0.5 fF		OUTF1	19
		OUTF2	20
L=1.6 μm, C1=4 fF, C2=0.5 fF		OUTG1	21
		OUTG2	22
		VBIAS	23
L=3.2 μm, C1=1 fF, C2=2 fF		OUTH2	24
L=3.2 μm, C1=1 fF, C2=0.5 fF		OUTJ1	25
		OUTJ2	26
L=3.2 μm, C1=1 fF, C2=1 fF		OUTK1	27
		OUTK2	28
L=3.2 μm, C1=1 fF, C2=4 fF		OUTL1	29
		OUTL2	30

In addition, the sense capacitors are connected to a source follower with active load. The source follower serves to isolate the sense capacitance from the load. Without the source follower, test equipment such as scope probes will add more capacitance to the sense capacitance nodes. The source follower gain is designed to be as close to one as possible. The load from test equipments such as scope probes limits the source follower bandwidth.

Our design has taken account of parasitic capacitance, test requirements, and partition noise expected. This ensures our circuit is testable and partition noise is large enough to be measured.

4.3 Sense Capacitor

One of our main concerns in designing this test structure was to maintain a relatively small area. For this reason, we have used metal-insulator-metal (MIM) capacitor to reduce the size of our test circuit. MIM capacitors are constructed with a thin insulation so that the distance of the dielectric is small. The outcome is a larger capacitor in a small device area.

For our purposes, we chose capacitor sizes 0.5 fF, 1 fF, 2 fF, and 4 fF. The capacitors have a 1 to 2 ratio for symmetry reasons. As a result, we designed a 1 μF capacitor to construct the different capacitances. Two 1 μF capacitors are connected in parallel to make the 2 fF capacitor, and two 1 μF capacitors are connected in series to make the 0.5 μF capacitor. This will ensure that even with process variation, the three capacitors have the ratios 1 to 2, and 1 to 4.

In our layout of the sense capacitor, we have made the capacitor in the shape of a hexagon shown in Figure 6. The advantage of a hexagonal capacitor versus a square capacitor is a smaller capacitance. Our process limits the shortest distance from via to planar edge, so we removed the corners of the square to meet the criteria [6]. The resulting capacitor is an equiangular capacitor to combat process variation and the capacitance can be computed using Equation 10.

$$Capacitance = \left(\frac{7}{8}LW\right)\left(\frac{capacitance}{\mu m^2}\right) \tag{10}$$

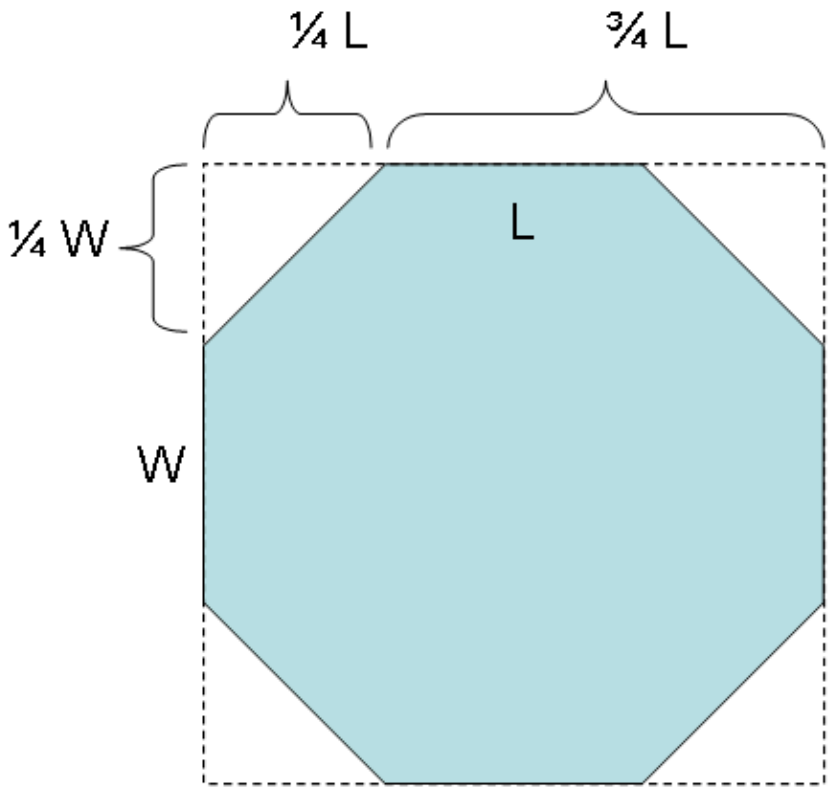

Figure 6-Diagram of the hexagonal capacitor.

4.3 Summary

Based on our simulations, we chose five reset transistor lengths to study. Each reset transistor design maintains the same parasitic capacitance and width. This allowed us to extract partition noise from total reset noise through varying only the transistor length. We assumed no process variation to simplify the results of our study. Furthermore, our capacitor sizes amplified the carrier fluctuation but maintained a manageable charge injection from the reset transistor.

CHAPTER FIVE: RESULTS

5.1 Introduction

In this chapter, we examine the results from TCAD simulation. These results will determine how to design our test circuit and the test equipment required to measure partition noise.

5.2 TCAD Simulation Results

We have simulated three reset transistor lengths to help determine the amount of partition noise each reset transistor will generate. Our sense capacitors are 0.5 fF and 1 fF, and we chose 0.4 μm, 0.7 μm, and 1 μm length transistors for our reset circuit. We applied 1V at the drain. The source voltage depends on the results from the charge injection shown in Figures 7 and 8 for 1 fF and 0.5 fF sense capacitors, respectively. The gate is swept from 0 V to 3.0 V to extract the threshold voltage.

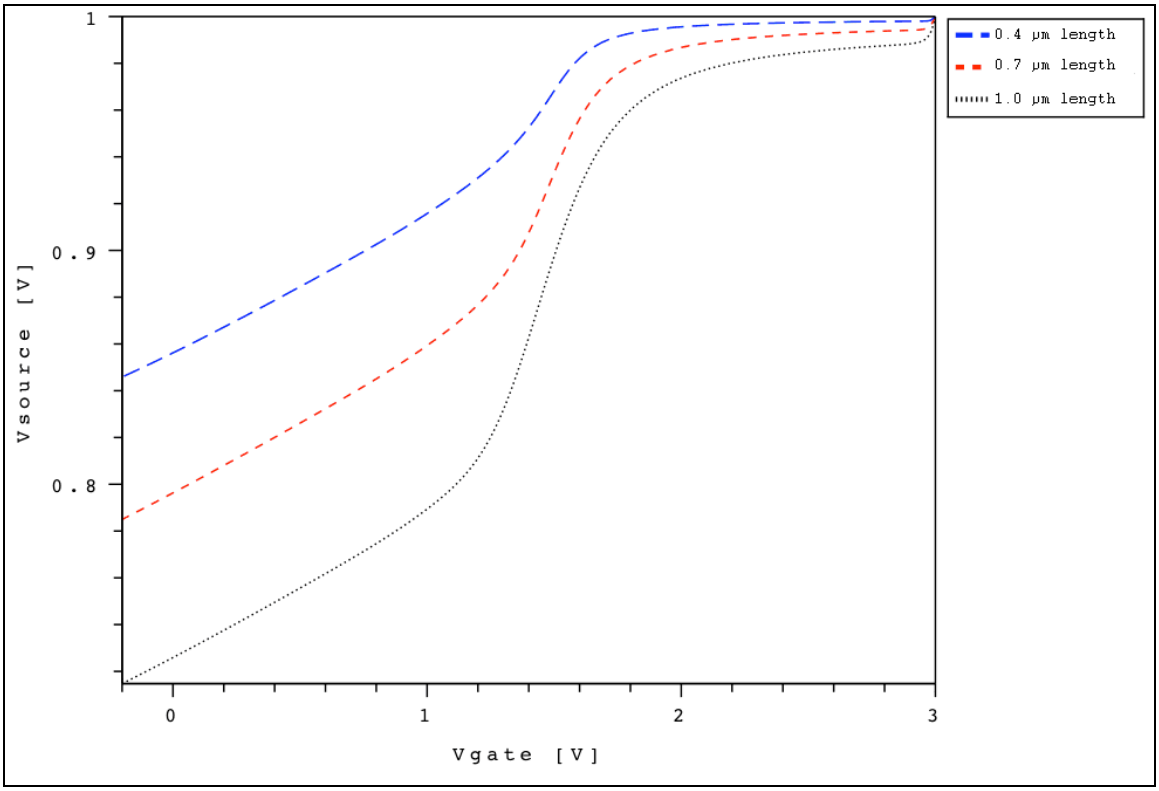

Figure 7-The drain is set to 1 V while the gate voltage is swept from 3 V to -0.2 V. This graph shows the charge injection into the source and sense capacitor node. The voltage on the source when Vgate=0 V is used to extract the threshold voltage in simulations. This is simulated with a 1 fF sense capacitor.

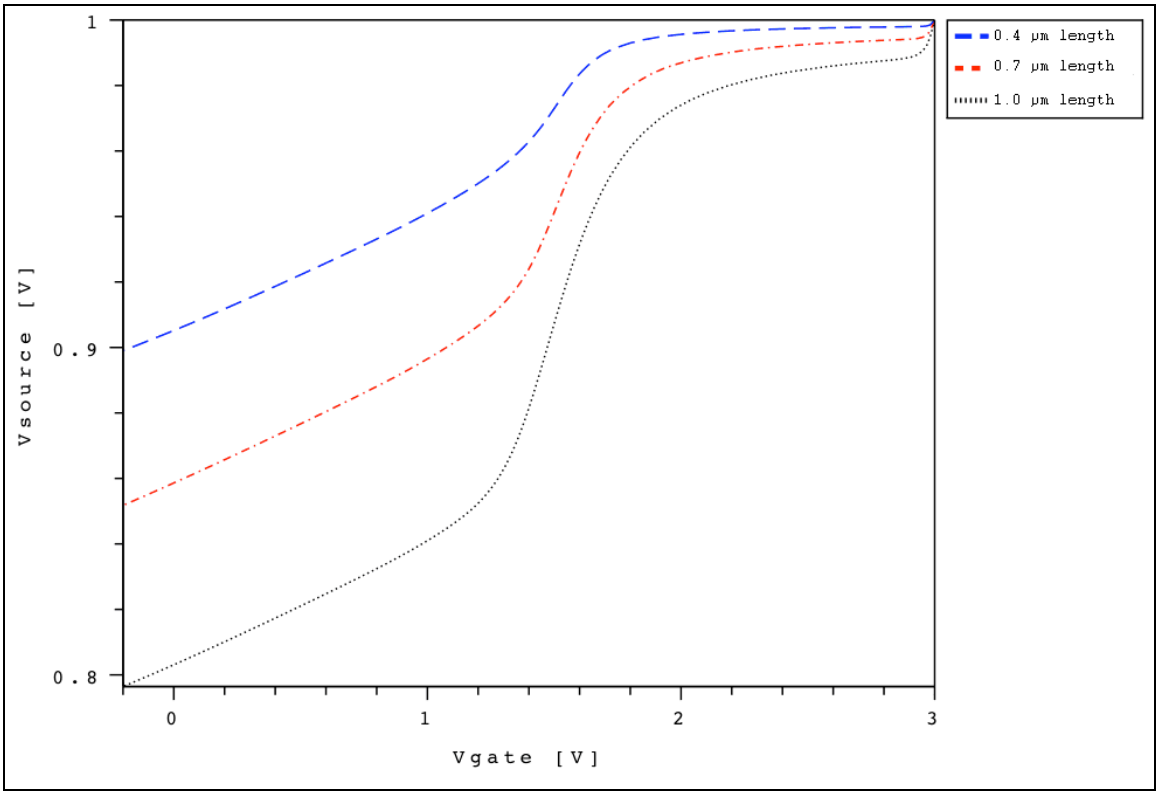

Figure 8-The drain is set to 1 V while the gate voltage is swept from 3 V to -0.2 V. This graph shows the charge injection into the source and sense capacitor node. The source voltage at Vgate=0 V is used to extract the threshold voltage in simulations. This is simulated with a 0.5 fF sense capacitor.

To extract the threshold voltage, we decided to use the ELR method of extrapolating the threshold voltage. That is, we used the linear portion of the drain current, I_d, to gate to source voltage, $V_{GS,}$ to extrapolate down to x-intercept [9]. The x-intercept is our threshold voltage, which in turn is the gate voltage, V_G. Our simulation results are listed in Tables 2 and 3 for a 1 fF and 0.5 fF sense capacitors, respectively.

Table 2-These are the corresponding threshold voltage for 0.4 μm, 0.7 μm, and 1 μm length transistors with a 1 fF sense capacitor.

Transistor Length [μm]	Threshold Voltage [V]
0.4	1.578
0.7	1.557
1.0	1.532

Table 3-These are the corresponding threshold voltage for 0.4 μm, 0.7 μm, and 1 μm length transistors with a 0.5 fF sense capacitor.

Transistor Length [μm]	Threshold Voltage [V]
0.4	1.485
0.7	1.524
1.0	1.563

To extract the number of residual electron in the channel, the drain is biased at 1 V and the gate is biased at 3 V. The source is at 1 V after all signals are settled. We swept the gate from 3 V to 0 V to perform a transient analysis and integrate the electron density in the inversion channel at the same time. Our TCAD simulation on the total residual channel charge is shown in Figures 9 and 10. Figure 9 shows the simulation result when the sense capacitance is 1 fF. With a 1 fF sense capacitance, the partition noise is l.85 μV

for a 0.4 μm length and width transistor. This means that measuring down to 1.85 μV of resolution would require at least a 16 bit resolution in a 50 mV range oscilloscope. Figure 10 are results from a 0.5 fF capacitor showing that the partition noise for the same transistor size is 3.6 μV. Most oscilloscopes have resolutions of 8, 12, or 16 bits, as well as a combination of the three sometimes. So, even though the partition noise has almost doubled, we still need 16 bits of resolution because 12 bits have a least significant bit (LSB) value of 12 μV.

Using the channel charge density and threshold voltage results from our TCAD simulations, we were able to pinpoint the charge density that will contribute to partition noise. Tables 4 and 5 show the expected partition noise for 0.4 μm to 1 μm transistor lengths with 0.4 μm transistor width. The results in Table 4 are for a 1 fF sense capacitor, whereas Table 5 results are from a 0.5 fF sense capacitor.

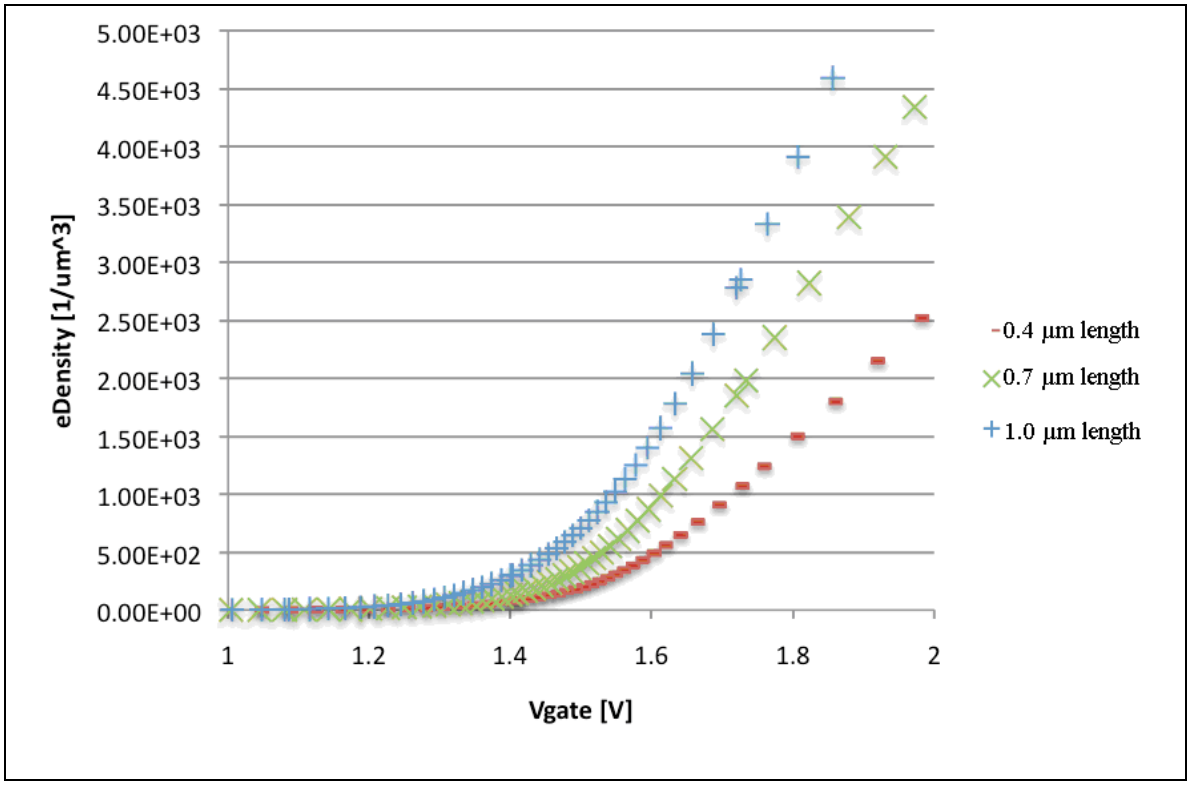

Figure 9-This is the resulting electron density in the inversion channel to gate voltage for a 0.4 µm width transistor and 1 fF sense capacitor.

Table 4-Table of transistor length to expected partition noise voltage with 1 fF sense capacitor. N is the expected electron density per square micron in the channel when the transistor is operating at the edge of sub-threshold, $\overline{N_n^2}$ is the carrier fluctuation across Cs, and $\overline{V_n^2}$ is the expected partition noise voltage.

Length	N	$\overline{N_n^2}$	$\overline{V_n^2}$
1.0 µm	929	154	3.96 µV
0.7 µm	613	102	2.62 µV
0.4 µm	433	72	1.85 µV

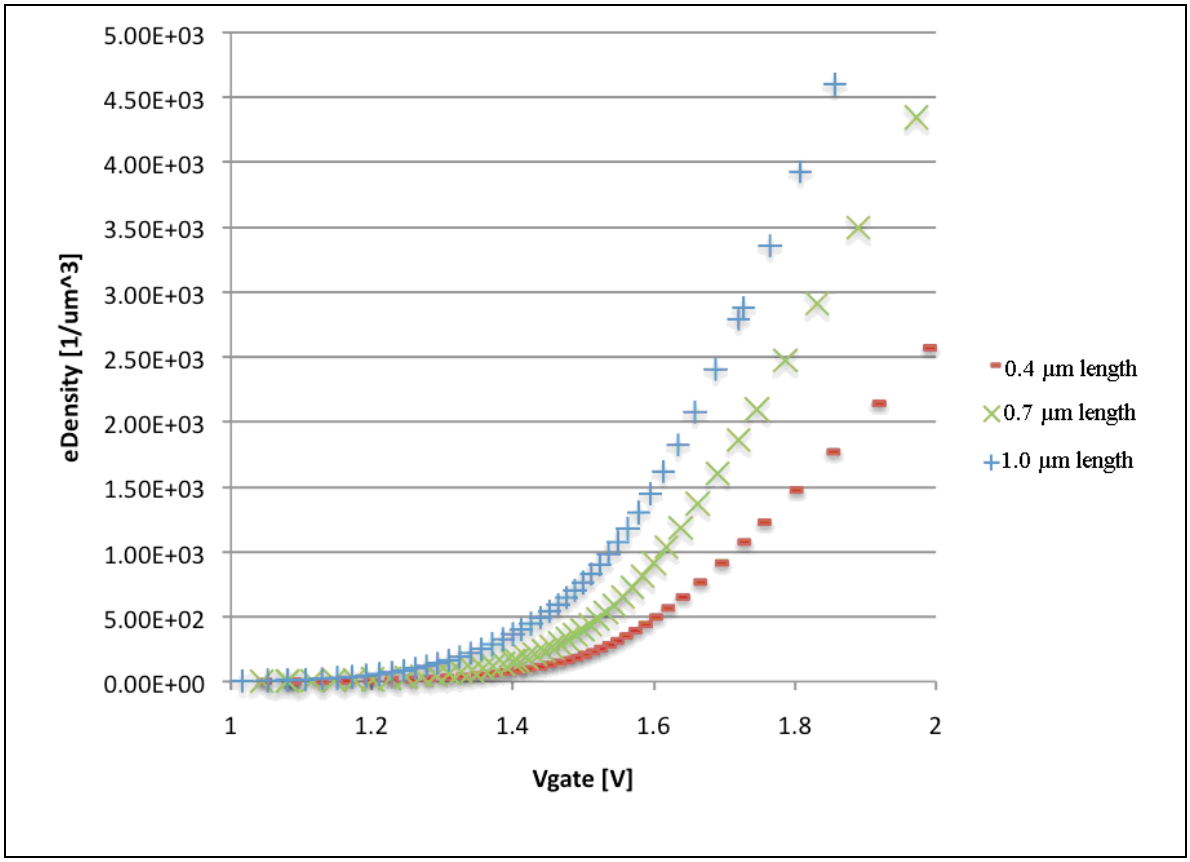

Figure 10-This is the resulting electron density in the inversion channel to gate voltage for a 0.4 µm width transistor and 0.5 fF sense capacitor.

Table 5-Table of transistor length to expected partition noise voltage with 0.5 fF sense capacitor. N is the expected electron density per square micron in the channel when the transistor is operating at the edge of sub-threshold, $\overline{N_n^2}$ is the carrier fluctuation across Cs, and $\overline{V_n^2}$ is the expected partition noise voltage.

Length	N	$\overline{N_n^2}$	$\overline{V_n^2}$
1.0 µm	1178	196	20.1 µV
0.7 µm	482	80	8.23 µV
0.4 µm	185	31	3.16 µV

Our simulation results show that the partition noise is less than 2 μV with a 3 ns fall-time. This means that in order to have an accurate measurement of partition noise, we would need to add a third stage that will gain up our signal of interest.

We can further increase the transistor lengths in order to increase partition noise generated and use a larger sense capacitor to avoid issues with charge injection. Another option is to further reduce the sense capacitance to amplify the noise signal. However, the second option will also increase the reset noise due to thermal noise. As previously suggested, the use of an external high gain amplifier in combination with option two will also reduce measurement error.

5.3 Summary

Our TCAD simulations have extracted the threshold voltage and residual channel charge that contribute to partition noise. The results showed that partition noise is a relatively small noise source, and it requires a low noise and high-resolution test setup in order for it to be accurately measured.

CHAPTER SIX: IMPLEMENTATION

6.1 Introduction

To measure partition noise, we must also take into account other noise sources such as reset noise, sense capacitance, and source follower gain and noise. In this section, we will go through the test setup and requirements to measure and extract partition noise. We will take a top-down approach in our test setup. First, we explain how to measure partition noise, source follower noise, and then source follower gain. Then, the mathematical relationship between the measured output noises to partition noise is provided below.

6.2 Partition Noise vs. Transistor Length

Based on the theory of partition noise, the only way to quantify partition noise would be to have a reference point where the transistor length is zero. Even though that is not possible, we can extrapolate down to zero length. We must measure the reset noise due to both thermal noises from the inversion channel and partition noise for various reset transistor lengths.

We will now cover bias conditions for our test circuit. For signal references, please refer to Figure 4. The sense capacitors C1 and C2 are reset to 1.5 V minus charge injection. While C1 is held at 1.5 V, RST2 turns off leaving C2 floating, while Q1 gate is first ramped from 0 V to 3 V and then back down to 0 V with an approximate fall-time of 3.75 ns. A timing diagram with bias conditions is shown in Figure 11. The noise voltage

on C2 is our partition noise plus reset noise. So, to track partition noise, the length of Q1 will be varied with all else constant. However, the noise voltage across C2 is measured at the output of the source follower, OUT2. As a result, we must take into account the source follower noise and gain.

$$\overline{V_{RST}^2(L)} = \frac{\overline{V_{OUT}^2(L)}}{A_{SF}} - \overline{V_{SF}^2(L)} \tag{11}$$

$\overline{V_{SF}^2(L)}$ and A_{SF} are the source follower noise and gain. $\overline{V_{OUT}^2(L)}$ is the noise measured at the output of the source follower. $\overline{V_{RST}^2(L)}$ is the total reset noise on across C2 and it has taken the source follower gain and noise into account. Since partition noise cannot be measured directly because it is lumped with reset noise, we can extract the increase in partition noise contributed from a transistor with length L_1 to L_2, where L_2 is greater than L_1. The increase in partition noise with transistor length, $\Delta\overline{V_{PN}^2(L_1 - L_2)}$, is the difference in reset noise, $\overline{V_{RST}^2(L)}$ with the change in transistor length.

$$\Delta\overline{V_{PN}^2(L_1 - L_2)} = \overline{V_{RST}^2(L_1)} - \overline{V_{RST}^2(L_2)} \tag{12}$$

We must measure the reset noise of several reset circuits with the same sense capacitance for different transistor lengths, and extrapolate reset noise down to L=0 to identify the reset noise contributed from thermal noise and partition noise.

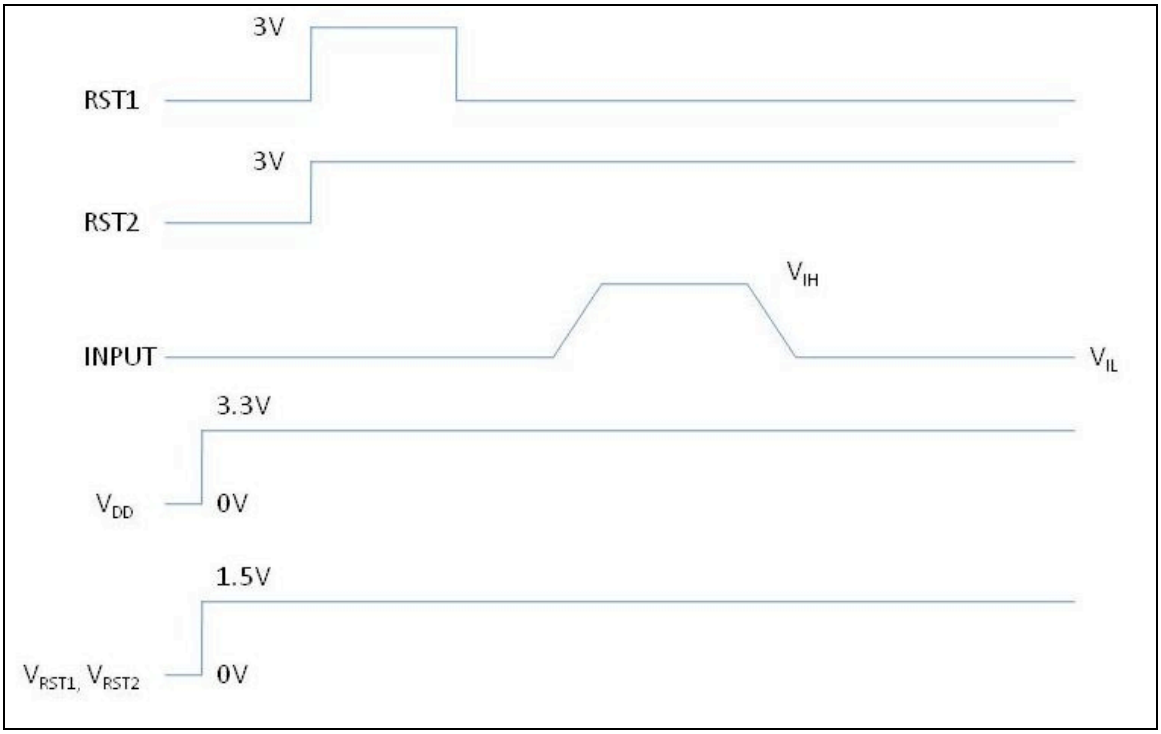

Figure 11-Timing and bias condition diagram. The cycle time is 20 ms to make sure all signals have settled.

6.3 Source Follower Gain

The source follower gain is very important in that it attenuates the signal across C2. To measure the gain of the source, V_{DD} and V_{bias} are biased at 3.3 V and 200 mV, while RST2 is turned on. We performed a sweep on V_{RST2} from 0 V to 1.5 V. The slope of linear portion of V_{RST2} to OUT2 is our source follower gain represented in Equation 13. The same can be done for the source follower on the left side since the circuit is symmetric. This test will also show the operating range of V_{RST1} and V_{RST2}.

$$A_{SF} = \frac{V_{OUT2}}{V_{RST2}} \tag{13}$$

6.4 Source Follower Noise

Source follower noise resulting from electrons colliding with the oxide to bulk interface is a white noise. We measure source follower noise with RST2 set to 3 V and V_{RST2} at 1.5 V. The source follower noise voltage must take into account of the source follower gain as shown in Equation 14.

$$\overline{V_{SF}^2} = \frac{\overline{V_{OUT2}^2}}{A_{SF}} \tag{14}$$

A_{SF} is the source follower gain, $\overline{V_{OUT2}^2}$ is the noise voltage measured at the source follower output, and $\overline{V_{SF}^2}$ is the actual source follower noise.

6.5 Setup Requirements

The setup requirement for noise measurements is especially critical. In general, direct current (DC) signals need to have bypass capacitors close to the device under test (DUT) to reduce high frequency noise. Digital signals can also have a low pass filter to reduce signal reflection. Oscilloscope or measurement equipment resolution must be a minimum of 16-bit resolution in a 50 mV range for a LSB of 763 nV to measure the partition noise of short channel MOSFETS. Furthermore, measurements on the wafer level require that the DUT be inside a Faraday cage, and use battery source instead of a DC supply instead of power supplies to reduce noise [10].

6.6 Summary

We have provided extensive method and setup requirements to extract partition noise using the circuit we designed. This includes measuring the source follower noise and gain.

CHAPTER SEVEN: CONCLUSION AND FUTURE WORK

7.1 Conclusion

In this work, we have developed a method to measure and characterize partition noise of an active reset circuit using TCAD simulations, which were used to extract the threshold voltage of a NMOS using the ERL method and to extract the electron charge density in the inversion channel during operation. Using the threshold voltage and electron charge density, we estimated the partition noise generated by a short channel NMOS. We found partition noise to be a very minuscule noise source of a few microvolts depending on the sense capacitance. From this information, we have designed a test circuit and test methodology to study partition noise.

7.2 Future Work

Our work has provided the circuit design and test method to measure partition noise. Future work on this subject will characterize the designed circuit as stated in the implementation chapter.

The testing and measurement of noise in general are difficult without the proper setup. The measurement of partition noise can be further improved by adding a second stage high gain, low noise amplifier built-in or added externally on a printed circuit board (PCB). The advantage in having a built-in amplifier is that it relaxes the oscilloscope

requirement and simplifies the setup. However, it may take several tries to design and fabricate a working amplifier with the specifications required.

If the test circuit can be packaged and tested on a PCB, then designing a test board with bypass components, filters, and an external amplifier will reduce noise from our input signals. Of course, the PCB should not be limited to just the components we suggested. Careful consideration into the PCB layout is needed to avoid cross coupling since we are working with digital signals.

As our technology moves to the gigahertz range, further studies into partition noise with fall times of less than 1 ns are needed. Sense capacitance may also be reduced for faster charge up time so that partition noise will become a large part of the total reset noise. Although a function generator or an arbitrary waveform generator can control the fall-time of our reset signal, they are usually limited to 1 ns. Instead, an additional driver circuit can be added to the input stage to control the fall-time of the input signal. These additions will greatly clarify the effects of partition noise on short channel MOSFETs.

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APPENDIX A: NMOS FABRICATION CYCLE

Simulation file: sprocess_lig.cmd defines the NMOS fabrication cycle

```
defop Boron_implants ()
{
  comment (text : "Boron implants");
  implant (species : boron, dose : 4.5e12 /cm2, energy : 5.0 keV, tilt : 0 deg, rotation : 0
deg, type : default);
  implant (species : boron, dose : 5.0e11 /cm2, energy : 20 keV, tilt : 0 deg, rotation : 0
deg, type : default);
  implant (species : boron, dose : 1.6e13 /cm2, energy : 85 keV, tilt : 0 deg, rotation : 0
deg, type : default);
  implant (species : boron, dose : 2.0e13 /cm2, energy : 260 keV, tilt : 0 deg, rotation : 0
deg, type : default);
}

defop Growing_gate_oxide ()
{
  comment (text : "Growing gate oxide");
  insert (dios : "

", sprocess : "
mgoals accuracy=1e-5 resolution=0.1 minedge=2e-6 normal.growth.ratio=2.0
min.normal.size=5e-4
", sde : "

", tsuprem4 : "

");
  deposit (material : oxide, thickness : .005 um);
  anneal (time : 90 min, temperature : 1000 degC);
}

defop Poly_gate_definition ()
{
  comment (text : "Poly Gate definition");
  deposit (material : poly, thickness : 0.21 um, deposition_type : isotropic);
  pattern (layer : "GATE", polarity : light_field);
  etch (material : poly, thickness : 0.23 um, etch_type : anisotropic, type : default);
```

```
  etch (material : resist, etch_type : strip);
}

defop Poly_reoxidation ()
{
  comment (text : "Poly reoxidation");
  deposit (material : oxide, thickness : .007 um);
  anneal (time : 8 min);
}

defop Remeshing_for_LDD ()
{
  comment (text : "Remeshing for LDD and halo implants");
  insert (dios : "

", sprocess : "
refinebox silicon min= {0.0 @<0.5*lgate/-0.04>@} max= {0.1 0@<0.5*lgate+0.03>@}
xrefine= {0.01 0.01 0.01} yrefine= {0.01 0.01 0.01} add
refinebox remesh
", sde : "

", tsuprem4 : "

");
}

defop LDD_halo_implants ()
{
  comment (text : "LDD");
  implant (species : arsenic, dose : 1.0e14 /cm2, energy : 15 keV, tilt : 0 deg, rotation : 0
deg);
}

defop Spacer_formation ()
{
  comment (text : "Spacer formation");
  deposit (material : nitride, thickness : .04 um);
  etch (material : nitride, thickness : .08 um, etch_type : anisotropic);
}

defop Remeshing ()
{
  comment (text : "Remeshing for Source/Drain implants");
  insert (dios : "
```

```
", sprocess : "
refinebox silicon min= {0.04 @<0.5*lgate-0.04>@} max= {0.18 \$ymax}  xrefine=
{0.01 0.01 0.01} yrefine= {0.05 0.05 0.05} add
refinebox remesh
", sde : "

", tsuprem4 : "

");
}

defop Source_Drain_implants ()
{
  comment (text : "Source/Drain implants");
  implant (species : arsenic, dose : 1.0e15 /cm2, energy : 25 keV, tilt : 0 deg, rotation : 0
deg);
  anneal (time : 10 sec, temperature : 1000 degC);
}

defop Contact_Pads ()
{
  comment (text : "Contact pads");
  etch (material : oxide, thickness : 0.25 um, etch_type : anisotropic);
  deposit (material : aluminum, thickness : 30 nm);
  pattern (layer : "METAL", polarity : light_field);
  etch (material : aluminum, thickness : 0.25 um, etch_type : anisotropic, type : default);
  etch (material : aluminum, thickness : 0.02 um, etch_type : isotropic, type : default);
  etch (material : resist, etch_type : strip);
}

defop Save_Structure ()
{
  comment (text : "Save Structure");
  insert (dios : "

", sprocess : "
transform clip min= {-1 -1} max= {2 10}
contact name=gate  point x=-0.2 y=0.001 replace
contact name=drain point x=-0.02 y=\[expr \$ymax - 0.001\] replace
contact name=substrate box silicon xlo=1.5 ylo=0 xhi=2.5 yhi=\$ymax

set Ygox \[interface oxide /silicon y = 0.001 \]
set Ypol \[interface poly  /oxide y = 0.001 \]
```

```
set Ytmp \[expr \$Ygox + 0.005\]
set Tox  \[expr \$Ygox-\$Ypol\]
sel z = { NetActive }
set Xgd \[format %.3e \[lindex \[lsort -real \[interpolate x = \$Ytmp  silicon val=1e15\]\]
0\]\]
set Xj  \[format %.3e \[lindex \[lsort -real \[interpolate y = @<0.5*lgate+0.39>@ silicon
val=1e15\]\] 0\]\]

#set Lgeff x
puts \"DOE: Lgeff \[format %.3e \[expr 2.0*\$Xgd\]\]\"
#set Xj    x
puts \"DOE: Xj    \[format %.3e \$Xj\]\"
#set Ygox  x
puts \"DOE: Ygox  \[format %.3e \$Ygox\]\"
#set Tox  x
puts \"DOE: Tox   \[format %.3e \$Tox\]\"
", sde : "

", tsuprem4 : "

");
}

environment (title : "2D Process simulation", save : true, grid : true, debug : false,
check1d : false, analytical : false, simulator : sprocess, region : "SIM2N", output :
"n@node@", node : "@node@", side : front, graphics : false, depth : 5 um, user_grid :
"line x location= 0.0      spacing= 1.0<nm>  tag=SiTop
line x location=50.0<nm>  spacing=10.0<nm>
line x location= 0.5<um>  spacing=50.0<nm>
line x location= 2.0<um>  spacing= 0.2<um>
line x location= 4.0<um>  spacing= 0.4<um>
line x location=10.0<um>  spacing= 2.0<um>  tag=SiBottom

set ymax @<lgate/2.0+0.4>@
line y location=0.0     spacing=\$ymax/8.0   tag=Mid
line y location=\$ymax  spacing=\$ymax/8.0   tag=Right

region silicon xlo=SiTop xhi=SiBottom ylo=Mid yhi=Right", grid_refinement : Struct {
  dios : "";
  sprocess : "";
  sde : "";
  tsuprem4 : "";
}, tsuprem4_delta_vertical : 0.5 um, tsuprem4_delta_horizontal : 0.5 um,
tsuprem4_min_vertical : 0.1 um, tsuprem4_min_horizontal : 0.1 um);
```

```
substrate (dopant : boron, concentration : 1.0e+16 /cm3);
insert (dios : "

", sprocess : "
AdvancedCalibration
", sde : "

", tsuprem4 : "

");
insert (dios : "

", sprocess : "
implant tables = AdvCal
", sde : "

", tsuprem4 : "

");
insert (dios : "

", sprocess : "
pdbSetSwitch Ox_Si B BoundaryCondition ThreePhaseSegregation
", sde : "

", tsuprem4 : "

");
insert (dios : "

", sprocess : "
pdbSetDouble Oxide_Silicon B TrappingRate_Silicon  {\[Arr 3.0e-15 2.5\]}
", sde : "

", tsuprem4 : "

");
Boron_implants ();
Growing_gate_oxide ();
Poly_gate_definition ();
Poly_reoxidation ();
Remeshing_for_LDD ();
LDD_halo_implants ();
anneal (time : 10 sec, temperature : 1000 degC);
```

```
Spacer_formation ();
Remeshing ();
Source_Drain_implants ();
Contact_Pads ();
Save_Structure ();
```

APPENDIX B: NMOS LAYOUT AND MESHING

Simulation file: sde_dvs.cmd defines the NMOS layout and meshing

```
#setdep @previous@

;--- Internal parameters -------------------------------
(if (string=? "@Type@" "nMOS")
 (begin
  (define DopPol  "ArsenicActiveConcentration")
 )
 (begin
  (define DopPol  "BoronActiveConcentration")
 )
)

(define Lg      @lgate@)
(define Xgdo    (* 0.5 @Lgeff|-1@))
(define Xj      @Xj|-1@)
(define Ygox    @Ygox|-1@)
(define Tox     @Tox|-1@)

(define PNres   0.006)
(define Xg      (/ Lg 2.0))
(define Ypol    (- Ygox Tox))
(define dXext   0.01)

(define BNDin  "n@previous@_bnd.tdr")
(define TDR    "n@previous@_fps.tdr")

;--- Load Boundary-----------------------------------------------------
(sdeio:read-tdr-bnd  BNDin)

(define Xmin (position:x (car (bbox (get-body-list)))))
(define Xmax (position:x (cdr (bbox (get-body-list)))))
(define Ymin (position:y (car (bbox (get-body-list)))))
(define Ymax (position:y (cdr (bbox (get-body-list)))))

;--- Place sub meshes ------------------------------------------------
(sdedr:define-submesh "SubMesh" TDR)
```

```
(sdedr:define-refinement-window "Win.RightHalf" "Rectangle"
 (position        -0.01  (- Ymin 0.01) 0.0)
 (position (+ Xmax 0.01) (+ Ymax 0.01) 0.0))

(sdedr:define-submesh-placement "SubMesh_R" "SubMesh"
   "Win.RightHalf" "Replace"
   "AttachPoint" (position 0 0 0) "ToPoint" (position 0 0 0) )

;--- Meshing -------------------------------------------------------
;-- Meshing Strategy:
;- Silicon
(sdedr:define-refinement-size "RSize.Silicon"
  (/ Xmax 4.0)  (/ Ymax 16.0)
  (/ Xmax 8.0)  (/ Ymax 18.0) )
(sdedr:define-refinement-material "RPlace.Silicon"
 "RSize.Silicon" "Silicon" )

;- Source/Drain area
(define YSDref (* 1.5 Xj))
(sdedr:define-refinement-size "RSize.SD"
  (/ (- Xmax Xg) 12.0) (/ (- YSDref Ygox) 16.0)
   PNres                PNres )
(sdedr:define-refinement-function "RSize.SD"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-window "RWin.SD"
 "Rectangle"
 (position Xg    0.0    0.0)
 (position Xmax  YSDref 0.0) )
(sdedr:define-refinement-placement "RPlace.SD"
 "RSize.SD" "RWin.SD" )

; Junctions under the gate
(sdedr:define-refinement-size "RSize.GD"
  (* 1.0 PNres)  (* 1.0 PNres) 0.0
  (* 0.8 PNres)  (* 0.8 PNres) 0.0)
; Gate-Drain Junction
(sdedr:define-refinement-window "RWin.GD"
 "Rectangle"
 (position (- Xgdo dXext)    Ygox                    0.0)
 (position (+ Xgdo dXext) (+ Ygox (* 0.35 (- Xj Ygox))) 0.0) )
(sdedr:define-refinement-placement "RPlace.GD"
 "RSize.GD" "RWin.GD" )

; Channel Multibox
```

```
(sdedr:define-refinement-window "MBWindow.Channel"
 "Rectangle"
 (position  0.0           Ygox      0.0)
 (position (* 1.1 Xgdo)  (* 0.5  Xj) 0.0) )
(sdedr:define-multibox-size "MBSize.Channel"
  (/ Xg 4.0)  (/ (- Xj Ygox) 4.0)
  (/ Xg 8.0)    2e-4
  -1.45         1.45 )
(sdedr:define-multibox-placement "MBPlace.Channel"
 "MBSize.Channel" "MBWindow.Channel" )

; Gate Multibox
(sdedr:define-refinement-window "MBWindow.Gate"
 "Rectangle"
 (position 0.0 Ymin  0.0)
 (position Xg  Ypol  0.0) )
(sdedr:define-multibox-size "MBSize.Gate"
  99   (/ (- Ypol Ymin) 4.0)
  66     3e-4
  0.0   -1.75 )
(sdedr:define-multibox-placement "MBPlace.Gate"
 "MBSize.Gate"  "MBWindow.Gate" )

;--- Saving BND file ------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "n@node@_half_bnd.tdr")

;-----------------------------------------------------------------------
; Save CMD file
(sdedr:write-cmd-file "n@node@_half_msh.cmd")

;-----------------------------------------------------------------------
; Build Mesh
(system:command "mesh -F tdr n@node@_half_msh")

;-----------------------------------------------------------------------
; Reflect device
(system:command "tdx -mtt -x -ren drain=source n@node@_half_msh n@node@_msh")
```

APPENDIX C: THRESHOLD VOLTAGE EXTRACTION

Simulation file: sdevice_des.cmd is used to extract the threshold voltage

```
!(
if { "@Type@"  == "nMOS" } {
  set SIGN   1.0
  set EQNS   "Poisson Electron"
} else {
  set SIGN   -1.0
  set EQNS   "Poisson Hole"
}
)!

File {
   * input files:
   Grid=   "@tdr@"
   Parameter="@parameter@"
   * output files:
   Plot=   "@tdrdat@"
   Current="@plot@"
   Output= "@log@"
}

Electrode {
   { Name="source"    Voltage=@Vs@ Resistor=40 }
   { Name="drain"     Voltage=0.0 Resistor=40 }
   { Name="gate"      Voltage=0.0 Barrier=-0.55 }
   { Name="substrate" Voltage=0.0 }
}

Physics{
   EffectiveIntrinsicDensity( OldSlotboom )
}

Physics(Material="Silicon"){
   MLDA
   Mobility(
      PhuMob
      HighFieldSaturation
```

```
    EnormalHigh
  )
  Recombination(
    SRH( DopingDep )
  )
}

Insert = "PlotSection_des.cmd"
Insert = "MathSection_des.cmd"

Solve {
*- Creating initial guess:
  Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson }
  Coupled { !(puts $EQNS)! }

*- Ramp to drain to Vd
  Quasistationary(
    InitialStep=1e-1 Increment=1.35
    MinStep=1e-5 MaxStep=0.5
    Goal { Name="drain" Voltage=!(puts [expr $SIGN*@Vd@])! }
  ){ Coupled { !(puts $EQNS)! } }

*- Vg sweep
  NewCurrentFile="IdVg_"
  Quasistationary(
    DoZero
    InitialStep=1e-3 Increment=1.35
    MinStep=1e-5 MaxStep=0.05
    Goal { Name="gate" Voltage=!(puts [expr $SIGN*@Vdd@])! }
  ){ Coupled { !(puts $EQNS)! }
    CurrentPlot( Time=(Range=(0 1) Intervals=30)  )
  }
}
```

APPENDIX D: EXTRACT THRESHOLD VOLTAGE WITH INSPECT

Simulation file: inspect_ins.cmd extracts threshold voltage from Id-Vgs graph.

```
#-----------------------------------------------------------------------#
#set Vtgm   x
#set Vti    x
#set Id     x
#set SS     x
#set gm     x

set N     @node@
set i     @node:index@
set Lg    @lgate@
set Vds   @Vds@
set Vg    @Vdd@
set Type  @Type@
puts "Gate Length: $Lg um"

set ID "$Type"
set N   ${Type}_${N}

#- Automatic alternating color assignment tied to node index
#-----------------------------------------------------------------------#
set COLORS  [list green blue red orange magenta violet brown]
set NCOLORS [llength $COLORS]
set color   [lindex  $COLORS [expr $i%$NCOLORS]]

#- INSPECT IdVg plotting
#-----------------------------------------------------------------------#
# Plotting Id vs Vg curves
gr_setTitleAttr "IdVg Lg=$Lg Vds=$Vds"

proj_load  IdVg_@plot@ PLT($N)

cv_createDS IdVg($N) \
 "PLT($N) gate OuterVoltage" "PLT($N) drain TotalCurrent" y
cv_abs IdVg($N) y
cv_setCurveAttr IdVg($N) "IdVg $ID" \
  $color solid 2 none 3 defcolor 1 defcolor
```

```
gr_setAxisAttr X  {Gate Voltage (V)}     16  {} {} black 1 14 0 5 0
gr_setAxisAttr Y  {Drain Current (A/um)} 16  {} {} black 1 14 0 5 1

#- Extraction
#-----------------------------------------------------------------------#
source EXTRACT_ins.lib

#- Defining current level for Vti extraction
#-----------------------------------------------------------------------#
set Io    [expr 100e-9/$Lg] ; # [A/um]
if { $Type == "nMOS" } { set SIGN 1.0 } else { set SIGN -1.0 }

if { $Vds < 0.5 } {
set Vtb   [ExtractVtgmb Vtgm  IdVg($N) $Type]
}
set Vti   [ExtractVti   Vti    IdVg($N) $Io]
set Idmax [ExtractMax   Id     IdVg($N)]
set SS    [ExtractSS    SS     IdVg($N) [expr $SIGN*1e-2]]
set gm    [ExtractGmb   gm     IdVg($N) $Type]
```

APPENDIX E: CHARGE DENSITY EXTRACTION

Simulation file: sdevice1_des.cmd extracts the charge density of the inversion channel.

```
#setdep @node|-3@


** Comment here
Device MOS {

 Electrode {
  { Name="source"    Voltage=0.0 }
  { Name="drain"     Voltage=0.0 }
  { Name="gate"      Voltage=0.0 Barrier=-0.55 }
  { Name="substrate" Voltage=0.0 }
 }

 File {
  * input files:
  Grid=   "@tdr@"
  *files from NF sample
  *Grid = "mos_mdr.grd"
  *Doping = "mos_mdr.dat"
  *Parameter = "mos"
  * Parameter="@parameter@"
  * output files:
  Plot=   "mos_@tdrdat@"
  Current="mos_@plot@"
 }

 Physics {
  AreaFactor=0.4
  EffectiveIntrinsicDensity( OldSlotboom )
      Noise (
    #Hydro#  DiffusionNoise(e_h_Temperature)
      DiffusionNoise(LatticeTemperature)
      FlickerGRNoise
    )
 }

 Physics(Material="Silicon"){
```

```
 Mobility(
  PhuMob
  HighFieldSaturation
  EnormalHigh
 )
 Recombination(
  SRH( DopingDep )
 )
}

Physics(MaterialInterface="Silicon/Oxide"){
 Charge ( Conc=2.0e10 )
}

CurrentPlot {
 eDensity(
  Integrate(Window[(@<-(lgate-0.02)/2>@ 0.00) (@<(lgate-0.02)/2>@ 0.02)]
Name=Channel)
 )
}

NoisePlot {
        eeDiffusionLNS eeLNVSD eeDiffusionLNVSD eeFlickerGRLNVSD
        Grad2PoECACGreenFunction PoECReACGreenFunction
}

}



System {

Vsource_pset v2 (n2 n0) {pwl = (0       3
                        50e-9    3
                        @time@   -0.2
                        80e-6 -0.2)}

** Drain :  removed to add cap on drain
Vsource_pset v1 (n1 n0) { dc = 1 }

*reset transistor
MOS mos1 ( "drain"=n1 "gate"=n2 "source"=n3 "substrate"=n0)
Capacitor_pset c1 (n3 n0) { capacitance = @cap@ }
```

```
 *source follower
 *MOS mos2 ("drain"=nsfd "gate"=n3 "source"=nsfs "substrate"=n0)
 *Vsource_pset v3 (nsfd n0) { dc = 2.7 }
 *Capacitor_pset c2 (nsfs n0) { capacitance = 1e-12 }
 *Resistor_pset r1  (nsfs n0) { resistance = 1e6 }

 *initialize (n1 = 1 n2 = 3 n3 = 1)

 set (n0 = 0)

 ** Determining quantities to plot
 Plot "mos1_n@node@_des.plt" (time() n0 n1 n2 n3 i(c1,n3))
}

File {
 Current="@plot@"
 Output= "@log@"
 *would I need to add this to the output files list?  ACExtract="AC_@node@_"
}

Plot {
 *--Density and Currents, etc
 eDensity hDensity
 TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
 eMobility hMobility
 eVelocity hVelocity
 eQuasiFermi hQuasiFermi

 *--Temperature
 eTemperature Temperature hTemperature

 *--Fields and charges
 ElectricField/Vector Potential SpaceCharge

 *--Doping Profiles
 Doping DonorConcentration AcceptorConcentration

 *--Generation/Recombination
 SRH Band2Band * Auger
 * AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

 *--Driving forces
 eGradQuasiFermi/Vector hGradQuasiFermi/Vector
```

```
 eEparallel hEparallel eENormal hENormal

 *--Band structure/Composition
 BandGap
 BandGapNarrowing
 Affinity
 ConductionBand ValenceBand
 eQuantumPotential hQuantumPotential

 *--Gate Tunneling
 * eBarrierTunneling hBarrierTunneling  BarrierTunneling
 * eDirectTunnel hDirectTunnel
}

Math {

 Extrapolate
 RelErrControl
 Notdamped=1000
 Iterations=15
 ExitOnFailure
 Number_of_Threads = 1

*added for transient
 Digits=5
 Method = Blocked
 SubMethod = Pardiso
 Transient=BE
 CheckTransientError
 AutomaticCircuitContact

*added for noise
 Derivatives
 NewDiscretization
 ConstRefPot
}

Solve {

 NewCurrentPrefix = "ignore_"
 Coupled { Poisson }
 Coupled { Poisson Electron Hole Contact Circuit}

  *solve for noise
```

```
 ACCoupled(
        StartFrequency=1e0 EndFrequency=1e12 NumberOfPoints = 13 Decade
        Node( n1 n2 n3 ) ObservationNode( n3  ) Exclude ( v1 v2 )
        *CircuitNoise
        ACExtraction = "n@node@_equi"
        ## NoisePlot = "n@node@_equi"
){
        Poisson          Electron Hole Contact Circuit
 }

 Quasistationary(
  MaxStep=0.1 MinStep= 0.0001
  Goal { Parameter = v2.dc value = 3 }
  ){ Coupled { Poisson Electron Hole Contact Circuit} }

 Quasistationary(
  MaxStep=0.1 MinStep= 0.0001
  Goal { Parameter = v1.dc Voltage=1 }
  ){ Coupled { Poisson Electron Hole Contact Circuit} }



 NewCurrentPrefix = ""
 Transient (
   InitialTime=0 FinalTime=2e-6 InitialStep=1e-10 MaxStep=2e-7 MinStep=1e-14
Increment=1.3
   Plot { Range = (50e-9 @time@) Intervals = 10 }
 ){ ACCoupled(
        ACCompute( Time=(@<time+5e-9>@) )     *compute ac analysis 10 ns after the
transistor is off
      StartFrequency=1e0 EndFrequency=1e13 NumberOfPoints= 13 Decade
        Node( n1 n2 n3 ) ObservationNode( n3 ) Exclude ( v1 v2 )
      CircuitNoise
       ACExtraction    = "n@node@_tran"
      ## NoisePlot      = "n@node@_tran"
   ){
      Poisson Electron Hole Circuit Contact
   }
 }
}#end Solve
```