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A Software Defined Radio Platform with Direct Conversion: SOPRANO

Shinichiro Haruyama
SONY Computer Science Laboratories, Inc

Robert H. Morelos-Zaragoza
SONY Computer Science Laboratories, Inc, robert.morelos-zaragoza@sjsu.edu

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Abstract— **In this paper, a new software defined radio platform with multiport-based direct conversion is proposed, named SOPRANO (Software Programmable and Hardware Reconfigurable Architecture for Network). The main features of SOPRANO are a high-level design methodology for digital circuits, a new mixer-less direct conversion method, and software algorithms for multi-band and multi-mode operation. We built the first prototype SOPRANO 1.0, which was able to receive PSK and QAM signals with two different carrier frequencies at 2.45GHz and 5.25GHz by changing signal processing software.**

Keywords— **Software radio, direct conversion, multimode receiver, synchronization.**

I. Introduction

Due to recent advancements in hardware and software technologies, implementing software defined radio concept is becoming more realistic than ever before. One of the key functions of software defined radio is its multi-band and multi-mode operation. To implement that function, we need to have not only new RF circuits and high-speed digital circuits, but also a new design methodology and software algorithms. This paper describes a new design methodology and several algorithms for a new multi-port direct conversion technology.

II. Hardware Platform

A block diagram of the hardware platform is shown in Figure 1. The first prototype SOPRANO 1.0 has only receiver functions. The hardware consists of analog RF circuits and digital circuits. The analog RF circuits consist of antennae, RF LNAs, filters, and a multi-port junction MMIC, which is a mixer-less direct converter. The digital circuits consist of ADCs, DACs and digital signal processing circuits including FPGAs and a CPU.

III. Direct Conversion Based on Multi-Port Technology

A software defined radio receiver should be able to receive a wide range of frequencies and bandwidths. It is very difficult to achieve this using a conventional superheterodyne receiver, because of fixed analog circuits. In SOPRANO direct conversion is utilized, i.e., RF signals are downconverted to baseband signals in just one stage of mixing. The simpler structure of direct conversion receivers make them more suitable for a flexible software defined radio implementation. Moreover, direct conversion is performed without a mixer [1] [2]. A photograph of the proposed five-port junction MMIC is shown in Figure 2. Advantages of this direct conversion method include wide band reception capability and low power consumption. Some of the unique features of direct conversion using six-port technology include[3]: (i) Immunity to image frequency and adjacent channel interferences, relaxing the requirements of the channel selection filter; (ii) Tolerance to variations of the input power level, making the dynamic range to depend mainly on ADC resolution; (iii) Wideband operation. With proper calibration, I/Q imbalances, DC offset and adjacent channels interference have a smaller impact in performance in five-port direct converter, compared to a conventional mixer. One of the main contributions of this work is that digital calibration (and, subsequently, compensation of time-varying imperfections) is accomplished with the aid of adaptive digital algorithms. Nevertheless, the five-port direct converter shares the problems associated with other forms of direct conversion, such as flicker noise and DC offset. These problems can be alleviated through the use of a linear equalizer together with a spectrum shaping method by line coding, as proved recently in [5].

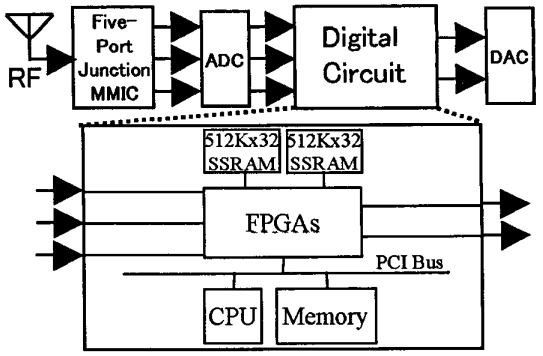

Fig. 1. Block diagram of SOPRANO platform

IV. Design Methodology

The methodology employed in SOPRANO has the goal of filling the gaps in the design process between communication engineers, usually performing top-level design and simulations of wireless communication systems using signal processing tools such as SPW, Matlab, or C, and hardware designers, typically designing circuits in RTL with languages such as VHDL or Verilog.

A design starts with C/C++ programs to do simulation of the target device. The C/C++ language models are

The authors are with Advanced Telecommunication Laboratory, SONY Computer Science Laboratories, Inc., Tokyo Japan. Email: haruyama & morelos@csl.sony.co.jp.

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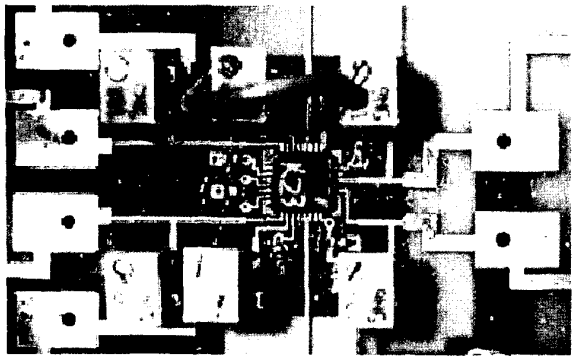

Fig. 2. Photograph of five-port junction MMIC

then modified with hardware implementation information and fed into a RTL synthesis tool along with user's design restrictions such as hardware resource requirement [6]. The synthesized RTL is sent to a logic synthesis tool to generate a netlist, which is then mapped, placed, and routed on an FPGA.

V. Algorithms

A Matlab Simulink model of the multiport direct-conversion receiver was developed. The model allows for key issues associated with this technology, such as the effects on the demodulated symbols of variations in components, to be identified. Novel algorithms were then developed in Matlab and C/C++ to compensate for these variations in the characteristics of the multiport device.

Besides the signal processing tasks usually required in a digital receiver, such as symbol and carrier recovery, the algorithms implemented in SOPRANO can be broadly categorized as (1) multiport specific (IQ computation and digital calibration) and (2) direct-conversion specific (DC offset and IQ imbalance compensation). In the following, the digital signal processing algorithms implemented in SOPRANO are briefly described.

A. Calculation of baseband in-phase and quadrature samples

Based on the five-port device power detector outputs, $V_j, j = 1, 2, 3$, the in-phase (I) and quadrature (Q) channel samples are computed as follows.

$$I = h_{I0} + h_{I1}V_1 + h_{I2}V_2 + h_{I3}V_3, \quad (1)$$

$$Q = h_{Q0} + h_{Q1}V_1 + h_{Q2}V_2 + h_{Q3}V_3, \quad (2)$$

Also, in order to give an optimum use to the ADC output quantization bits, or ADC dynamic range, a digital automatic-gain control (AGC) stage follows the IQ computation stage to ensure that the levels of the received I-channel and Q-channel samples are properly normalized with respect to the maximum range of the ADC. This is achieved by monitoring the average amplitudes of the samples and multiplying the incoming samples by a factor such that the average amplitudes lie approximately at 3 dB below the full scale. A photograph of the real-time constellation calculation of the QPSK signal is shown in Figure 3.

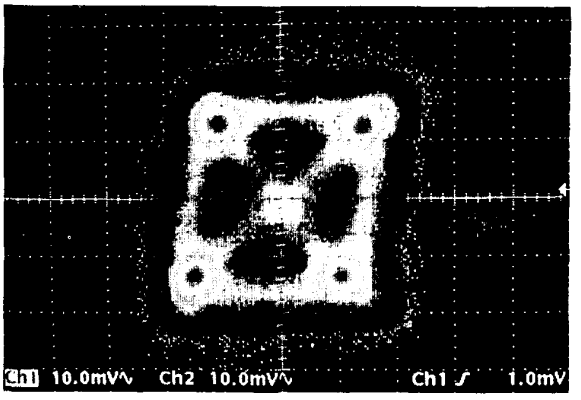

Fig. 3. Real-time constellation of a demodulated QPSK signal

B. DC Offset Compensation

In direct-conversion receivers, DC offsets is caused, among others, by LO leakage and interfering signals and can be removed partially in the RF front end through proper design. Any residual dynamic DC offset is corrected in the digital domain by removing the average values of the I-channel and Q-channel samples.

C. IQ Imbalance Compensation

Due to mismatches in the characteristics of the power detectors used in the multiport device, an imbalance between the I-channel and Q-channel symbols may be present. To compensate for this imbalance, a novel digital calibration and compensation algorithm has been developed and implemented. The algorithm adaptively modifies the ADC inputs from two of the power detectors, those associated with the sum and difference of phase-shifted versions of the local signal and the incoming RF signal, in order to minimize the IQ imbalance.

D. Multi-band and Multi-mode Capability

The goal of the current version of SOPRANO is to implement a multiple-band and multiple-mode digital receiver for a narrow band system operating in two different carrier frequencies (2.45 GHz and 5.25 GHz) with different modulation modes (BPSK, QPSK, 8PSK, 16QAM and 64QAM). To this end, a blind carrier recovery technique aided by modulation identification was developed and implemented in the platform. The technique combines a conventional digital PLL structure with a modulation identification algorithm. This technique is a modulation identification (ID) method that is robust against phase and frequency offsets. The phase error detector characteristics of this *multiple-mode digital PLL* are reconfigured based on the information produced by a bank of phase-lock detectors (PLD) and a novel ID logic [7]. The proposed modulation ID technique

allows to implement a receiver architecture that first acquires the signal in blind mode and then tracks the signal in decision-directed mode. Figures 4 to 7 show snapshots of experimental results of 100 recovered constellation symbols, after IQ computation, gain and DC adjustment, and timing recovery, at a carrier frequency of 5.25 GHz.

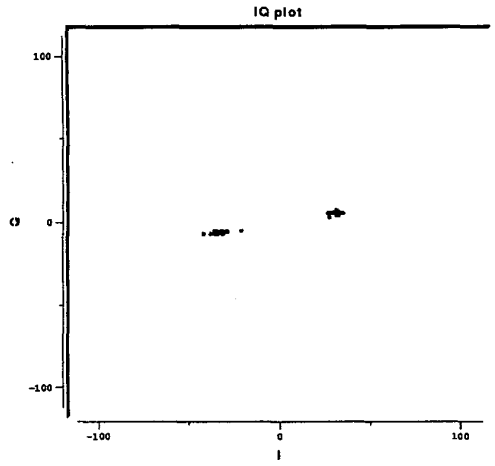

Fig. 4. Demodulated BPSK constellation after timing recovery

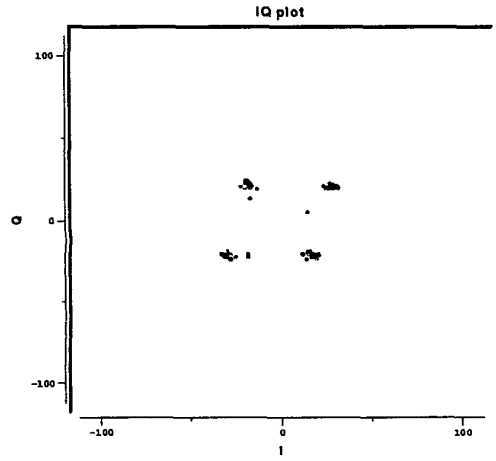

Fig. 5. Demodulated QPSK constellation after timing recovery

VI. Conclusion

In this paper, a new software defined radio platform was introduced. SOPRANO features a direct conversion method based on a five-port junction MMIC, a high-level design methodology, and novel algorithms for multi-band and multi-mode operation. Both multi-band operation and multi-mode capability have been verified experimentally. The proposed high-level design methodology makes the SOPRANO platform very suitable for software defined radio prototyping.

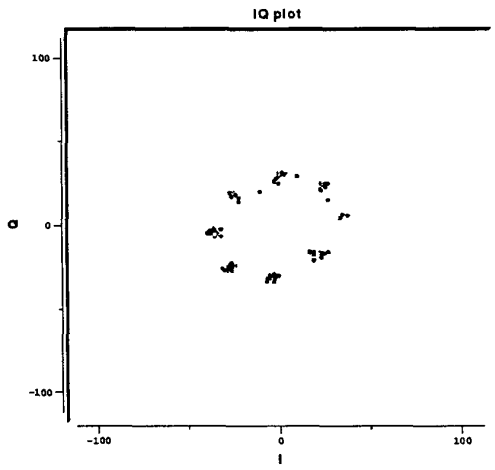

Fig. 6. Demodulated 8PSK constellation after timing recovery

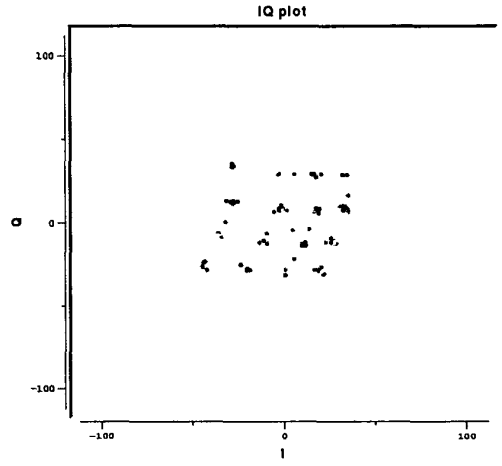

Fig. 7. Demodulated 16QAM constellation after timing recovery

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