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Method of Non-Data-Aided Carrier Recovery with Modulation Identification

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SUMMARY A non-data aided carrier recovery technique using digital modulation format identification called multi-mode PLL (Phase Locked Loop) is proposed. This technique can be interpreted as a modulation identification method that is robust against static phase and frequency offsets. The performance of the proposed technique is studied and the analytical expressions are derived for the probability of lock detection, acquisition time over AWGN channel in the cases of M-PSK and M-QAM modulations with respect to frequency offset and signal-to-noise ratio.
key words: Software Defined Radio, Carrier Recovery, Digital PLL, Modulation Identification

1. Introduction

Recently, a multimode transceiver, known as Software Defined Radio (SDR) is receiving much attention in the wireless communication field [1]. Such multiple functions in the physical layer of a SDR can be configured such that modulation scheme, data rate, coding scheme and so on. Specifically, multiple modulation schemes can be considered for adaptive modulation or hierarchical modulation [2]. Thus such a multimode transceiver, a function to identify a change operation is necessary.

For this problem, there are two main approaches, which can be classified as the non-blind and the blind techniques. The non-blind approach employs supplementary information to identify the mode change. On the other hand, in the blind approach, there are some identification algorithms instead of using such a supplementary information. In fact, this approach can be considered as a concept in wireless communication, since it presents the possibility of realizing a universal transceiver, which does not require supplementary information, and estimates the environment to reconfigure to the optimum configuration still on research.

For the multimode transceivers, this paper proposes a "Multimode PLL" which can achieve not only carrier recovery but also blind modulation identification. In [3], a technique based on fourth-order cumulants was proposed to identify modulation formats, and shown to be robust against carrier frequency and phase offsets. However, the complexity in [3] is an important problems, because it uses high order moments as parameters. In addition, the applications are not given in [3]. In [4] and [5], the SDR is considered as an application of the modulation identification techniques. In [4], the assumed modulation type is only M-PSK. For the frequency and phase offset, this paper uses a technique similar to differential detection, therefore there is deterioration in the SNR.

On the other hand, in [5] the nearest neighbor rule is employed for the modulation identification. However, [5] assumes that carrier synchronization is perfect. The method of modulation identification proposed in this paper can also handle frequency and phase offset, through the use of a conventional digital phase-locked loop (PLL) [6] and a modulation identification algorithm. In addition, a future plan to apply the proposed method to the Adaptive Modulation Scheme (AMS), means that not only M-PSK but also M-QAM can be considered [2]. However, in this paper the basic characteristics and effectiveness of the multimode PLL are shown without AMS.

The parameters of the PLL, such as the Phase Error Detector (PED) characteristics, are reconfigured based on the information produced by a bank of Phase-Lock Detectors (PLD) and an identification (ID) logic. Thus, this PLL is referred to as a *multiple-mode digital PLL*. This paper focuses on carrier recovery synchronization, here perfect symbol timing is assumed. Under frequency and phase offsets, the identification logic needs to be designed such that the modulation format is successfully identified even if the constellations are rotating. Thus, the ID logic used in [7] was modified by adding more hit counters associated to specific sectors in the lock areas. The proposed technique does not exclude the use of other modulation ID approaches [3].

Therefore, the main contribution of this paper is to introduce the multimode PLL as one of the blind approaches focusing on consumer wireless communication, e.g. AMS. The advantages of the blind approaches, which were shown previously, are included in the multimode PLL. In fact, since in consumer wireless communication carrier synchronization has to be considered, the contribution of this paper is to consider not only modulation identification but also carrier synchronization by using the PLD. It is used for detecting of carrier lock as well as modulation identification. The mul-

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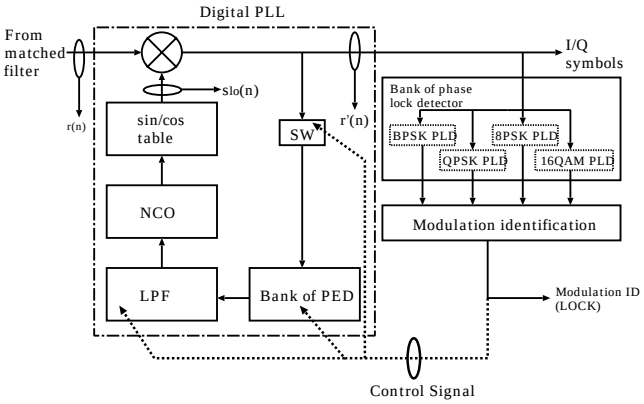

Fig. 1 Multimode PLL

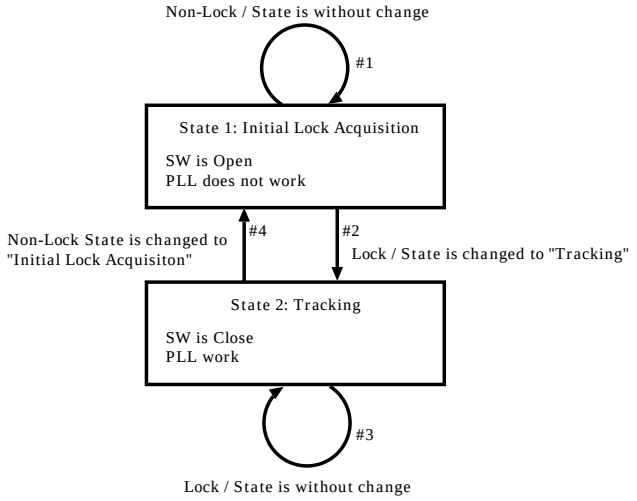

Fig. 2 State transition model

timode PLL is therefore every useful in the consumer wireless communication, compared the proposals in [3]-[5]. This is a very desirable feature in a consumer software radio receiver. Moreover, the proposed multiple-mode carrier recovery scheme has less complexity that using cumulants (fourth-order statistics) [3]. Furthermore the basic performance characteristics of the multimode PLL are obtained theoretically. This includes the maximum frequency offset, the lock rate, the acquisition time, modulation identification success rate and so on. Comparing with [3], the modulation identification ability is equivalent to the ideal environment which has no frequency and phase offset. In addition, this paper also pays attention to the acquisition time or how fast the multimode PLL can lock the phase and identify the modulation scheme.

The most important advantage of this proposal is the acquisition time is expected to be much shorter than the case where the carrier recovery and the modulation identification work separately. This is because in the multimode PLL, carrier recovery and modulation identification are done at the same time.

The rest of this paper is organized as follows. In section II the system model is shown where the configuration of the multi-mode PLL and the modulation identification logic is discussed in detail. The theoretical analysis and performance results of the multi-mode PLL are presented in section III. The conclusions are drawn in section IV.

2. System model

In this section, the system model and assumptions are discussed. Firstly, the multimode-PLL operation is explained, and the modulation identification logic is described afterwards.

2.1 A multiple-mode digital PLL [8]

A simplified block diagram of the proposed multi-mode PLL is shown in Fig.1, where the two main functions, modulation identification and carrier recovery are illustrated. *SW* denotes a switch that opens or blocks the carrier recovery loop. Here, NCO is a Numerically Controlled Oscillator that outputs the signal $s_l(n)$ used to cancel the frequency offset. The received complex baseband signal $R(t)$ is shown with continuous-time value as follows,

$$R(t) = \exp[-j(\phi + 2\pi\Delta f t)] \sum_{i=-\infty}^{\infty} s(i)H(t - iT_s) + g(t), \quad (1)$$

where ϕ, Δf and $H(t)$ are the phase offset, the frequency offset and channel impulse response, respectively. ϕ is the initial phase offset, which is the phase difference between the received signal and the correct constellation position. Here, $s(i)$ is the i-th symbol baseband data, T_s is the symbol interval, and g(t) is Additive White Gaussian Noise (AWGN). We consider perfect equalization and time synchronization. Since, there is no multi-path and amplitude distortion is compensated for by normalizing the amplitude to 1, we can assume $H(t) = 1$. Therefore the n-th received symbol $r(n)$ interval $t \in [(n-1)T_s, nT_s)$ is given by

$$r(n) = \exp[-j(\phi + 2\pi\Delta f T_s n)]s(n) + g(n) \quad (2)$$

Let Δf be small compared to the symbol rate R_s, so that the received signal lies within the capture range of the digital PLL. This condition is equivalent to $\Delta f T_s << 1$, where $T_s = 1/R_s$. Equivalently, this result can be applied to single-carrier narrow-band systems, as well. Let the *normalized frequency offset* be equal to $\Delta f T_s$. From equation (2) the received points $r(n)$ rotate at an angular speed of $2\pi\Delta f$ radians every T_s seconds with respect to the phase ϕ. In the modulation identification logic, such symbol rotation has to be

taken into consideration, therefore, the PLL works to cancel such a symbol rotation. Furthermore, the PED and Low Pass Filter (LPF) are designed to adapt to the transmitted modulation format. In this system the possible modulation schemes are BPSK, QPSK, 8PSK and 16QAM. Therefore, the modulation identification logic allows the frequency and phase offset. This system operates in two states, (1) initial lock acquisition and (2) tracking, as shown in Fig. 2. The initial state (1) is the Initial Lock Acquisition state, where the switch SW is open and the incoming signal symbols rotate with *normalized frequency offset* $\Delta f T_s$. The carrier lock detection, obtained by using the bank of PLDs, works in a window of size N symbols. The PLDs output is either "1" or "0" meaning "Lock" or "Non-LOCK", respectively. If any PLD outputs "1", the modulation identification logic obtains the modulation identification result using outputs of the PLDs. Upon successful identification of the modulation type, the state is changed to (2). The PLL parameters, which are PED and LPF, are reconfigured to adapt the modulation format and SW is closed so that the PLL can start to work. If every PLD outputs "0", the state does not change, and window the bank of PLDs work for initial acquisition in the next. In state (2), the bank of PLDs and modulation identification logic still play a role in the tracking stage, by monitoring the carrier recovery subsystem through the lock. If lock is lost in state (2), the state is changed back to the initial lock acquisition state (1) and SW is open.

2.2 Modulation identification under frequency/static phase offsets

In this section, we introduce the modulation identification logic under frequency/static phase offsets [7]. The modulation identification in Fig. 1 is realized by the "PLD block" & "Modulation identification block". Since the modulation identification has the critical relationship with the processing of the PLDs, at first the PLD processes are described. The main purpose of the PLD process is to detect lock the carrier. Each PLD is composed of a lock area, non-lock area, and counter.

The particular size of phases and lengths of the PLDs in the complex plane (signal space) are shown in Fig. 3, focusing on the first quadrant. The PLDs are prepared for every modulation scheme. The function of the PLDs is to detect "Phase Locked" state which represents the condition that almost of the received signals, in the I-Q plane, are near a constellation point. (I and Q represent the in-phase and quadrature components, respectively.) On the other hand, the difference between modulation schemes is the constellation positions. Since the modulation identification algorithm uses the concept that each modulation scheme has different constellation position, the phase lock logic can be used modulation identification. Our proposed scheme

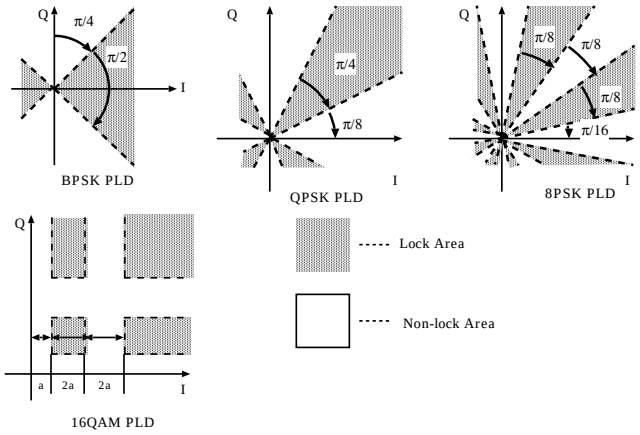

Fig. 3 Each Phase Lock Detectors (PLD) configuration

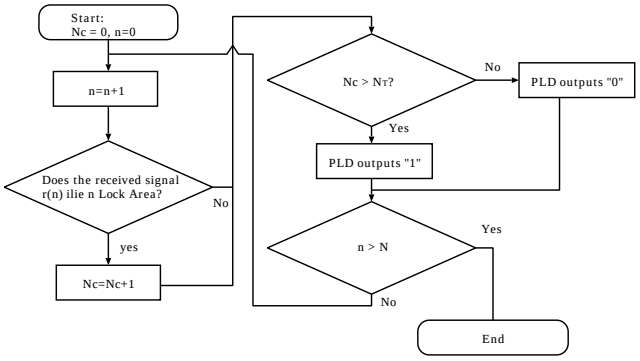

Fig. 4 PLD logic flow chart

uses this idea in the modulation identification logic. The phase lock process operates window by window. For one window, duration time n $(0 < n < N-1)$ each PLD's counter counts the number of symbols in the lock area and outputs as N_C^{MOD}, where MOD denotes the modulation scheme. To detect the "Lock" state, the PLDs use the common threshold value N_T as a criteria. When observing over one window, if N_C^{MOD} is greater than N_T, PLD of MOD outputs "1" meaning "Lock", else outputs "0" meaning "Non-Lock". Moreover, during the processing, if one PLD output "1", the process in that window will be stopped. In the next window, the same process is iterated independently of the state condition. In Fig. 4 the process of PLD is shown in detail. The phase uncertainty used in this phase lock algorithm presented in this paper is different from that typically used in conventional phase lock algorithm. By using training signals, the general phase lock can definitely cancel the phase offset and correctly demodulate the signals. On the other hand, the multimode PLL uses the blind signal process, therefore, there are no training signals. In addition, the purpose of this processing is modulation identification, hence, the correct phase position is not necessary to demodulate the signal

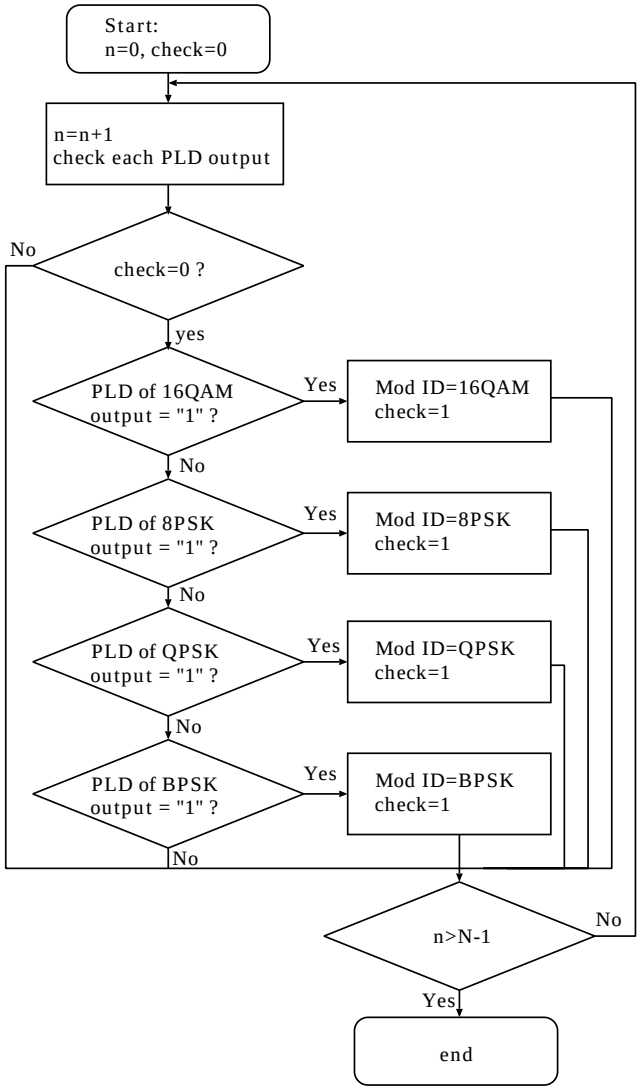

Fig. 5 Modulation identification logic flow chart

correctly. In fact, the multimode PLL M-ary PSK can tolerate integral multiples of $2\pi/M$ phase offset from the correct constellation positions, while in 16QAM, $\pi/2$ phase offset from the correct constellation position can be tolerated. The above conditions on the phase offset are enough to identify the modulation schemes.

In multimode PLL, the modulation identification logic identifies the modulation scheme by monitoring the outputs of the PLDs. The modulation identification result corresponds to the PLD that has output "1" and breaks possible ties with other modulation schemes with a PLD output "1".

A detailed schematic diagram of the modulation identification logic is shown in Fig. 5. This process is performed on each window independently. As shown in Fig. 5 the modulation identification orders used in this scheme are 16QAM, 8PSK, QPSK and BPSK. In fact, this order has an influential effect on the modulation identification ability. The objective of this paper is to demonstrate the basic ability and characteristics of the multimode PLL. The modulation identification order is understood to be a considerable future subject. The modulation identification result corresponds to the PLD that has output "1". Once a modulation scheme has been identified, the identified scheme is kept as the result along the window. There is an important difference between a successful "Lock" and a successful "Modulation Identification". A successful "Lock" means that the PLD of MOD outputs a "1" in a window under the condition that the transmitted signals are modulated by MOD. However when "Lock" becomes successful, "Modulation Identification" is still possibly a fail, because, if the PLD of another modulation scheme outputs "1" before MOD, this modulation scheme will get priority over MOD. The definition of successful "Modulation Identification" is that the modulation identification result is MOD under the condition that the transmitted signals are modulated by MOD.

As described above, this paper proposes a simple multimode PLL which has a capability to improve its characteristics by considering the design of PLDs and modulation identification logic.

3. Performance analysis

It is important to observe that there is a delicate balance among the frequency offset ΔfT_s, the signal-to-noise ratio per symbol, E_s/N_0, and the size of the observation window, N. At low E_s/N_0, the value of N should be set as high as possible, as done in [4], [5] and [7], in order to average out the effects of additive noise. At the same time, however, N is limited by the value of ΔfT_s. That is, if ΔfT_s is relatively large, then N needs to be small enough, adversely, if N is not small enough, received signals in the I-Q plane are plotted as only a circle in each PSK modulation schemes. In the same way, the threshold N_T needs to be designed to adapt the ΔfT_s and E_s/N_0.

3.1 Maximum frequency offset

This section deals with the estimation of the maximum frequency offset for which the signals can be recovered, under the assumption that no AWGN is added to the received signals. To design N and N_T, we set two-level maximum frequency offsets denoted as $(\Delta fT_s)_{\max,\mathrm{N}}$ and $(\Delta fT_s)_{\max,\mathrm{N_T}}$, respectively. To compare the multimode PLL with [3], the maximum frequency offset $(\Delta fT_s)_{\max,\mathrm{N}}$ is set to be 0.001. $(\Delta fT_s)_{\max,\mathrm{N}} = 0.001$, so as to certify the reliable employment of multimode PLL in the situation where the maximum frequency offset $(\Delta fT_s)_{\max,\mathrm{N}}$ is less than 0.001. In addition, the narrowest angular range Φ among the lock areas is, that in 16QAM $\Phi_{16QAM} \cong \pi/10$. By using two parameters

Table 1 Maximum frequency offset with a threshold of 27 symbols

MOD	Φ (deg)	$(\Delta f T_s)_{\max,\mathrm{N_T}}$
BPSK	90	0.00926
QPSK	45	0.00463
8PSK	22.5	0.00231
16QAM	17.8	0.00183

$(\Delta f T_s)_{\max,\mathrm{N}} = 0.001$ and $\Phi_{16QAM} \cong \pi/10$, the observation window size is obtained,

$$N = \frac{\Phi_{16QAM}}{2\pi\,(\Delta f T_s)_{\max,\mathrm{N}}} = 50 \tag{3}$$

On the other hand, to design N_T, we have to consider the modulation identification ability, acquisition time, and the transition states. In this paper, N_T is set to 27 by empirical rule. We in fact plan to fit the multimode PLL into the AMS, thus, the range of Es/No where the multimode PLL can lock the phase with practicable threshold N_T is desired. For this reason, N_T is set to 27, however, N_T can be easily changed. If we consider the concrete application of the multimode PLL, then N and N_T can be optimized.

Unlike N, N_T determines the maximum frequency offset $(\Delta f T_s)_{\max,\mathrm{N_T}}$ which precludes the phase lock. Note that the phase increment between symbols equals $2\pi\Delta f T_s$ radians. Consequently, $(\Delta f T_s)_{\max,\mathrm{N_T}}$ is given by

$$(\Delta f T_s)_{\max,\mathrm{N_T}} = \left(\frac{\Delta f}{R_s}\right)_{\max,\mathrm{N_T}} = \frac{\Phi}{2\pi N_T}, \tag{4}$$

where $T_s = 1/R_s$ is the symbol interval. It follows that the maximum frequency offset $(\Delta f T_s)_{\max,\mathrm{N_T}}$ sets an upper bound on the value of N_T. The larger the value of $(\Delta f T_s)_{\max,\mathrm{N_T}}$, the smaller the value of N_T, and vice-versa. Table 1 shows the values of $(\Delta f T_s)_{\max,\mathrm{N_T}}$ with a threshold $N_T = 27$, for the four modulations of interest in this paper.

Meanwhile, the minimum carrier offset $(\Delta f T_s)_{\min}$ can be obtained by defining the required maximum acquisition time T_{req} window which represents the limited time that the multimode PLL has to acquire the carrier lock. By using T_{req}, $(\Delta f T_s)_{\min}$ is expressed as follows;

$$(\Delta f T_s)_{\min} = \frac{\Psi}{2\pi(T_{req}N - N_T)} \tag{5}$$

Here, Ψ is the widest angular range among the non-lock area. Ψ depends on the type of the modulation scheme. In PSK, $\Psi = \Phi$ shown in Table 1, and in 16QAM, $\Psi \cong \pi/2$. The variable T_{req} is dependent on the application, consequentlly, this paper shows the acquisition time instead of the required acquisition time T_{req} in section 3.3.

3.2 Probability of lock detection under frequency offsets

In this section, the probability of lock detection of each PLD is analyzed under the assumptions of perfect symbol timing and equalization (i.e., no fading). Let $\Delta\theta = 2\pi\Delta f T_s$ and consider a received symbol $s(0)$ at the beginning of an observation window of length N symbols. Let ψ denote the phase of $s(0)$. If $|\Delta_f| \neq 0$, as mentioned above, subsequent symbols will "rotate" at a speed of $\Delta\theta$ radians per symbol. Therefore, the i-th symbol within the observation window, $0 \leqq i < N$, will experience a phase rotation equal to $i\Delta\theta$ with respect to $s(0)$. Recall that lock detection is successful if the number of received symbols inside the lock area is greater than a threshold value N_T over the observation window of length N symbols.

For the sake of presentation, a bound on the probability of lock detection is derived below for BPSK modulation, as a function of the phase of the first received symbol $s(0)$, the normalized angular frequency offset $\Delta\theta$, and the signal-to-noise ratio per symbol E_s/N_0. Let $\Pr\{\mathrm{s(i)} \in \mathcal{L}|\psi\} \triangleq \mathrm{p_i}$ denote the probability that the i-th received symbol, $s(i)$, lies inside the BPSK lock area, denoted $\mathcal{L}$, given that the initial symbol has a phase ψ, can be lower bounded as

$$p_i \geqq \acute{p_i} = 1 - \left[Q\left(\sin(\pi/4 - (\psi + i\Delta\theta))\sqrt{\frac{E_s}{N_0}}\right) + Q\left(\sin(\pi/4 + (\psi + i\Delta\theta))\sqrt{\frac{E_s}{N_0}}\right)\right], \tag{6}$$

where $Q(x)$ and $\acute{p_i}$ are the Gaussian Q-function and an approximation of p_i ,respectively.

The probability $P_o(M,\psi)$ that M symbols lie outside of the lock area $\mathcal{L}$, given an intial phase ψ, is $P_o(0,\psi) \approx \prod_{i=0}^{N-1} \acute{p_i} = \gamma$, and

$$P_o(M,\psi) \approx \acute{P}_o(M,\psi) = \sum_{a_0=0}^{N-1-(M-1)} \sum_{a_1=a_0+1}^{N-1-(M-2)} \cdots \sum_{a_j=a_{j-1}+1}^{N-1-(M-1-j)} \cdots \sum_{a_{M-1}=a_{M-2}+1}^{N-1} \gamma \prod_{\ell=0}^{M-1} q_{a_\ell}, \quad M \geqq 1, \tag{7}$$

where $a_{-1} \triangleq 0$, $\acute{P}_o(M,\psi)$ is an approximation of $P_o(M,\psi)$ and q_{a_ℓ} is shown by using (6) as follows,

$$q_{a_\ell} \triangleq \frac{(1 - \acute{p_{a_\ell}})}{\acute{p_{a_\ell}}}. \tag{8}$$

From Eqs. (6) to (8), the probability of lock, i.e., the probability that up to $N - N_T$ symbols lie outside of region $\mathcal{L}$, given the initial phase ψ, is approximated as

$$\Pr\{\text{Lock}|\psi\} \approx \sum_{i=0}^{N-N_T} \acute{P}_o(i,\psi). \tag{9}$$

Note that $\Pr\{\text{Lock}|\psi\}$ is a random variable that depends on ψ. Integrating over the probability density function of the initial phase ψ, leads to the following expression for the probability of lock detection

$$\Pr\{\text{Lock}\} \approx \int_0^{2\pi} \sum_{i=0}^{N-N_T} P_o(i,\psi) p_\psi(\psi)\, d\psi. \tag{10}$$

Assuming a uniform distribution on the value of the initial phase ψ, expression (10) can be written as

$$\Pr\{\text{Lock}\} \approx \frac{1}{2\pi} \sum_{i=0}^{N-N_T} \int_0^{2\pi} P_o(i,\psi)\, d\psi. \tag{11}$$

The bound (11) was evaluated numerically (Monte Carlo integration) and is plotted versus E_s/N_0, for several values of normalized frequency offset, in Fig. 6. A similar argument holds for QPSK and 8-PSK modulations. The results are shown in Figs. 7 and 8. In the case of 16-QAM, the expression for p_i becomes more involved, as it depends on the particular type of symbol being received, i.e., inner, wall or corner. Also note from the plots that, at high E_s/N_0, the probability of lock approaches a constant value greater than or equal to 0.5. The value of the constant can be computed for BPSK modulation, with reference to Fig. 10, as follows.

First consider the case with no frequency offset, $|\Delta f| = 0$. Given a random initial phase ψ with uniform distribution in the range $[0, 2\pi)$, the probability of lock is simply the ratio of the volumes of the lock area to the total two-dimensional Euclidean space $\mathcal{R}^2$, i.e., $\Pr\{\text{Lock}\} = \pi/2\pi = 0.5$. For the case of $|\Delta f| \neq 0$, at high E_s/N_0 values, recall that $\Pr\{\text{Lock}\}$ equals the probability that at least N_T symbols lie inside the lock area. Consequently, up to $(N - N_T)$ symbols can lie outside the lock area just before or after its boundary. The lock area angular range increases by $\Theta_2 = (N - N_T)2\pi\Delta f T_s$ (see Fig. 10.) Therefore, in the first quadrant, the normalized area of the lock region increases from $\Theta_1 = \pi/4$ to $\Theta_1 + \Theta_2 = \pi/4 + (N - N_T)2\pi\Delta f T_s$. As a result, at high E_s/N_0, the probability of lock tends to be a constant value

$$\Pr\{\text{Lock}\} \to \frac{1}{2} + 4(N - N_T)\Delta f T_s. \tag{12}$$

As an example, for $\Delta f T_s = 0.001$, $N = 50$ and $N_T = 27$, $\Pr\{\text{Lock}\} \to 0.592$. For other modulation formats, similar results can be obtained in a straight forward manner. For 16-QAM modulation, at high E_s/N_0 and in the absence of frequency offset, the probability of lock, averaged over ψ, equals 0.26.

3.3 Acquisition Time

Assuming a uniform distribution on the value of the initial phase offset ψ, the acquisition time averaged with the initial phase offset is denoted T_a which can be written as

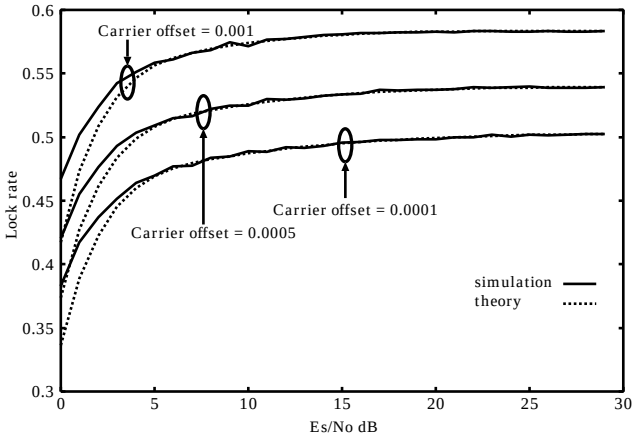

Fig. 6 Analytical and simulation results of the probability of lock with BPSK modulation for various values of normalized frequency offsets.

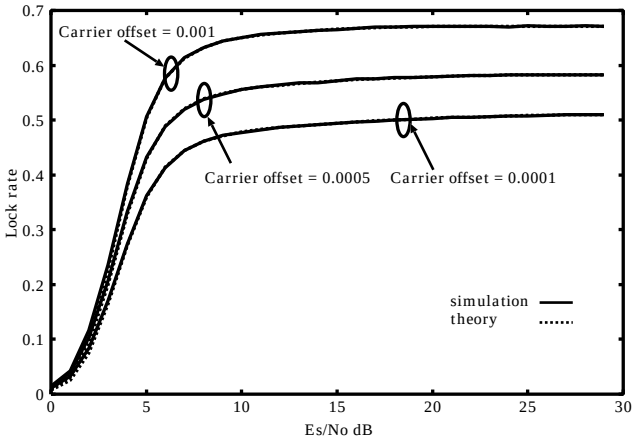

Fig. 7 Analytical and simulation results of the probability of lock with QPSK modulation for various values of normalized frequency offsets.

$$T_a = \frac{1}{2\pi} \int_0^{2\pi} t_a(\psi) d\psi \tag{13}$$

where $t_a(\psi)$ is acquisition time when initial phase offset is ψ. By using the lock probability $P_o(M,\psi)$, $t_a(\psi)$ can be expressed as

$$\begin{aligned} t_a(\psi) &= P_o(M,\psi) + \sum_{i=2}^{N_{max}} i P_o(M, N(i-1)\Delta\theta + \psi) \\ &\quad \Pi_{j=1}^{i-1}(1 - P_o(M, N(j-1)\Delta\theta + \psi) \\ N_{max} &= \infty \end{aligned} \tag{14}$$

To try to obtain the correct $t_a(\psi)$, N_{max} has to be ∞, however, it is impossible in practical, therefore, here, large enough N_{max} which are $N_{max} = 100$ in the case of

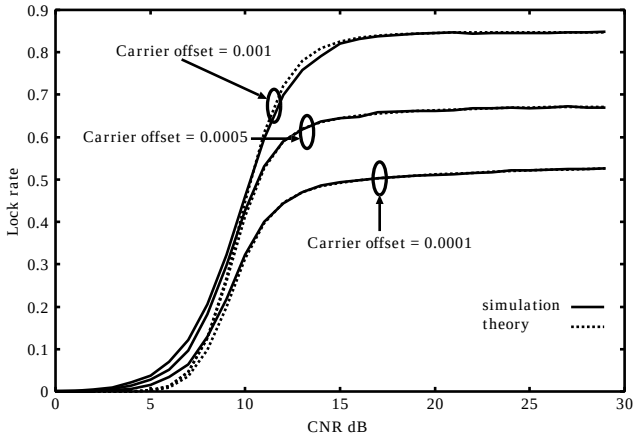

Fig. 8 Analytical and simulation results of the probability of lock with 8PSK modulation for various values of normalized frequency offsets.

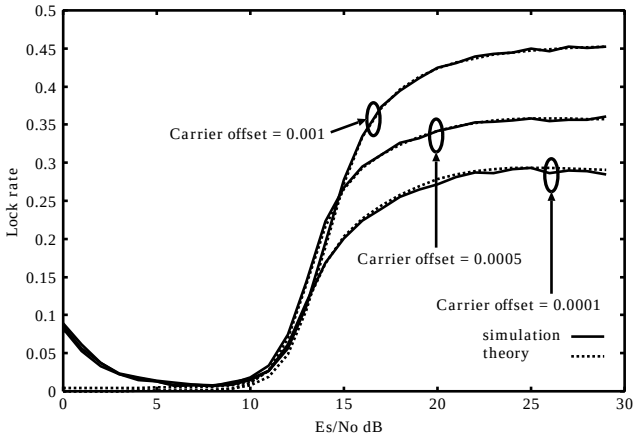

Fig. 9 Analytical and simulation results of the probability of lock with 16-QAM modulation for various values of normalized frequency offsets.

BPSK, QPSK and 8PSK, and $N_{max} = 400$ in 16QAM are used in the results shown in Figs. 11- 14. The theoretical value of the acquisition time Eq. (13) and the simulation results are evaluated, versus Es/No, for several values of normalized frequency offset in Figs. 11- 14. The Acquisition time depends on two parameters: The frequency offset and the phase difference between the adjacent lock areas. The conditions that the frequency offset becomes larger or the phase difference between the adjacent lock areas becomes smaller make the acquisition time shorter. The value of frequency offset and of phase difference between the adjacent lock area affect the rotation speed of the received signals and the maximum from the received signal position to the lock area, respectively. It can be said that, in this multimode PLL, by the previous discussion, there is a desirable frequency offset characteristic corresponding to acquisition time as shown in Fig. 15, where

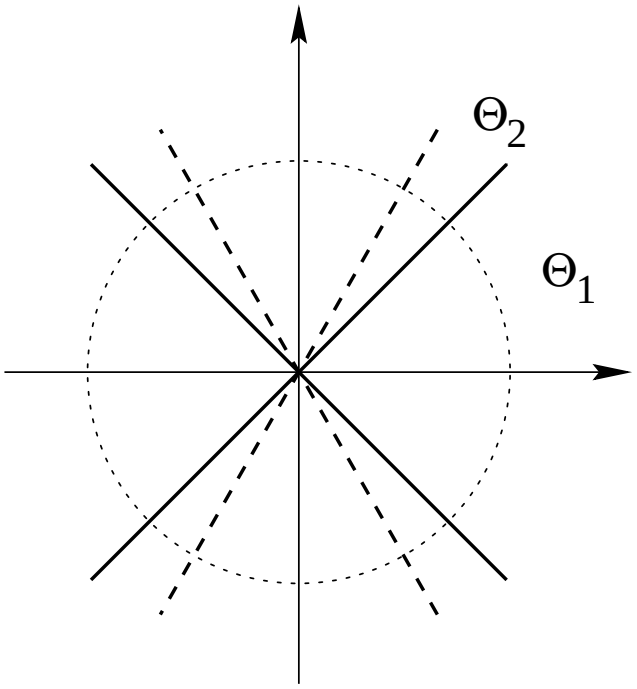

Fig. 10 Illustration of extended range of lock area due to frequency offset for BPSK modulation: $\Theta_1 = \pi/4$ and $\Theta_2 = (N - N_T)2\pi\Delta f T_s$.

$Es/No = 20dB$, and the frequency offset is less than $(\Delta f T_s)_{\max,\mathrm{N}}$. Note and that, when the frequency offset value is close to $(\Delta f T_s)_{\max,\mathrm{N}}$, the acquisition time is minimum.

To compare the proposal with the modulation identification ability of [3], Fig. 16 shows the lock probability and Fig. 17 shows modulation identification success rate. We note, that the comparing the proposed modulation identification algorithm with the conventional algorithms is quite difficult, because, in general, the conditions , i.e. the application, the calculated amount, the channel model, the modulation scheme, are different for each modulation identification algorithm. Therefore, in this paper, a specific case from [3] is used. In this case the modulation schemes assumed are BPSK, Pulse Amplitude Modulation(PAM)4, 8PSK, and QAM(4,4). It is further assumed that there is no frequency and phase offset, the observation period is 100 symbols and the correct modulation identification success rate does not attain 1 even if SNR is greater than $15dB$. On the other hand, in Fig. 17, in the region where Es/No is greater than $20dB$, the average "Modulation identification success rate" for all modulation schemes is close to 1 as it is in [3]. In the region where Es/No is greater than $25dB$ the "Modulation identification success rate" for all modulation schemes are 1, note that, the observation period is 50 symbols which is less than in [3]. In conclusion, the modulation identification ability is approximately

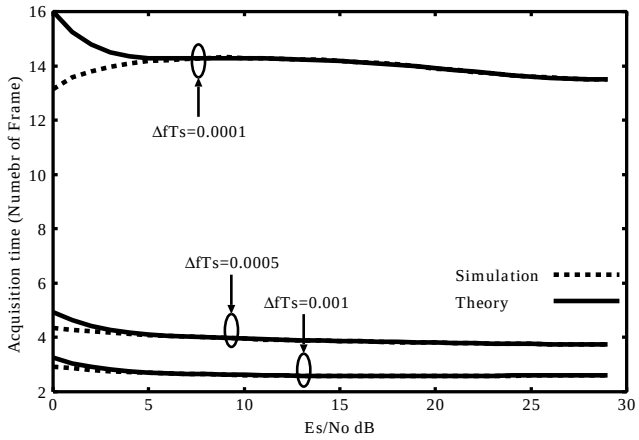

Fig. 11 Es/No vs Acquisition time in BPSK, $\Delta fT_s = 0.0001, 0.0005, 0.001$

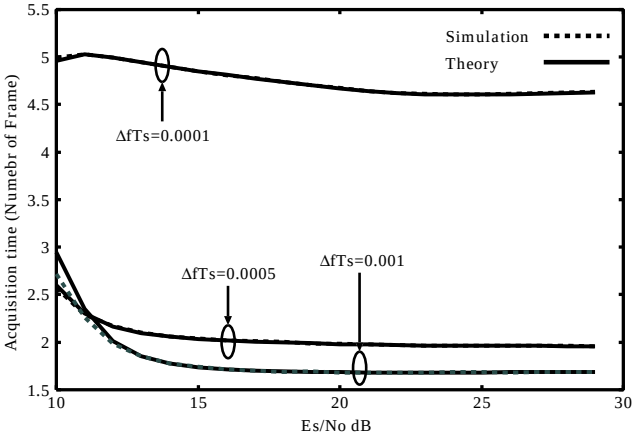

Fig. 13 Es/No vs Acquisition time in 8PSK, $\Delta fT_s = 0.0001, 0.0005, 0.001$

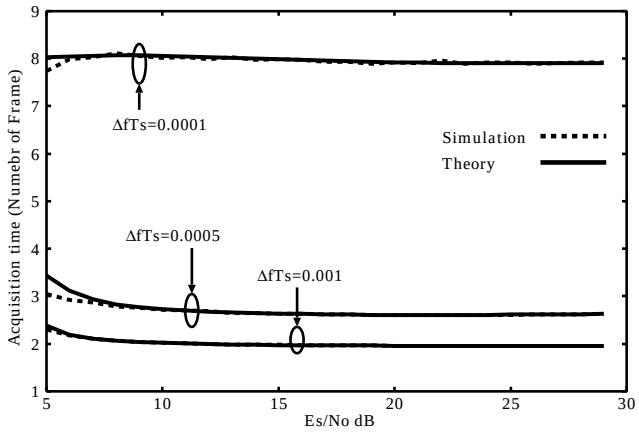

Fig. 12 Es/No vs Acquisition time in QPSK, $\Delta fT_s = 0.0001, 0.0005, 0.001$

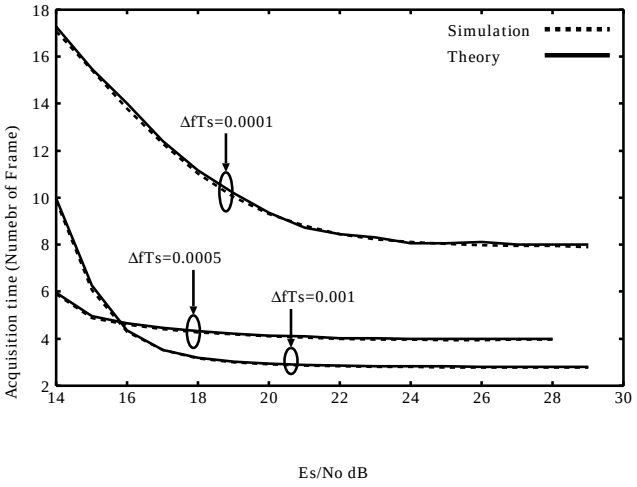

Fig. 14 Es/No vs Acquisition time in 16QAM, $\Delta fT_s = 0.0001, 0.0005, 0.001$

equivalent to [3] in the described conditions.

Fig.16 shows that the "Lock rate" of all modulation schemes is "1" in the region where Es/No is greater than $15dB$. The logic of the modulation identification and carrier lock are simpler to that in [3], therefore, by improving the modulation identification logic, the "Modulation identification success rate" can be made close to the "Lock rate". This shows that the multimode PLL has the capability to improve itself.

3.4 Dynamic behavior of carrier recovery with changes in the modulation format

The dynamic behavior of the processes of lock detection and modulation identification has been studied by means of simulations and experimental tests. Figs. 18 and 19 show simulation results of four modulation schemes with normalized frequency offset ΔfT_s equal to 0.001 and 0.0025, respectively, and $E_s/N_0 = 27$ dB. Each modulation was transmitted over 600 consec-

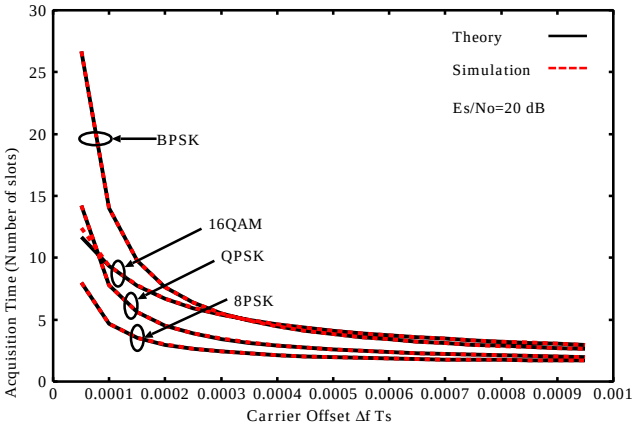

Fig. 15 Carrier offset vs Acquisition time, Es/No=20dB

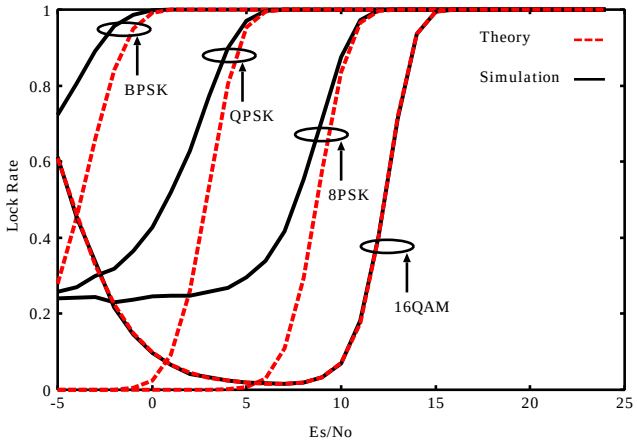

Fig. 16 Lock probability vs Es/No , initial phase offset and carrier offset is zero

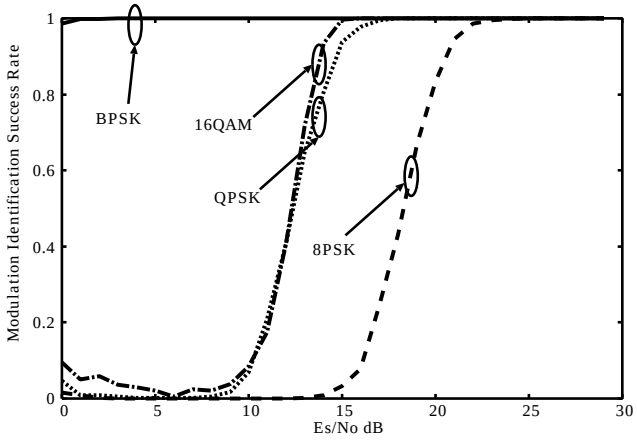

Fig. 17 Es/No vs Modulation identification success rate, initial phase offset and carrier offset is zero

utive symbols for a total of 2400 symbols. The initial phase of the constellations was chosen randomly. The transmission order was BPSK, QPSK, 8PSK and 16-QAM. From the figures, the signal labeled 'MOD' denotes the modulation format received (1=BPSK, 2=QPSK, 3=8PSK and 4=16-QAM). The signal labeled 'ID' refers to the identified modulation scheme, with '0' indicating no lock condition. The signals I_{in} and I_{out} refer to the received and recovered in-phase component of the symbols, i.e., the real part of the received complex baseband symbols. By symmetry of the constellations, and assuming equally likely transmitted symbols, similar curves were obtained for the quadrature component. It is noted that the results in Fig. 16, 17 are only instantaneous results which are obtained from the long temporal results.

For a normalized frequency offset $\Delta f T_s = 0.001$, all the modulations were successfully identified and locked. However, when the offset was increased to 0.0025, the 16-QAM signal could no longer be identified and recov-

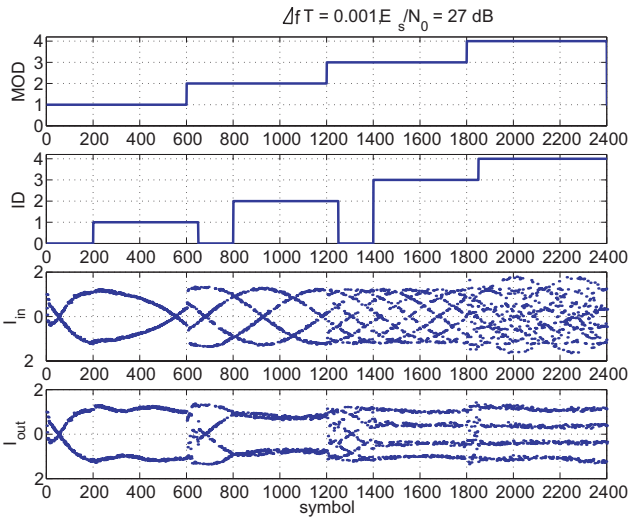

Fig. 18 MATLAB simulation results for BPSK, QQPSK, 8PSK and 16QAM, $\Delta f T_s = 0.001$, and $E_s/N_0 = 27$ dB.

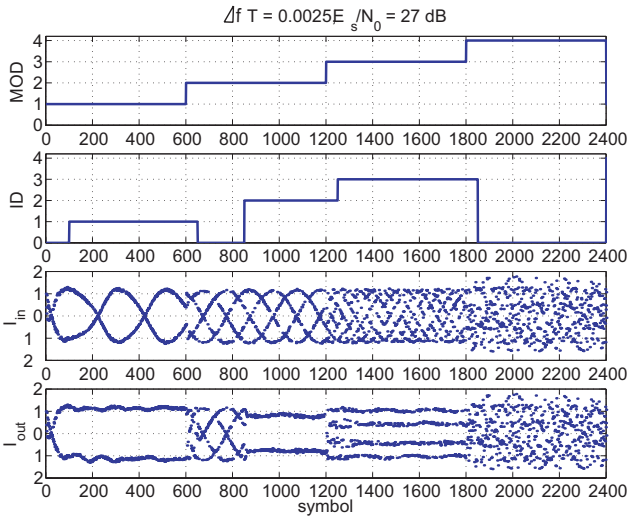

Fig. 19 MATLAB simulation results with BPSK, QPSK, 8PSK and 16QAM, $\Delta f T_s = 0.0025$, $E_s/N_0 = 27$ dB.

ered. This serves to confirm the computations of the maximum frequency offset that can be handled by the multiple-mode digital PLL.

Although the value $\Delta f T_s = 0.0025$ exceeds the maximum frequency offset for 8PSK modulation, in accordance to Table 1, 8PSK modulation was still successfully identified and recovered. This is became the AWGN process can help some of the constellation points to lie inside the lock area. From equation (4), it follows that in the absence of AWGN, for $\Delta f T_s = 0.0025$ and a total $\Phi/(2\pi\Delta f T_s) = 25$, received points will lie in the lock area. However, 8PSK is successfully identified because, in the particular case shown in Fig. 19, at least two points (most likely near the

boundaries of the lock sectors) were affected by additive noise in such a way that they were received in the lock area. However, general identification is not successful for 8PSK modulation for this value of $\Delta f T_s$ (although the signal can still be locked, after being identified, as it is evident from Fig. 19.)

4. Conclusion

In this paper, we have studied a multimode PLL which can achieve both carrier recovery and modulation identification. With the aid of employing digital PLL, PLD and modulation identification logic, the proposed system is robust against carrier offsets. In addition, the multimode PLL employs not only the blind approach but also a digital PLL, being useful for consumer multimode transceivers, i.e. software defined radio with adaptive modulation. Here, the PLDs are used not only for phase lock detection but also for modulation identification. Therefore, the complexity is less than that using cumulants [3] or other conventional schemes, and the acquisition time is expected to be much shorter, because the processes of the carrier lock and modulation idnetification are performed almost at an instant.

This paper also shows the delicate balance among frequency offset $\Delta f T_s$, Es/No and observation window N. A method to design N and N_T was presented. In addition, two kinds of maximum frequency offset $(\Delta f T_s)_{\max,\mathrm{N}}$ and $(\Delta f T_s)_{\max,\mathrm{N_T}}$ are obtained by N and N_T, respectively. In the performance analysis, the lock probability and the acquisition time are evaluated with theoretical value and computer simulations. These parameters relate $\Delta f T_s$ and the PLD configuration. In addition, considering the acquisition time, the existence of desirable frequency offset is explained by evaluating the frequency offset versus lock probability.

Comparing modulation identification ability with [3], even the observation period in our proposal is shorter while, the modulation identification ability is approximately equivalent. Furthermore, it is shown that the multimode PLL has more capability to improve the performance than the method presented in [3].

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