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A Neuromorphic Quadratic, Integrate, and Fire Silicon Neuron with Adaptive Gain

David Parent
San Jose State University

Eric Basham
San Jose State University

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Eric J. Basham, and David W. Parent *Member, IEEE*

***Abstract*—An integrated circuit implementation of a silicon neuron was designed, manufactured, and tested. The circuit was designed using the Quadratic, Integrate, and Fire (QIF) neuron model in 0.5 µm silicon technology. The neuron implementation was optimized for low current consumption, drawing only 1.56 mA per QIF circuit and utilized hysteretic reset, non-inverting integrator, and voltage-squarer circuits. The final area of each circuit in silicon was 268 µm height × 400 µm width. This design is the first IC of its kind for this neuron model and is successfully able to output true spiking that follows the behaviors of bistability, monotonic, and excitability spiking. The normal QIF design also features an easy way to change the time constant (which nominally operates in the millisecond range) of the spiking via a single, external capacitor (the only off-chip component in this design); the adaptive gain variation of the QIF circuit adds a second parameter that adjusts the time constant via an external resistor. The design also allows for an adjustable reset threshold and operates on a ±5 V power supply.**

***Index Terms*—Silicon Neuron, Quadratic, Integrate, and Fire, Neuromorphic Engineering, Integrated Circuit**

I. Introduction

Silicon neurons (SiNs) are part of a developing field called neuromorphic engineering. An SiN is an analog/digital mixed-signal circuit that models the behavior of a neuron [1]. Earlier approach to modeling neural behavior was to use dynamical system models [2]. The key features of dynamical neural models were bistability, excitability, and monotonic spiking [2]. With an accurate SiN model of neural behavior, novel applications for control and signal processing have become available.

SiNs have many real-world applications and also open the pathway for further development of many unique fields such as robotics. A robotic system designed around artificial neurons would be expected to have more organic movements and behavior, leading to more life-like robots and more usefulness. An example of this vision would be from the 2004 movie, "I, Robot." The movie shows robots that exhibit biological-looking movement and behavior. The development of SiNs could one day open the door to such robotic research and advancement.

Another important application of SiNs is the advancement of biomedical devices such as artificial limbs [3-5]. Modern artificial limbs are made from plastic composites, metals, and other materials; some more-advanced models even include electronics that allow limited movement of the digits of the hand [5]. With further development of tissue-to-circuit interfaces, SiNs may one day provide more fluid control of an artificial limb to an amputee. SiNs can also lead to improvements to computing and neural networks, including reduced power consumption [6].

Analysis of research into SiN circuits showed that a common neural model employed was the Leaky, Integrate, and Fire (LIF) model by [7]. The LIF model is a very simple implementation that uses a resistor and capacitor in parallel. As current flows into the capacitor, charge builds up. When the charge crosses the voltage threshold, the voltage on the capacitor is reset. Although this simplicity allows for easy implementation, the drawback is that the model does not actually generate a true voltage spike; instead, this spike is simulated. Among the problems with this model is that it represents an unrealistic behavior since no bistability is present.

Another attempt into neuromorphic engineering was the design of a circuit by [8] that implemented another neural model called the Integrate and Fire (IF) model. This model, an even simpler version than the LIF model, built 175 SiN circuits onto a single silicon chip. One major drawback to this design is its fixed time constants, which are fixed in place through the unchangeable components fabricated in silicon. This work uses an external capacitor to control the time constant of the neural spikes. Some of the same drawbacks exist with this IF model as does with the LIF model.

Many other SiN designs have been developed in this field, including some that use low power such as [9]. However, these designs use either the IF or LIF approaches, which as previously mentioned, included their modeling flaws.

While many researchers have investigated large neural arrays [10-12], there is still a need to research small arrays. Mishra [13] was able to use only two QIF neurons to calculate an analog XOR function. Small QIF networks can also be used to implement analog-to-digital conversion.

A hardware QIF model [14] that used discrete components reported a current of 200 mA. This circuit was able to achieve three modes of spiking, which included: bistable, excitable, and monotonic. The circuit used an integrator, a multiplier, a summing opamp, and a hysteretic reset. Although this circuit uses the energy-efficient QIF model, its implementation in discrete components (with power supplies of 15 V) increased the circuit area and power consumption.

A. The Quadratic, Integrate, and Fire Model

The Quadratic, Integrate, and Fire (QIF) model is a simple truly spiking neural model based on the dynamical system theory approach [2]. The behavior of the neuron is modeled by using the following equation:

$$\frac{\partial V}{\partial t} = V^2 + b \tag{1}$$

Since circuit hardware can perform the integrate function more easily, the equation was simplified to the following form:

$$V = \frac{1}{RC}\int V^2 + b \tag{2}$$

where V represents the voltage across the cell membrane and b is the input that represents the input current to the cell. The reset condition is given as follows:

When $V > V_{peak}$ then $V = V_{reset}$

The IC design was based on a discrete version given by [8]. Instead of using discrete components, the circuit was integrated into silicon, which limited the overall number of off-chip components as well as reduced the circuit size. This integration into silicon also reduced the power consumption of the circuit. A key differentiation of the design was the implementation of adaptive gain as shown in Figure 1. The loop gain of the circuit is described using the following equation, which originates from the gains of each circuit block that performs integration, multiplication, and summing function for the QIF design:

$$\frac{\partial V}{\partial t} = \frac{1}{RC}(V^2 + b) = m(V^2 + b) \tag{3}$$

Adaptive gain is implemented by removing the resistor of one of the opamp providing the gain for "m." This resistor is then set externally and is adjustable, which provides a gain that can be changed. The following list summarizes the key features of the design:

- Lower circuit area
- Ultra-low current consumption
- Adaptive gain implementation via single external resistor
- Adjustable time constant via single integrator capacitor
- Minimal number of off-chip components

II. System Overview

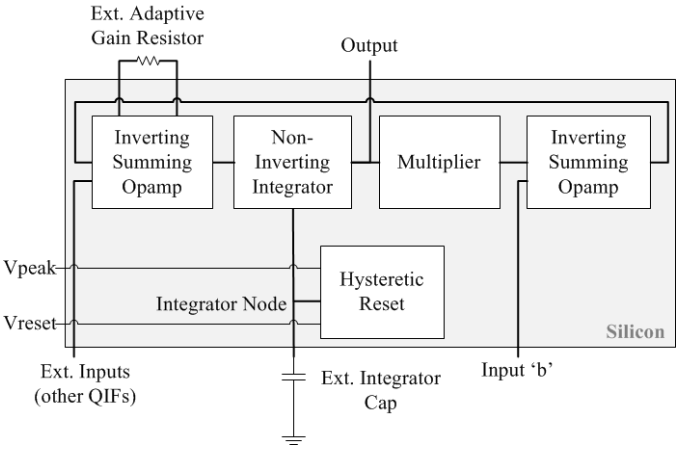

Figure 1: System overview of integrated QIF circuit.

III. Design Process

A. Development of the Opamp

The design of the SiN integrated circuit was based on the discrete implementation of the QIF model presented in [14], with major differences including a reduction in power consumption, integration of the system in silicon, and smaller physical size. Since opamps played a central role in all the different subcircuits in the discrete QIF design, it was decided to make the opamp the starting point of the IC design.

Different types of opamp architectures were explored, with a design decision made to use the two-stage Miller architecture. To design both opamp stages to meet bandwidth, gain, and power-consumption requirements, the GM/Id design method was used as developed by [15]. Using this methodology, an opamp was designed that operated in the moderate inversion region and drew a background current in the µA-range.

The final opamp design yielded the specifications shown in Table 1:

TABLE 1:
FINAL OPAMP SPECIFICATIONS

Feature	Specification
Open-Loop Gain	76.9 dB
Gain-Bandwidth	6.9 MHz
Phase Margin	175°
Current Consumption	200 µA
DC Output Offset	-14 µV

B. Non-inverting Integrator Circuit

The Deboo architecture shown in Figure 2, was used to create a non-inverting integrator that integrated the feedback signal of the system. The key feature of this integrator is that the integration time constant is controlled by a single capacitor (C_1 in Figure 2) that is connected externally to the IC. This allows the time period of the spikes to be adjustable from micro to milliseconds depending on the size capacitor used. The node the external capacitor connects to, is called the

integrator node. The voltage at this node is reset to VSS during a spiking event by means of a hysteretic reset circuit. Pass gates were implemented to prevent the current from being sourced from the prior stage during the discharge of the integrator node.

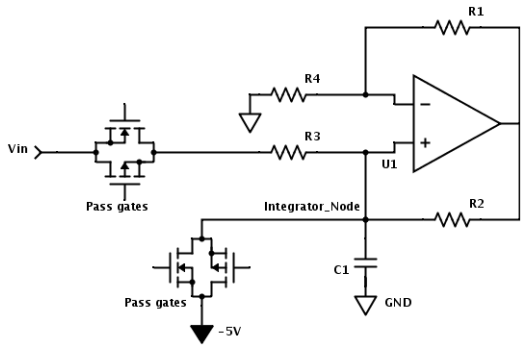

Figure 2: Non-inverting integrator (Deboo).

C. Hysteretic Reset Circuit

The hysteretic reset was based on the design introduced by [10] and is shown in Figure 3. The voltage accumulating on the integrator node is monitored using two comparators (one set with an upper threshold of Vpeak; the other set to a lower threshold of V_{reset}). The crossing of the integrator node voltage over the V_{peak} threshold triggers the activation of the hysteretic reset via an SR latch that turns on the pass gates in the integrator circuitry that drain the voltage from the integrator node. When the integrator voltage crosses the V_{reset} threshold, the hysteretic circuit is deactivated.

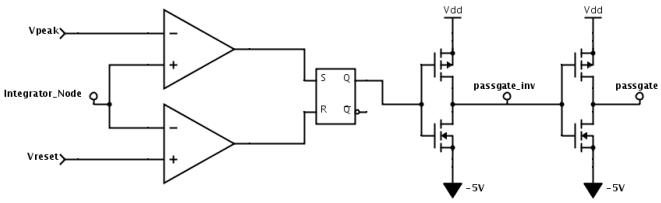

Figure 3: Hysteretic reset circuit block.

D. Multiplier Circuit

A multiplier circuit was needed to generate the V^2 function in the QIF equation. After exploring several different solutions, a multiplier design was used that was related to the Gilbert architecture and is based on a design by [16]. However, the design by [16] was altered and the transistors resized to operate at a very low power state as shown in Figure 4. This led to the separation of the multiplier circuit block into three parts: the input inverting circuit, the multiplier core, and the output scaling block as shown in Figure 5.

The first part of the circuit block consists of the input inverter. This is a simple non-inverting opamp that takes the output of the integrator circuit block and inverts it. This inverted signal, along with the original, non-inverted signal, is then fed into the multiplier core inputs. The multiplier core is where the V^2 function is performed. A squared-function was achieved but due to the low power design of the core, the maximum squared output available was 11 mV. This output was corrected by scaling the square function into the correct voltage range (i.e. a 2 V input equals 4 V), by using another non-inverting opamp to gain the signal. The final, complete multiplier block design allows for an input range of +/- 2 V with an output maximum of 4 V.

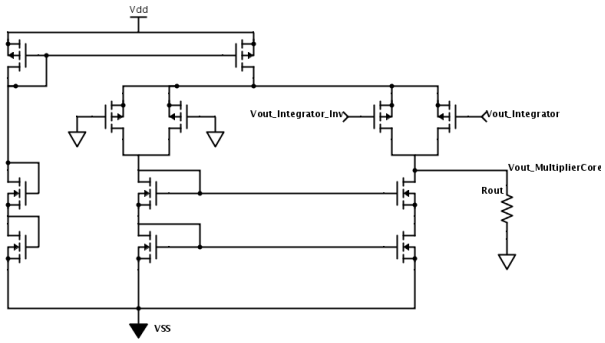

Figure 4: Multiplier core.

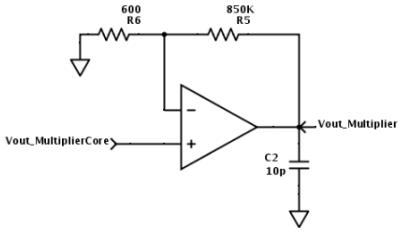

Figure 5: Multiplier output scaling circuit. C_2 shown here is implemented off-chip.

E. Supporting Circuits

After the multiplier block, an inverting summing amplifier was used to add the I_2 input signals to the output of the multiplier as shown in Figure 6. The summed output of this block was then fed back into the input of the system, which exists as another inverting summing opamp. These two inverting opamps correct the signal's polarity before being input into the integrator circuit block. Inverting summing opamps were used to minimize low impedance pathways in the system.

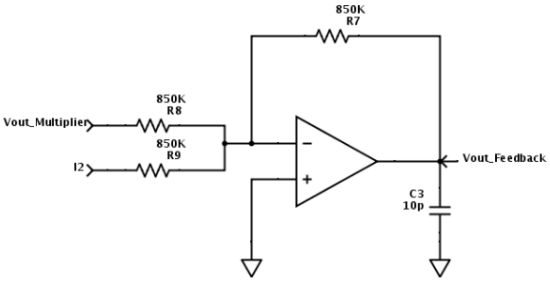

Figure 6: Inverting summing opamp with output feedback.

F. Simulations and results

LTspice was initially used to draft the complete circuit design. After simulations showing the correct neural behaviors were obtained, the design was copied into Cadence

software. The outputs were re-verified and found to be correct. The layout of the circuit in silicon was then performed.

The pad frame of the chip had a layout area of 268 µm × 400 µm, which allowed for four copies of the design to be placed into silicon. Three of the QIF circuits were identical; the fourth was changed to incorporate adaptive gain. To implement the adaptive gain, one of the resistors in the feedback loop of the input inverted summing opamp was removed. Figure 7 shows the summing input circuit of the QIF with the adaptive gain resistor.

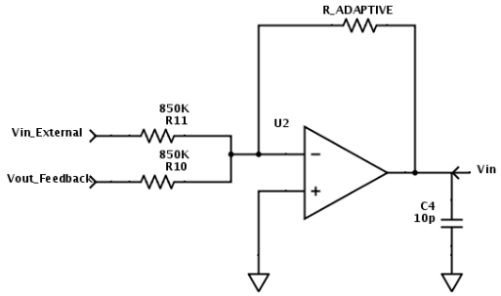

Figure 7: Inverting summing opamp.

IV. Post-Fabrication Lab Analysis Results and Discussion

A. Monotonic Spiking

The following test results are derived from in-lab analysis performed on one of the received chips from MOSIS. The QIF chip was connected to the DC power supplies (±5 V). The Vpeak and Vreset signals were implemented using DC power supplies. The supplies were set to the following settings and connected to the QIF chip: Vpeak = 2 V, Vreset = -2 V. Input "b" was connected to an external DC power supply set to a constant 0.6 V. An external cap of 0.1 µF was connected to the integrator capacitor input. After all the required inputs were connected to the QIF, a continuous spiking output was measured on the oscilloscope.

Figure 8 shows the QIF circuit correctly continuously spiking in response to a constant input.

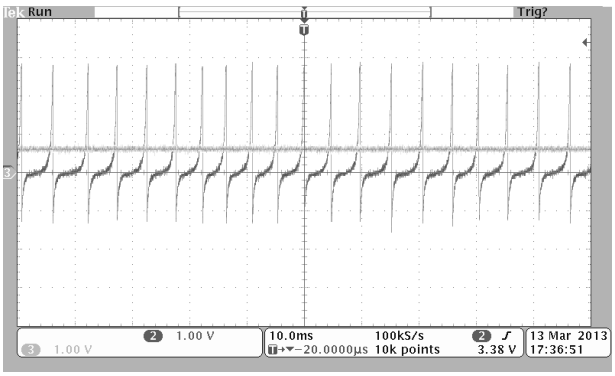

Figure 8: Monotonic spiking measured with the following conditions: Vpeak= 2 V; Vreset= -2 V; b= 0.6 V DC; ext. integrator cap= 0.1 µF.

B. Excitability Spiking

For excitability testing, the external signals remained the same as the prior test, except for the "b" input, which was set to two positive pulses.

Figure 9 shows the QIF circuit correctly spiking in response to two input pulses, which both represent the I2 input. When the positive voltage by the I2 input is seen by the QIF, it is added to the output of the multiplier and integrated. When the voltage level of the integration crosses the Vpeak threshold, the hysteretic reset circuit block activates and drains the voltage stored on the external integrator cap to ground. This results in the spiking output. When no I2 input pulse is present, no integration occurs and no spiking is outputted by the QIF system.

The input pulses, when increased in amplitude, were found to cause the spiking frequency to increase as expected.

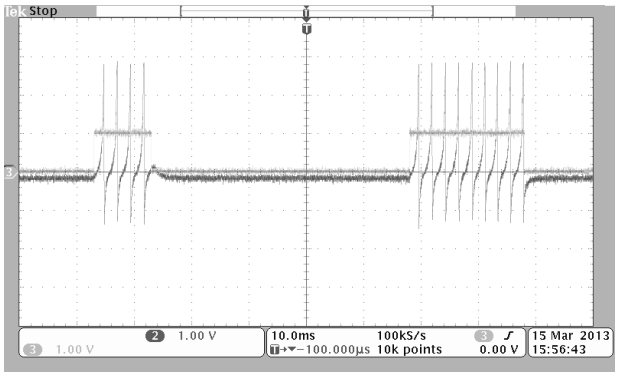

Figure 9: Excitability spiking measured with the following conditions: Vpeak= 2 V; Vreset= -2 V; b= two positive input pulses at 10 ms and 20 ms pulse width each; ext. integrator cap= 0.1 µF.

C. Bistable Spiking

For bistable spiking, the circuit setup remained the same as in the monotonic spiking test, except for the following changes: Vreset was changed to 0 V. The "b" input consisted of a short positive pulse, followed by a delay, and finally ending with a negative pulse. The integrator cap value was changed to 0.01 µF.

Figure 10 shows the results of the QIF correctly exhibiting bistable behavior. With the Vpeak and Vreset settings to the bistable conditions of 2 V and 0 V, respectively, the positive input pulse causes the QIF to enter the bistable region. The negative input pulse causes the spiking to leave the bistable region. Just as with Part B, the input pulse adds to the multiplier output and causes integration of the value. The integrated value then increases as long as the input pulse is present and results in a spike when Vpeak is crossed and the integrator cap is drained.

When the input returns to zero after the initial pulse, the value of Vreset at 0 V means that not all of the voltage at the

integrator node is drained. This slight voltage at the integrator cap is high enough for another charge to build up and causes another spiking event, which, again, only resets to 0 V. This creates an infinite loop of spiking until the negative amplitude input pulse is received by the QIF, which fully drains the integrator cap voltage and stops the spiking.

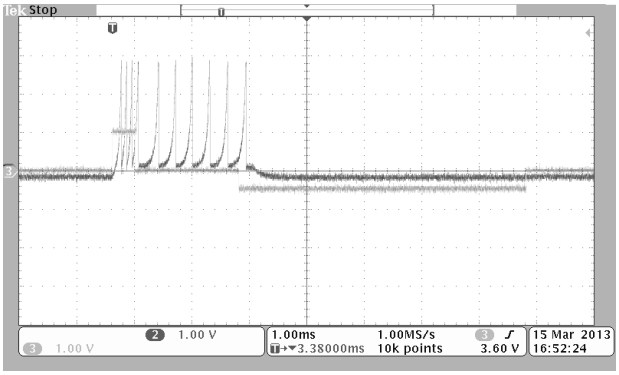

Figure 10: Bistable spiking measured with the following conditions: Vpeak= 2 V; Vreset= 0 V; b= one positive, one negative pulse; ext. integrator cap= 0.01 µF.

D. *Strength-Duration Curve Comparison*

A Strength-duration curve is a measure of how the system reacts to varying pulse widths and amplitude input signals. For example, low amplitude, large pulse width signals may trigger a spiking event same as that for high amplitude, small pulse width signals. Figure 11 shows the simulated vs. actual lab analysis strength-duration curve for the circuit. The graph itself represents the spiking threshold that is simulated/measured.

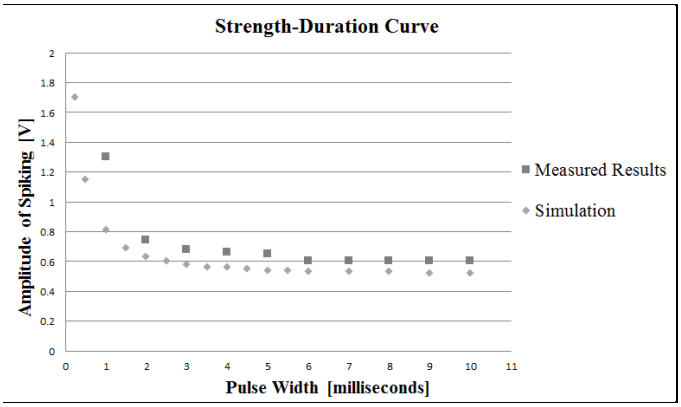

Figure 11: Strength-duration curve obtained from simulation and postfabrication lab analysis; both curves show similar characteristics.

E. *Functional Regions Comparison*

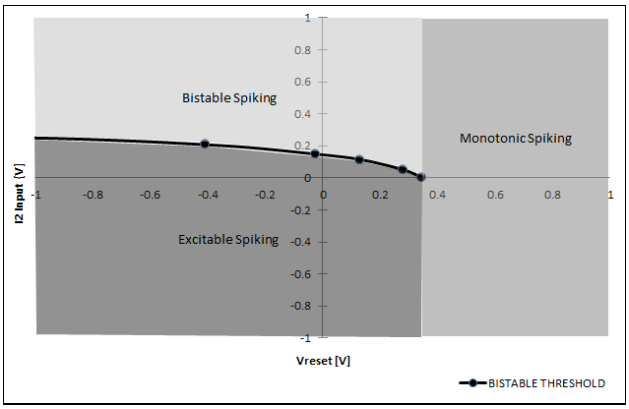

Figure 12: Functional regions of spiking obtained during lab analysis.

Figure 12 shows the different regions of spiking that were obtained during lab analysis. Depending on the value of I_2 ("b" input), as well as the value that Vreset is set to, it is possible to achieve either monotonic, excitable, or bistable spiking.

The offset of the curve in Figure 12 to the right of the origin is being caused by a DC offset introduced into the circuit after fabrication. The source of the offset is from the output of the multiplier since both the input I2 and the multiplier output are added together as shown in the circuit of Figure 6. The multiplier's characterization consists of a V^2 function, with the vertex of the parabolic curve designed to operate as close as possible to 0 V. Any upward DC shift of this function would introduce a DC bias voltage into the input of Figure 6, as what happened here with this circuit.

Figure 12 also shows the relationship of the behavior of the QIF depending on the two main parameters, V_{reset} and I_2. The y-axis represents the value that the V_{reset} parameter is fixed to. The x-axis is the I_2 input that is given to the system. The three regions shown in the figure are the different spiking patterns that arise from the different combinations of V_{reset} and I_2.

F. *Adaptive Gain Results*

Figure 13 shows the results of the circuit simulation prior to fabrication; each quadrant shows the spiking frequency as the adaptive gain resistor is changed.

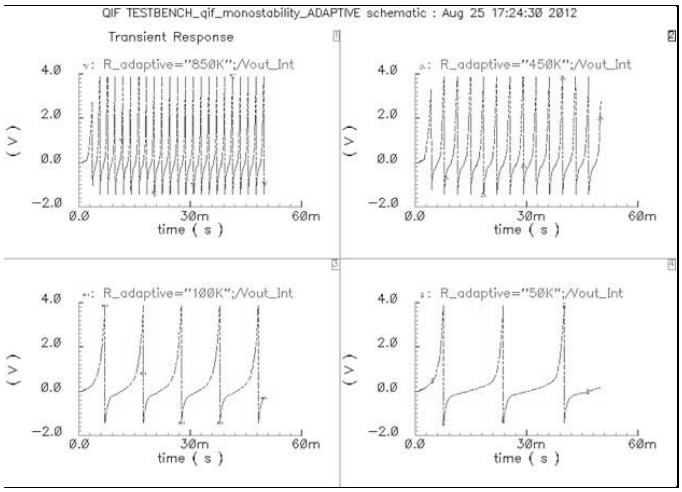

Figure 13: Adaptive gain simulation results in spice. Upper-left quadrant: 850 kΩ resistor; upper-right quadrant: 450 kΩ resistor; lower-left quadrant: 100 kΩ; lower-right quadrant: 50 kΩ.

G. *Current Consumption*

The fabricated chip's current consumption was measured in the lab and it was found that each QIF drew a current of 1.56 mA.

The discrete version of the QIF design by [14] reported a current consumption of 200 mA, which shows that the integrated QIF design drew 128× lower current.

V. Conclusion

A functioning artificial neuron integrated circuit (IC) was successfully designed, fabricated, and tested. The IC design was based on the Quadratic, Integrate, and Fire (QIF) dynamic systems model of neuron behavior. The goal emulating key features of neuron behavior such as monotonic, excitable, and bistable spiking was successfully implemented and verified through in-lab analysis. Other features of the design that were envisioned at the start of the project were also implemented. One of the features implemented was a significant reduction of current consumption vs. the discrete version of the QIF design. The designed QIF IC consumes a current draw of only 1.56 mA. Next, the footprint of the circuit was minimized to 268 µm × 400 µm. The design also allows for an adjustable adaptive gain using only a single externally set resistor. The time constant from the QIF is also adjustable via a single external capacitor. The circuit operates on a simple ±5 V power supply and outputs spikes of approximately 4 V in amplitude with periods in the millisecond range. Given that the fabricated die contains four QIF neurons, this implementation is suitable for small low-power neural networks. Future work will consist of developing applications for small neural nets, as well as developing the educational resources that are needed for the technology to be adapted.

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