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Pranabendra Sarma
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ELECTRICAL CHARACTERIZATION OF PRINTED CIRCUIT BOARD
INTERCONNECTS: MEASUREMENTS AND ANALYSIS

A Thesis

Presented to

The Faculty of the Department of General Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Engineering

by

Pranabendra Sarma

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APPROVED FOR THE DEPARTMENT OF GENERAL ENGINEERING

Dr. Avtar Singh, Electrical Engineering Dept.
Thesis Advisor

Dr. Guna Selvaduray, Materials Engineering Dept.
Reading Committee

Dr. Eric Bogatin, Sun Microsystems
Reading Committee

APPROVED FOR THE UNIVERSITY

ABSTRACT

ELECTRICAL CHARACTERIZATION OF PRINTED CIRCUIT BOARD INTERCONNECTS: MEASUREMENTS AND ANALYSIS

by

Pranabendra Sarma

The characteristic impedance of the traces of a 10 layer printed circuit test board was calculated using three different field solvers. The traces consisted of microstrips and different types of striplines. The characteristic impedance and the time-of-flight were also measured using a Tektronix TDR and a HP network analyzer. The values obtained from the field solvers were compared with the measured values. The suitability of the solvers to model interconnects (traces) was analyzed. The results obtained from the three field solvers compared well with the measured data for trace separations above three mils. The measured and the calculated results differed by more than 10 percent in some cases where the trace separations were less than three mils. This study provides a framework for evaluating the applicability of a field solver for modeling multilayer printed circuit board traces.

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CHAPTER 1

INTRODUCTION

Before fabricating a printed circuit board (PCB), the designer should ascertain the effects of the electrical characteristics of the printed circuit board interconnects. A printed circuit board's stubs, variable trace widths, vias, and IC packaging can affect the characteristic impedance of traces on the board.[1] With clock frequencies of 33 MHz and above becoming normal, transmission line characteristics of interconnects are gaining importance. This necessitates transmission line analysis of both on-chip wires and board level interconnects. Transmission line behavior becomes significant when the rise time of a signal is less than or comparable to the time-of-flight delay. With the increase in number of I/Os and as the lines become closer, cross-talk results due to the mutual capacitance and inductance between neighboring lines. With decreasing size of digital systems and increasing clock speeds, electro-magnetic interference (EMI), due to coupling and cross-talk between lines on printed circuit boards and integrated circuit (IC) chips, becomes a major design problem.[2]

A majority of the system houses get their boards from different vendors. It will be very costly to do testing of

each and every board to determine the behavior of the interconnects. Rejecting boards because of non compliance is not a viable solution. To get a board satisfactory to both the fabricator and the customer, close cooperation between the designer and the fabricator is necessary. It is here that the designer will be benefited by a modeling and simulation scheme, before the layout drawings are even submitted to the printed circuit board fabricator. The designer has to verify that all signals, that are degraded by reflective and cross-talk noise along the propagation path, must stay within the noise-margin constraints. Noise budgeting requires that the designer identify and quantify the significant noise contributors early in the design cycle. The design should be adjusted to minimize the major contributing effects and thereby maintain adequate noise margins. Simulation can ease the development of a reliable design, before production, in two ways: it can pinpoint areas in the board layout that are prone to signal degradation; and it provides an easy method to run successive analysis of design alternatives.[1]

All the basic types of interconnections found in a printed circuit board can be modeled using transmission line techniques. The two most important characteristics of the signal line itself are its propagation delay and its characteristic impedance. On printed circuit boards the

propagation delay becomes important mainly on critical timing chains such as clock lines. The characteristic impedance, Z_0 , is important when considering loading, reflections, and cross-talk.[3]

In the market, a number of software tools are available for modeling PCB interconnects and to extract their electrical characteristics. These software tools provide a much needed benefit to the design engineer to model the interconnects and to evaluate the effects of physical geometry on the electrical characteristics before finalizing the design process. There are two important considerations before selecting a software to validate the design process: how good are the results produced by the software and how well do they match the measured and simulated values. The ease of using and the costs of the software are also important factors.

The aim of this study was to investigate the available software tools in the market to model PCB interconnects and to correlate the calculated data with measured data obtained from instruments such as the time domain reflectometer (TDR) and the network analyzer. Initially different software vendors were contacted, with the idea of evaluating their tools by using the measured physical geometry of interconnects from printed circuit boards fabricated for this study. Three different field solvers from Integrity

Engineering, Contec Microelectronics, and Quad Design respectively were used to model the interconnects. Printed circuit boards were fabricated by two vendors. Due to the high cost of cross-sectioning and laboratory measurement of the physical geometry, the data from a board fabricated by Zycon Corporation of Santa Clara was used for the study. The cross-sectioning of the board and the measurements of the physical geometry were carried out at Ultra Test International, Inc. in San Jose. The TDR and the network analyzer measurements were carried out at Sun Microsystems' failure analysis laboratories in Mountain View. The data provided by the present study should prove helpful in correlating the calculated values from the field solvers and the measured values from the instruments. This can form a basis for evaluation of the tools for future use in the printed circuit board design and fabrication process. The details and results of this study and a description of the PCB fabrication procedure, as well as a discussion of the electrical parameters of the interconnects, are presented in the following chapters.

CHAPTER 2

PRINTED CIRCUIT BOARD FABRICATION

To make a complete multilayer circuit board, from incoming materials to shipping, over 50 different process steps are required.[4] These steps include electrical, chemical, mechanical, and optical processes, including testing at key points to make sure that quality is built into the product. These steps[4-6] are briefly discussed below.

2.1 Printed Circuit Board Fabrication Process

The basic building blocks of a PCB are the metal foil, the core, either one-sided or two-sided, and/or the prepregs. They are shown in Figure 1. Metal foil, which is usually copper, is available as separate sheets or preapplied to the dielectric material. Metal foil is applied under heat and pressure to the dielectric. The dielectric flows around dendrites that are formed during creation of the metal foil, and creates a strong physical bond. The metallic ground planes for power and ground are laminated in a similar manner. The dielectric layers can be solid pieces of material or a combination of dielectric and a binder such as epoxy. The dielectric for the test board, FR-4 (fire-retardant), was constructed from a fiberglass fabric and

Figure 1. Components of a Printed-Circuit Board[5]

epoxy. A pre-preg layer is a dielectric layer whose epoxy has not been fully cured. This allows the epoxy to reflow easily when different layers are bonded together. This flow of epoxy bonds the layers and prevents shorts during plating of any plated-through hole.

Once the design of the board is received from the customer, the front end tooling traveler and the production traveler, detailing all necessary instructions to manufacture the board, are prepared. At this point the customer design and documents are reviewed and all manufacturing issues are resolved with the customer.

In the next step, based on the production requirement, the drilling, the routing and the test fixture NC programs are created. The artworks for all imaging processes are edited and panelized using customer supplied data. All necessary silver films are then plotted.

From the silver films, photo masters and/or finals are made. The tooling holes are then punched into the film and final inspection of all photo tools is performed.

The copper surfaces are then prepared for dry-film photoresist application. To assure proper adhesion and intimate contact, the surfaces are acid washed and scrubbed with pumice.

Each surface is then coated with a photoresist material and the circuit board image transferred to the surface using

photo tool artwork. The dry-film photoresist used in PCB fabrication is a multilayer organic-composite system. It is composed of a flexible photoresist film between release and cover sheets as shown in Figure 2. To achieve proper adhesion and intimate contact, dry-film photoresists are laminated onto the surface with flow achieved under heat and pressure. The photo image is then developed and the unwanted copper removed, leaving isolated conductors in the circuit pattern. The photoresists are then removed from the conductors.

An automated optical inspection system (AOI) is used to inspect the circuit pattern for quality and to assure customer satisfaction.

The copper circuitry is then cleaned and a black oxide treatment (solution of sodium chlorate and sodium hydroxide) applied to the layers to enhance bonding during lamination process. All the inner-layer details are then assembled and pressed together to form multilayer panels. Cross-section of the inner layer of a PCB is shown in Figure 3.

Once the multilayer panels are assembled, holes are drilled through the board to establish a continuous path between layers and to provide holes for customers to mount the required components. Each panel is then dipped in a copper solution to deposit copper in the barrels of the drilled holes. The panels are then coated with a photo-

Figure 2. Dry-film Photoresist System [6]

Figure 3. Cross-Section of PCB Inner Layer[5]

resist material and the circuit board image transferred to the top and bottom panels using photo tool artwork. The photo image is then developed.

The panels are then electroplated in a copper solution to form electrical conductors on circuits and holes.

Next in the stripping and etching process, the photo-resist is removed to expose copper. The unwanted copper is removed leaving isolated conductors in the circuit pattern. This completes the top and the bottom layers.

The panels are now electrically tested for opens and shorts, using custom designed beds of pins to test conductivity.

The circuit pattern is now coated with a solder resist ink and required legends are printed onto the panel to identify various components. The panels are then dipped in molten solder, and blasted with hot air to even out solder coatings to prepare the surfaces for solder mount parts.

A cross-section of a sample board is then cut from each lot and the plated holes examined with a microscope. The individual boards are then cut out of the panels. After electrical test, dimension and visual inspection, and quality audits, the boards are packaged, labeled and shipped to the customer. A process similar to the one described above was used to fabricate the test board used in the study.

2.2 The Test Board

The test board used in this study was a 10 layer board, with one top and one bottom signal layer and four inner signal layers and four inner ground planes. The traces were 8 inches and 2 inches long. The traces were metallized with one ounce copper (one ounce copper per square foot). The inner layers were bare copper with an average thickness of 0.0014 inch (1.4 mils) and the outer layers, after solder-plating, had an average thickness of 0.0023 inch (2.3 mils). The top and the bottom layer consisted of three sets of microstrips each, with trace separation ranging from 0.001 inch (1.0 mils) to 0.290 inch (290 mils). Layer 3 and layer 8 consisted of three sets of symmetrical striplines with trace separation ranging from 0.001 inch to 0.290 inch. Layers 5 and 6 consisted of three sets of broadside coupled strip-lines and one set of asymmetrical striplines. The different constructions of the traces are discussed in the next section. The total thickness of the plate was approximately 0.079 inches (79 mils). The individual layer thicknesses and the interconnect physical geometries are shown in Figure 4 through Figure 9. The nomenclature used in the figures is explained here. ϵ_r means the dielectric constant, h stands for dielectric thickness of microstrip construction, b stands for dielectric thickness of stripline construction, h_1 is the distance of the trace from the lower ground plane

and h_2 is the distance of the trace from the upper ground plane in case of striplines, t is the thickness of the trace, w_b is the width of the bottom of the trace and w_t is the width of the top of the trace, h_t is the separation between the top and bottom traces in case of a broadside coupled stripline, and s_{ij} is the separation between the i th and j th traces at their widest part. All units are in mils.

The physical geometry values were obtained by measuring the traces after cross-sectioning the board. All together nine cross-sections were made for the two outer and four inner signal layers. The measured values had a variation of ± 0.9 mils in dielectric thickness between section E and section D of layer 5/6 and ± 0.8 mils between section A and section D in layer 3. In some of the symmetrical striplines, h_1 and h_2 had a difference of ± 0.5 mils. The variation in separation distances was between 0.1 to 0.3 mils except in case of section E in layer 5/6 where it was 10 mils in a separation of 281 mils. All the cross-sections were photographed. Some of these cross-sections are shown in Figure 10 through Figure 13. In cases where the separation distance was too large, namely 290 mils, only one trace was photographed as a representative sample. The whole section could not be photographed with the available equipment. These photographs clearly show the traces in each layer.

Section A, Microstrips. $t=2.3$ mils., $h=5.1$ mils, $w_{b1}=8.7$ mils, $w_{b2}=8.0$ mils, $w_{b3}=7.1$ mils, $w_{t1}=7.1$ mils, $w_{t2}=6.2$ mils, $w_{t3}=5.4$ mils, $s_{12}=290.2$ mils, $s_{23}=290.3$ mils.

Section B, Microstrips. $t=2.3$ mils., $h=5.0$ mils, $w_{b1}=8.6$ mils, $w_{b2}=9.2$ mils, $w_{b3}=8.9$ mils, $w_{t1}=6.8$ mils, $w_{t2}=6.6$ mils, $w_{t3}=6.7$ mils, $s_{12}=3.6$ mils, $s_{23}=3.5$ mils.

Section C, Microstrips. $t=2.2$ mils., $h=4.9$ mils, $w_{b1}=8.5$ mils, $w_{b2}=8.9$ mils, $w_{b3}=8.9$ mils, $w_{b4}=8.7$ mils, $w_{b5}=8.4$ mils, $w_{t1}=6.8$ mils, $w_{t2}=7.1$ mils, $w_{t3}=w_{t4}=7.0$ mils, $w_{t5}=6.7$ mils, $s_{12}=4.0$ mils, $s_{23}=3.9$ mils, $s_{34}=4.1$ mils, $s_{45}=4.0$ mils.

Figure 4. Physical Dimensions of Layer 1, Sections A, B, and C.

Section A, $t=1.2$ mils, $h_1=8.5$ mils, $h_2=9.0$ mils, $w_{b1}=6.5$ mils, $w_{b2}=7.5$ mils, $w_{b3}=8.5$ mils, $w_{t1}=6.1$ mils, $w_{t2}=7.1$ mils, $w_{t3}=8.0$ mils, $s_{12}=s_{23}=291$ mils.

Section B, $t=1.4$ mils, $h_1=8.8$ mils, $h_2=8.0$ mils, $w_{b1}=7.5$ mils, $w_{b2}=7.8$ mils, $w_{b3}=7.9$ mils, $w_{t1}=7.4$ mils, $w_{t2}=7.5$ mils, $w_{t3}=7.6$ mils, $s_{12}=s_{23}=5.0$ mils.

Section D, $t=1.3$ mils, $h_1=9.4$ mils, $h_2=8.8$ mils, $w_{b1}=w_{b2}=w_{b3}=w_{b4}=w_{b5}=7.9$ mils, $w_{t1}=w_{t2}=w_{t3}=w_{t4}=w_{t5}=7.4$ mils, $s_{12}=s_{23}=s_{34}=s_{45}=5.0$ mils.

Figure 5. Layer 3, Symmetrical Striplines, Sections A, B, and D.

Section D, Broadside Coupled Striplines, $h_1=5.6$ mils, $h_2=6.0$ mils, $h_3=9.6$ mils, $s_{12}=s_{23}=5.6$ mils, $w_{b1}=w_{b2}=w_{b3}=7.5$ mils, $w_{t1}=w_{t2}=w_{t3}=7.2$ mils, $w_{b4}=w_{b5}=w_{b6}=7.1$ mils, $w_{t4}=w_{t5}=w_{t6}=6.9$ mils, $t=1.4$ mils.

Section G, Broadside Coupled Striplines, $h_1=5.7$ mils, $h_2=5.7$ mils, $h_3=9.6$ mils, $s_{12}=s_{23}=10.3$ mils, $w_{b1}=w_{b2}=w_{b3}=7.5$ mils, $w_{t1}=w_{t2}=w_{t3}=7.2$ mils, $w_{b4}=w_{b5}=w_{b6}=7.4$ mils, $w_{t4}=w_{t5}=w_{t6}=7.1$ mils, $t=1.3$ mils.

Figure 6. Layer 5/6, Broadside Coupled Striplines.

Section E, Asymmetrical, Off-center Stripline, $h_1=16.1$ mils, $h_2=5.6$ mils, $t=1.4$ mils, $w_{b1}=6.6$ mils, $w_{b2}=7.9$ mils, $w_{b3}=8.8$ mils, $w_{t1}=6.1$ mils, $w_{t2}=7.3$ mils, $w_{t3}=8.2$ mils, $s_{12}=s_{23}=290$ mils.

Section F, Broadside Coupled Striplines, $h_1=h_2=6.0$ mils, $t=1.3$ mils, $h_3=9.6$ mils., $w_{b1}=7.5$ mils, $w_{b2}=7.1$ mils, $w_{t1}=7.2$ mils, $w_{t2}=7.1$ mils.

Figure 7. Layer 5/6, Asymmetrical and Broad side Coupled Striplines, Section E and F.

Section F, $t=1.3$ mils, $h_1=8.4$ mils, $h_2=8.5$ mils, $w_{b1}=7.2$ mils, $w_{b2}=7.2$ mils, $w_{b3}=7.0$ mils, $w_{t1}=7.0$ mils, $w_{t2}=7.1$ mils, $w_{t3}=6.9$ mils, $s_{12}=s_{23}=10.5$ mils.

Section H, $t=1.3$ mils, $h_1=9.0$ mils, $h_2=8.6$ mils, $w_{b1}=6.0$ mils, $w_{b2}=7.0$ mils, $w_{b3}=7.9$ mils, $w_{t1}=5.8$ mils, $w_{t2}=6.7$ mils, $w_{t3}=7.8$ mils, $s_{12}=s_{23}=290$ mils, Asymmetrical Striplines.

Section I, $t=1.2$ mils, $h_1=9.0$ mils, $h_2=8.8$ mils, $w_{b1}=w_{b2}=w_{b3}=w_{b4}=7.6$ mils, $w_{b5}=9.2$ mils, $w_{t1}=w_{t2}=w_{t3}=w_{t4}=7.1$ mils, $w_{t5}=8.7$ mils, All Trace Separations= 1.0 mil, Symmetrical Striplines.

Figure 8. Layer 8, Striplines, Sections F,H,and I.

Section C, Microstrips. $t=2.3$ mils., $h=5.3$ mils, $wb_1=wb_2=wb_3=8.1$ mils, $wt_1=wt_2=wt_3=6.7$ mils, $s_{12}=s_{23}=9.5$ mils.

Section H, Microstrips. $t=2.3$ mils., $h=5.3$ mils, $wb_1=7.3$ mils, $wb_2=8.2$ mils, $wb_3=9.0$ mils, $wt_1=5.7$ mils, $wt_2=6.6$ mils, $wt_3=7.5$ mils, $s_{12}=s_{23}=290$ mils.

Section I, Microstrips. $t=2.3$ mils., $h=5.1$ mils, $wb_1=wb_2=wb_3=wb_4=wb_5=7.5$ mils, $wt_1=wt_2=wt_3=wt_4=wt_5=6.5$ mils, All Trace Separations = 1.0 mils.

Figure 9. Layer 10, Microstrips, Section A,B, and C.

Figure 10. Cross-section photograph of Layer 1, section B showing microstrips.

Figure 11. Cross-section photograph of Layer 1, section C showing microstrips.

Figure 12. Cross-section of Layer 5/6, Section G, Brodside Coupled Striplines.

Figure 13. Cross-section of Layer 8, Section F, Symmetrical Striplines.

2.3 Terms Associated With PCB Geometry

In this section the different terms associated with the physical geometry of the PCB interconnects are explained.

2.3.1 Ground Planes

These are also known as shield planes. Solid copper planes, with clearance holes etched out in areas where no contact is desired, can be placed anywhere within the structure of the multilayered board. The planes either serve as electrical decoupling to minimize the noise interference or cross-talk between various critical circuits, or are used for shielding some circuits within the board or the entire board from any internal or external interference. A number of such planes can be incorporated within one board and can also be used for power distribution.[7] The test board had four internal ground planes. Figure 14 below shows a possible cross-section with the ground planes and the traces identified.

Figure 14. Cross-section of Multilayered PCB

2.3.2 Traces

The traces or the interconnects are the signal lines carrying signal and power to different components. For the test board, traces were made of 1 ounce copper . Depending on the locations, the traces can be either microstrips or striplines. The test board inner layers (3, 5/6, and 8) had traces with thickness of 1.4 mils and the outer layers (1 and 10) had 2.3 mils thick traces. As discussed in section 2.1, the trace separations varied.

2.3.2.1 Microstrips

Microstrips are one of the most popular transmission line structures. Ease of fabrication by photolithography techniques and a good range of impedance and couplings allow it to be used for a wide variety of circuit components.[8] In the microstrip structure, the signal lines are placed on the upper surface of the dielectric medium as shown in Figure 14. For such a microstrip line, most of the electromagnetic wave is contained in the underlying dielectric medium. However, a significant fraction of the wave energy resides in the air dielectric.[9] Therefore, the dielectric constant for the microstrip structure is not the dielectric constant of the underlying dielectric medium (FR-4 in case of the test board), but is a composite of the air and the dielectric medium.

2.3.2.2 Striplines

If the signal lines are sandwiched between two reference planes, the construction is known as a stripline or triplate structure. The presence of the second reference plane increases the capacitance and reduces the value of the characteristic impedance. Originally the stripline structure meant a ground-signal-ground transmission line with air dielectric. The triplate structure was developed at Sanders Associates, Inc. with striplines and solid dielectric.[8]

The stripline structures on the test board were divided into four categories: symmetrical striplines, asymmetrical striplines, off-center, and broadside coupled striplines.

In the symmetrical striplines the traces are all of equal width, whereas in the asymmetrical striplines the traces have different widths. The traces are centered with respect to the two reference or ground planes.

The off-center stripline structure is found mainly in multilayer boards. Two situations can make its use desirable. In order to make the board symmetric relative to the center-line (to avoid warpage), it is sometimes necessary to place the stripline off-center relative to its surrounding ground planes. It is also common to run two layers of striplines (broadside coupled stripline) between a single pair of ground planes to increase density. Layer 5/6 in the test board had three sets of such striplines. Each of these

layers was off-center relative to the ground planes. A similar construction is dual orthogonal striplines in which the coupled striplines are run perpendicular to each other. The test board did not have this type of stripline.

2.3.3 Plated-Through Hole or Via

In a two-sided or multilayered board, a via is used to facilitate signals to change layers. If the via is completely inside the surface and never reaches the surface, then it is known as a blind or buried via. If the via connects both the top and the bottom surface of the board, then it is known as plated-through hole. The via may be used in series with the signal line when changing layers or it may be used to connect surface mount components to a ground plane or another layer. The vias are also used to tie together ground planes on different layers of the PCB. When a via is in series with the signal path, it should have the same characteristic impedance as the transmission line it is interconnecting. When it is used for grounding, it should have as low an impedance as possible. Figure 15 shows a via connecting two microstrip lines.

2.3.4 Dielectric

Dielectric materials do not conduct electricity. The

Figure 15. Via connecting Microstrip lines^[10]

dielectric materials generally behave like capacitors. The dielectric strength (volts/inch) of a material refers to the maximum voltage that the material can withstand without resulting in a voltage breakdown. The dielectric constant refers to the ratio of the capacitance, C_x , of a given configuration of electrodes with a specified dielectric, to the capacitance, C_v , of the same electrode configuration having a vacuum or air as the dielectric.^[11]

CHAPTER 3

ELECTRICAL CHARACTERISTICS OF PRINTED CIRCUIT BOARD INTERCONNECTS.

In multilayered printed circuit boards used in computers, some of the conducting layers are used to provide electrical ground and power-supply voltages, and others to provide interconnections among integrated circuit chips. A signal layer usually contains parallel signal lines; two adjacent layers of orthogonal lines constitute a signal-plane pair. Signal lines may or may not have adjacent neighbors. If two or more parallel lines are in close proximity, the presence of signal on one line causes noise to appear in adjacent lines. At the near (source) end of the signal lines, such noise may be saturated or unsaturated, depending on signal rise time and the length over which the lines are coupled. At the far end, the noise generally increases linearly with the length and inversely with the rise time.[9]

3.1 Transmission Lines

If the interconnections are sufficiently long or the circuits are sufficiently fast, such that the rise times of the waveforms are comparable to the time-of-flight across

the line (determined by the speed of light), the interconnects must be modeled as transmission lines. The rise time of a pulse generator is a rough measure of its high frequency content. The formula[12]

$$f = \frac{0.35}{\tau} \quad (1)$$

gives an approximate value for the highest sinusoidal frequency, f , contained in a step with rise time τ . Therefore, if the highest frequency component of the pulse generator is 100 MHz, then the rise time of the signal will be 3.5 nanosecond. The rise time is defined as the time required for the signal to move from 10 percent to 90 percent of its final value.

The highest effective clock frequency that the low frequency model will describe is approximated by[13]

$$f_{\text{clock}} = \frac{12}{20(l\epsilon_r^{1/2})} \quad (2)$$

with f_{clock} in gigahertz and l in inches. The denominator can be thought of as the electrical length, and the term in brackets is the inverse of the time-of-flight (TOF) down the interconnect. For the 8 inch traces of the test board and with a dielectric constant of 4.5 for FR-4, low frequency

lumped model analysis will work up-to a frequency of 35 MHz. Above that, transmission line analysis will be needed.

The rule of thumb when to use transmission line analysis is that when the rise time is shorter than twice the TOF, signals travel like waves and the transmission line properties of the interconnect must be used to analyze the influence of the interconnect on signal integrity.[13] Transmission line analysis always gives the correct answer irrespective of the rise time; however, the same answer can be obtained with the same accuracy using lumped approximation when $\tau > 5$ TOF.[14] All of the basic types of interconnects found in a printed circuit board can be modeled via transmission line techniques.

3.1.1 Lossless and Lossy Transmission Lines

Printed circuit board conductors have large cross-sections. The large cross-sections yield sufficiently low resistance; therefore these structures can be treated as lossless transmission lines. If the interconnects have significant resistance, they should be treated as lossy transmission lines. When the line resistance becomes larger than the characteristic impedance, resistance dominates the electrical behavior, and the inductive effects disappear. Then the wire should be modeled as a distributed RC line. The three major causes of losses in a transmission line are

resistive loss, skin effect loss, and dielectric loss.[14]
The traces in this study were modeled as lossless
transmission lines..

3.1.2 Definitions of Electrical Parameters

In the following paragraphs, the electrical parameters most commonly encountered in transmission line analysis are defined.[14,15,16]

- Characteristic impedance (Z_0): the characteristic impedance relates the voltage step traveling down the transmission line to the current traveling down the line by an Ohm's Law type relationship. A uniform transmission line (with constant physical dimension along the length of the conductor) can be defined by its characteristic impedance and the velocity of propagation.

$$Z_0 = \left(\frac{L}{C} \right)^{\frac{1}{2}} \quad (3)$$

where L = inductance per unit length, and

C = capacitance per unit length.

The inductance and the capacitance for the above conditions are reciprocal relationships in equation (3), so impedance can be determined by methods for estimating just

one parameter, for example capacitance, as indicated in equation (4).

$$Z_0 = \frac{1}{c_0 C_0 \epsilon_r} \quad (4)$$

where c_0 = velocity of light in vacuum or free space
 C_0 = capacitance per unit length in vacuum or free space.
 ϵ_r = relative dielectric constant of the medium.

The characteristic impedance of a transmission line is determined by its geometry and the properties of the material through which the electromagnetic energy of the line flows. For lossless lines, the characteristic impedance has a real value. No energy is dissipated in a lossless transmission line. Characteristic impedance cannot be directly measured on a simple impedance bridge. Characteristic impedance does not change with line length, and depends only on geometry and the material.

- Series resistance (R_s) is the dc resistance of a transmission line and is given by

$$R_s = \left(\frac{\rho l}{A} \right) (1 + k \Delta t) \quad (5)$$

where

ρ = conductor resistivity

l = line length

A = cross-sectional area

k = conductor temperature coefficient of resistance

Δt = change in temperature from 20⁰ C, and R is usually specified as a unit length parameter.

- Time delay or time-of-flight delay from one end of the line to the other end is given by

$$t_f = (LC)^{1/2} \quad (6)$$

where L and C are the total inductance and capacitance of the line.

- Velocity of propagation is given by

$$v = c_0 \epsilon_r = \frac{1}{(LC)^{1/2}} \quad (7)$$

These relationships do not apply to lossy lines, multiconductor structures, and inhomogeneous dielectrics. In many cases the following equation relating the characteristic impedance and inductance of a homogeneous line can be applied to lossy lines and inhomogeneous structures as a reasonable approximation.[14]

$$Z_0 = \frac{\epsilon_r^{1/2}}{c_0 C} \quad (8)$$

- ϵ_r - the relative dielectric constant, is a dimensionless quantity and is given by

$$\epsilon = \epsilon_0 \epsilon_r \quad (9)$$

where, $\epsilon_0 = 8.854 \times 10^{-12} \text{ F/m} = 0.225 \text{ pF/inch}$, is the permittivity of free space, and ϵ is the dielectric constant. The relative dielectric constant of air is 1.

For calculating mutual capacitance and mutual inductance, the formula sets given in reference [18] can be used. As the separation of the conductors decreases, the coupled noise increases. Field solvers, discussed in the next chapter, are necessary to calculate the effect of coupling.

CHAPTER 4

FIELD SOLVERS

To get better than 10 percent accuracy in calculated data and to analyze non regular structures, 2D or 3D field solvers are required. For the purpose of this study, results from three field solvers from Contec Micro-electronics, Quad Design, and Integrity Engineering (CALIF), were used.

The first requirement of using the field solvers is to establish a material and geometry file. The geometry file was prepared from the physical measurements of the cross-sections of the printed circuit board used for this study. These data provided information on the trace widths, trace thicknesses, trace spacings, distance of the traces from the ground planes and the total dielectric thickness. In case of the microstrips, a sufficiently thick layer of air was assumed to be covering the traces. The separation distances were measured from the centerline of one trace to the centerline of the other. Contec and Calif used the trapezoidal geometry of the etched traces as inputs, whereas Quad averaged the top and bottom widths to get an average width for the traces. The material file mainly consisted of the resistivity of the ground plane material, the resistivity of

the trace material and the relative dielectric constant. In case of the microstrips, the relative dielectric constant for air was taken to be 1. Contec calculated and displayed the effective dielectric constant for microstrip, but the other two field solvers did not show calculated value of the effective dielectric constant for the microstrip structure. The field solvers calculated the effective dielectric constant and capacitance per unit length. All the other parameters were derived and displayed. The characteristic impedance of the individual lines was calculated from the diagonal elements of the LC matrices and displayed. In terms of input parameters, Contec also could use frequency and the loss tangent. All the three field solvers displayed information about cross-talk coefficient. But the cross-talk can also be calculated from the capacitance matrix as (C_{12} / C_{11}) and (C_{13} / C_{11}) , etc. Similarly the relative inductive coupling terms can be calculated from (L_{12} / L_{11}) and (L_{23} / L_{22}) , etc. Comparing the inductance matrices, the variations in self and mutual inductance with increased ground plane separation can be found.

CHAPTER 5

TDR AND NETWORK ANALYZER MEASUREMENTS

Three different sets of measurements were carried out with the test board: time domain reflectometry (TDR) using a Tektronics 1502B Metallic TDR Cable Tester, frequency domain measurements using a HP 4195A Network/Spectrum Analyzer with 41951-69001 HP Impedance Adapter, and S-Parameter measurements using the HP 4195A Network/Spectrum Analyzer.

5.1 Time Domain Reflectometry (TDR)

The TDR employs a step generator and an oscilloscope in a closed loop system. The TDR sends a very fast edge down a transmission line to a test device and then measures the reflection from that device. The measured reflection helps in designing signal path interconnects and transmission lines in IC packages, PC board traces, and coaxial connectors. Information obtained from the incident and the reflected voltage waves, monitored by the oscilloscope at a particular point on the line, helps in the design process. The reflected signal reveals the characteristic impedance of the line and shows both the position and the nature (resistive, inductive, or capacitive) of each discontinuity along the line. In a typical TDR setup, the step generator

produces a positive-going incident wave that is applied to the transmission system under test. The step travels down the transmission line at the velocity of propagation of the line. If the load impedance is equal to the characteristic impedance of the line, no wave is reflected and all that will be seen on the oscilloscope is the incident voltage step, recorded as the wave passes the point on the line monitored by the oscilloscope. If a mismatch exists at the load, part of the incident wave is reflected. The reflected voltage wave will appear on the oscilloscope display algebraically added to the incident wave.[19] A basic setup for the TDR, along with TDR displays for typical loads, is shown in Figure 16 and Figure 17. A printout from the TDR is shown in Figure 18. In the printout, the first horizontal part of the plot shows the reading of the controlled impedance calibration cable with $Z_0 = 50\Omega$. The TDR measured impedance of the cable and the TDR was calibrated to 50Ω . The cable was then connected to the trace of the PCB via the SMA connector. The immediate steep drop that is seen in the TDR plot was due to the capacitance of the SMA connector. If the PCB trace had a characteristic impedance of 50Ω , then there would be no reflection and a flat line showing 50Ω would be seen. The PCB trace undergoing the test had a characteristic impedance of 50.5Ω , therefore the line was slightly higher as evident from Figure 18. The

display continued at the same characteristic impedance till incident wave reached the end of the trace at which point

Figure 3. A Time Domain Reflectometer.

Figure 4. Oscilloscope Display When $E_r = 0$

Figure 16. Basic TDR Setup with Oscilloscope Display^[19]

(A) OPEN CIRCUIT TERMINATION ($Z_L = \infty$)

(A) $E_r = E_i$ THEREFORE $\frac{Z_L - Z_0}{Z_L + Z_0} = +1$
 WHICH IS TRUE AS $Z_L \rightarrow \infty$
 $\therefore Z = \text{OPEN CIRCUIT}$

(B) SHORT CIRCUIT TERMINATION ($Z_L = 0$)

(B) $E_r = E_i$ THEREFORE $\frac{Z_L - Z_0}{Z_L + Z_0} = -1$
 WHICH IS ONLY TRUE (FOR FINITE Z_0)
 WHEN $Z_L = 0$
 $\therefore Z = \text{SHORT CIRCUIT}$

(C) LINE TERMINATED IN $Z_L = 2Z_0$

(C) $E_r = +\frac{1}{3} E_i$ THEREFORE $\frac{Z_L - Z_0}{Z_L + Z_0} = +\frac{1}{3}$
 AND $Z_L = 2Z_0$

(D) LINE TERMINATED IN $Z_L = \frac{1}{2} Z_0$

(D) $E_r = -\frac{1}{3} E_i$ THEREFORE $\frac{Z_L - Z_0}{Z_L + Z_0} = -\frac{1}{3}$
 AND $Z_L = \frac{1}{2} Z_0$

Figure 17. TDR display for typical loads [19]

it encountered an open termination with $Z_{Load} = \text{infinity}$. The reflected wave at this point equaled the transmitted wave and the display jumped up immediately, showing that the end of the line was reached. The big dip at the beginning of the trace indicated a high capacitive loading and implied that the via design of the board should be modified.

Figure 18. TDR display showing Z_0 readings.

The vertical scale in Figure 18 shows the reflection coefficient ρ . Each division is equal to 25 mp. The horizontal scale shows the distance traveled by the signal and each division is equal to 0.5 ft. The reflection coefficient ρ is related to Z_L by the equation^[19]

$$\rho = \left(\frac{Z_L - Z_0}{Z_L + Z_0} \right) \quad (10)$$

where Z_L = Impedance of the conductor to be measured,

and Z_0 = Characteristic Impedance of the reference cable = 50Ω .

Based on equation (10) and the TDR display shown in Figure 18, the characteristic impedance of the conductor can be calculated. A sample calculation is shown below to demonstrate the accuracy of measurements of the TDR. From Figure 18, the average value of the reflection coefficient is measured to be 0.015. Therefore, rearranging equation 10 and substituting the values of the reflection coefficient and Z_0 ,

$$Z_L = \frac{50(1+0.015)}{(1-0.015)} = 51.52\Omega$$

The measured value of the characteristic impedance of the conductor as shown in Figure 18 is 50.5Ω . The difference between the measured and the analytical value is $\Delta Z = (50.5 - 51.52)\Omega = -1.02\Omega$. This corresponds to a difference of 2.02 percent and shows that measurements of the TDR are quite reliable.

5.2 Network Analyzer - Impedance Measurement.

The HP 4195A network/spectrum analyzer with HP 41951A[20] impedance measurement kit was used to measure the characteristic impedance and the relative dielectric constant. The setup can be used to measure impedance

directly. The relative dielectric constant was found from calculation by using the measured value of the scattering parameter s_{12} .

To measure impedance, it was necessary to perform 1-port Full calibration[20]. The calibration sequence is given below:

1. Press the CAL key.
2. Press the CAL menu softkey.
3. Press the ONE PORT FULL CAL softkey.
4. Press the OPEN soft key.
5. Connect the OS (OPEN) termination to the 41951A's 7 mm connector and press the ENTER key.
6. Press the SHORT softkey.
7. Replace the OS (OPEN) termination with the 0Ω (SHORT) termination and press the ENTER key.
8. Press the LOAD softkey.
9. Connect the $50\ \Omega$ (LOAD) termination and press the ENTER key.
10. Press the return softkey.
11. Press the CORRECTION on/off to enable correction (on/off).

After the preceding procedure is performed, the HP 4195A eliminates the measurement errors due to the HP 41951A Impedance Test Kit, and gives the best impedance measurement accuracy at the 7 mm connector.

The calibration cable was calibrated to 50Ω at the end of this procedure. The network analyzer was configured to measure impedance. The starting frequency was selected to be 1 MHz and the end frequency was selected to be 150 MHz. The resolution band width (RBW) was fixed at 10 KHz and all the measurements were done at 100.085 MHz. First the calibrated cable was connected to one end of a trace on the test board and the Z_{open} reading was read off the screen of the analyzer. Next, the other end of the trace was shorted and the Z_{short} reading was noted. The characteristic impedance was calculated from $Z_0 = (Z_{open} * Z_{short})^{1/2}$. The reflected wave for short was nearly 180° out of phase with the reflected wave of the open termination as was shown in Figure 17.

5.3 Network Analyzer - Scattering Parameter Measurements.

To calculate the velocity of propagation, the scattering parameter s_{21} was measured as described below.

The analyzer was configured to measure s_{21} and the test board was setup for through connection by hooking up the R1 port (reference port) of the analyzer to one end of a 8" trace of the PCB and the other end of the trace was connected to port T (test port) of channel 2 of the analyzer. The Reference port was connected to the 41951-69001 HP Impedance Test Adapter^[20] and was terminated by a 50 ohm

load. The output from the test kit was connected to the PCB with a 50 ohm cable. The analyzer was formatted to measure the ratio T/R (in dB). The display was set to rectan X-A & B and continuous signal sweep mode was selected. The starting frequency was selected to be 1 MHz and the end frequency was selected to be 150 MHz. The resolution bandwidth was selected to be 100Hz. The normalization procedure was performed by the following method:

1. Press the CAL key.
2. Press the S-Parameter key.
3. Press the S-Parameter CAL Menu key.
4. Press the NORMALIZE(through) key.
5. Press the THRU key.
6. Press the ENTER key.
7. Press the RETURN soft key when the analyzer screen displays the message "THRU CAL completed".
8. Press the CORRECTION on/off soft key for correction.
9. TRIG ON to complete calibration.

Once the calibration was completed, the reading for the trace was taken. After taking the reading for the 8" trace, similar reading for the corresponding 2" trace of the test board was measured. Only the phase reading of the measurement was needed to find out the s_{21} parameter. The difference in the values of the two readings would give the

s_{21} values of a 6" trace. This procedure was adopted to compensate for the capacitive loading of the connector pins. As can be seen from Figure 18 shown earlier, there was a big capacitive drop in the Z_0 measurements by the TDR. This process eliminated the readings from both the ends, thus ensuing that the results for the 6" length will be disturbance free. s_{21} (phase) is related to TOF by the following formula:

$$s_{21}(\text{phase}) = \omega \times \text{TOF} \quad (11)$$

$$\text{TOF} = \frac{d}{v_p} \quad (12)$$

where d = distance traveled and v_p = propagation velocity

$$v_p = \left(\frac{c_0}{\epsilon_r^{1/2}} \right) \quad (13)$$

$$\epsilon_r = \left(\frac{c_0}{v_p} \right)^2 \quad (14)$$

The relative dielectric constant was calculated for a few interconnects, for microstrips as well as striplines. The results were used in normalizing the simulated values of

the characteristic impedance. The calculated values of ϵ_r from s_{21} measurements are shown in Table 1.

Table 1. Relative Dielectric Constant Calculated From Scattering Parameter s_{21} .

Trace	Layer	s_{21}			TOF, nsec	v_p , in/nsec	ϵ_r
		δ'' (deg)	ϕ'' (deg)	δ'' (rad)			
A1	1A1	41.80	7.79	0.59	0.94	6.36	3.56
A2	1A2	41.86	8.85	0.58	0.92	6.56	3.35
A5	1B2	41.34	6.77	0.60	0.96	6.26	3.68
A4	1B1	39.54	5.40	0.60	0.95	6.34	3.59
A6	1B3	40.49	4.91	0.62	0.99	6.08	3.90
B2	3A2	45.65	8.45	0.65	1.03	5.82	4.26
C2	5E2	47.60	9.61	0.66	1.05	5.70	4.44
E1	8H1	47.83	10.58	0.65	1.03	5.81	4.27
E2	8H2	46.53	8.82	0.66	1.05	5.74	4.38
E9	8I3	45.34	8.92	0.64	1.01	5.94	4.08

The first column shows the trace nomenclature. The second column shows the actual position of the trace, such as 1A1 refers to layer 1, section A, and trace number 1. Under s_{21} , the first two columns show the values of s_{21} in degrees and the third column shows the difference between the first two columns in radians. The next two columns give the calculated values of the time-of-flight (TOF) and the

velocity of propagation and the last column gives the calculated value of the relative dielectric constant for a particular layer.

From the tabulated results, it can be seen that the value of ϵ_r varied from layer to layer. For microstrips the average effective relative dielectric constant was 3.6. The values of ϵ_r for layer 3, layer 5, and layer 8 were 4.26, 4.44, and 4.3 respectively. The value of 4.08 obtained from the highly coupled trace in layer 8, section I, was not taken into account because of possible distortion caused by cross-talk.

The reason for using three different values of ϵ_r is explained below. At the start of the project it was decided to work in several fronts in parallel to expedite the project. Therefore, the fabrication of the boards and consultation with the software vendors were carried out simultaneously. Unfortunately the laboratory arrangement for measurements was not ready when the board cross-sectioning was completed. As the time span for evaluation of the software was limited, it was decided to use the ϵ_r value supplied by the board vendor, 4.5 ± 0.3 , giving a range from 4.2 to 4.8. It was decided to normalize all the calculated results by using the measured values of the relative dielectric constant. The normalization scheme is explained in chapter 6.

CHAPTER 6

DATA NORMALIZATION

To normalize the values of characteristic impedance obtained from the field solvers, the following method was used.

The characteristic impedance varies inversely as the square root of the relative dielectric constant, [9] i.e.,

$$Z_0 \propto \frac{1}{\sqrt{\epsilon_r}} \quad (15)$$

$$\therefore \frac{Z_n}{Z_s} = \frac{\sqrt{\epsilon_s}}{\sqrt{\epsilon_n}} \quad (16)$$

where s stands for simulated value and n stands for normalized value. The right hand side of equation (16) represents the normalization factor. By substituting the measured value of the relative dielectric constant, ϵ_r , for ϵ_n , the normalized characteristic impedance can be calculated.

While values of the normalized characteristic impedance obtained as above can be used effectively for striplines, for microstrips the above method will produce errors. The measured relative dielectric constant for microstrips was actually effective dielectric constant. For striplines, the

dielectric medium was constant, but for microstrips the dielectric medium was a combination of FR-4 and the air above the board. Therefore the measured relative dielectric constant was a combination of the relative dielectric constant of both air and FR-4. The effective relative dielectric constant can be calculated for $w/h \geq 1$, where w is the width of the conductor and h is the thickness of the insulating material below the conductor, by using the following formula[21]:

$$\epsilon_{\text{eff}} = \frac{\epsilon+1}{2} + \frac{\epsilon-1}{2} \left(1 + \frac{10h}{w}\right)^{-1/2} \quad (17)$$

The effect of the conductor thickness is handled by transforming the line width , w , into an effective line width w_{eff} , with $w_{\text{eff}} > w$ to account for the thickness , t , of the metal.[21]

$$w_{\text{eff}} = w + \frac{t}{\pi} \ln \left\{ \frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left[\frac{1}{\pi \left(\frac{w}{t} + 1.10\right)} \right]^2}} \right\} \quad (18)$$

The ϵ in equation (17) is the relative dielectric constant of the conductor. The effective dielectric constant can be calculated using the above equations. These values along with the measured values are shown in Table 2.

Table 2. Effective Relative Dielectric Constant For Microstrips For Different Values of ϵ_r .

Layer	$\epsilon_r = 4.7$		$\epsilon_r = 4.5$		$\epsilon_r = 4.2$		Measured ϵ_{eff}
	$w_{eff}(\text{mil})$	ϵ_{eff}	$w_{eff}(\text{mil})$	ϵ_{eff}	$w_{eff}(\text{mil})$	ϵ_{eff}	
1A1			10.21	3.39	10.21	3.19	3.56
1A2			9.41	3.36	9.41	3.16	3.35
1B1	10.20	3.53	10.20	3.39	10.20	3.19	3.59
1B2	10.00	3.52	10.00	3.39	10.00	3.18	3.68
1B3	10.10	3.53	10.10	3.39	10.10	3.19	3.90

On the basis of the values shown in Table 2, the effective relative dielectric constants for Quad, Calif, and Contec were calculated respectively as 3.53, 3.38, and 3.18. Normalization factors for both microstrips and striplines were calculated from values shown in Table 1, Table 2, and equation (16). These values, shown in Table 3, were used to normalize the simulated values obtained by using the field solvers. No calculation was done for trace separation of

290 mils using Quad as no cross-talk or coupling effect was expected at that separation distance.

Table 3. Normalization Factors For Microstrips And Striplines

	STRIPLINE	MICROSTRIP
Contec	0.990	0.94
Calif	1.023	0.97
Quad	1.045	0.99

The values of characteristic impedance obtained from the field solvers were multiplied by the normalization factors. These normalized values were then compared with the measured values as discussed in chapter 7.

CHAPTER 7

DATA ANALYSIS

In this chapter, the measured data from the TDR measurements and the data from the network analyzer was compared to the calculated results from the three field solvers. As no cross-talk measurements were performed, so the data analysis was mainly confined to comparing the values of the characteristic impedance calculated by the three packages to the measured data as well as comparing the time-of-flight obtained from the network analyzer and the values obtained by the packages. It is to be mentioned that no calculation was made with Quad for trace separation of 290.0 mils as no coupling was expected for such a separation. Table 4 shows the measured and calculated Z_0 for microstrips and Table 5 shows the measured and calculated values of Z_0 for striplines. The first column in the tables shows the location of the conductor, 1A1 meaning layer 1, section A, conductor number 1. Under the heading of each software, the calculated and normalized values of characteristic impedance are shown. Both TDR and impedance analyzer measurements as well as the percentage difference between them are shown in the last three columns. The data from the tables were further subdivided according to the line type and line

separation and compared with the respective measured data. The data from the TDR and the impedance analyzer measurement is presented graphically in Figure 19 with an explanation.

Table 4. Measured and Calculated Values of $Z_0(\Omega)$ For Microstrips

Section	Simulated Z0						Measured Z0		%Difference Between A and T
	Contec		Quad		Calif		TDR(T)	Impedence Analyzer(A)	
	Simulated	Normalized	Simulated	Normalized	Simulated	Normalized			
1B2	46.95	44.13	48.27	47.79	45.99	44.61	48.40	47.34	-2.24
1C4	47.88	45.01	48.2	47.72	47.07	45.66	47.80	47.48	-0.67
1C3	47.33	44.49	47.39	46.92	46.51	45.11	47.70	47.59	-0.23
10H3	51.29	48.21			47.79	46.36	50.70	47.79	-6.09
1C2	47.29	44.45	47.71	47.23	46.47	45.08	48.40	47.82	-1.21
10I3	44.97	42.27	45.89	45.43	41.47	40.23	50.90	48.54	-4.86
10C2	53.63	50.41	52.71	52.18	52.99	51.40	49.80	48.88	-1.88
1C5	49.77	46.78	49.79	49.29	49.06	47.59	50.40	50.05	-0.70
1A1	51.16	48.09			51.33	49.79	52.10	50.36	-3.46
1C1	49.46	46.49	49.55	49.05	48.76	47.30	50.90	50.41	-0.97
10H2	53.95	50.71			54.95	53.30	52.60	50.53	-4.10
1B3	48.78	45.85	48.93	48.44	47.94	46.50	51.00	50.60	-0.79
1B1	49.52	46.55	49.17	48.68	48.67	47.21	51.10	51.00	-0.20
10I4	45.00	42.30	46.61	46.14	41.74	40.49	51.10	51.65	1.06
10I2	45.15	42.44	45.86	45.40	41.46	40.22	50.90	51.65	1.45
10C3	53.47	50.26	52.73	52.20	52.87	51.28	50.20	52.30	4.02
10I1	49.47	46.50	48.41	47.93	47.17	45.75	51.90	52.37	0.90
10I5	49.80	46.81	48.42	47.94	47.01	45.60	50.90	52.44	2.94
10C1	53.80	50.57	52.66	52.13	53.19	51.59	50.30	52.60	4.37
10H1	57.17	53.74			57.88	56.14	55.30	52.90	-4.54
1A2	53.60	50.38			54.56	52.92	55.20	53.85	-2.51
1A3	56.88	53.47			57.68	55.95	58.40	56.50	-3.36

Table 5. Measured and Calculated $Z_0(\Omega)$ For Striplines.

Section	Simulated Z0						Measured Z0		% Difference Between A And T
	Contec		Quad		Calif		TDR(T)	Analyzer(A)	
	Simulated	Normalized	Simulated	Normalized	Simulated	Normalized			
5D2	43.71	43.27	43.00	44.94	41.53	42.49	48.40	45.90	-5.45
3D3			44.16	46.15	42.56	43.54	49.10	46.25	-6.16
8H1	53.46	52.93			47.93	49.03	48.60	46.31	-4.94
3A3	46.11	45.65			47.02	48.10	48.20	46.41	-3.86
5G2	44.59	44.14	43.51	45.47	42.66	43.64	50.80	47.52	-6.90
5D5	43.67	43.23	42.61	44.53	41.57	42.53	50.40	47.76	-5.53
5F2	47.24	46.77	45.61	47.66	45.29	46.33	50.60	48.11	-5.18
5G5	43.65	43.21	42.69	44.61	41.82	42.78	51.00	48.72	-4.68
5 E3	43.05	42.62			39.77	40.68	47.90	48.77	1.78
3D4			44.85	46.87	42.84	43.83	49.00	48.82	-0.37
3D2			44.20	46.19	42.57	43.55	49.00	49.08	0.16
8F3	47.19	46.72	46.43	48.52	46.48	47.55	52.30	49.20	-6.30
5D3	44.85	44.40	43.57	45.53	42.76	43.74	49.00	49.27	0.55
8F2	50.18	49.68	45.25	47.29	45.68	46.73	52.30	49.30	-6.09
8H2	50.18	49.68			52.70	53.91	52.30	49.35	-5.98
8F1	53.46	52.93	45.97	48.04	46.03	47.09	52.30	49.38	-5.91
3D5			45.30	47.34	43.96	44.97	49.60	49.56	-0.08
5D1	45.06	44.61	43.87	45.84	42.96	43.95	50.60	49.81	-1.59
3B2	44.48	44.04	43.17	45.11	42.22	43.19	49.30	49.90	1.20
3D1			45.20	47.23	44.15	45.17	50.00	50.10	0.20
3A2	48.84	48.35			51.20	52.38	50.60	50.15	-0.90
3B3	45.63	45.17	43.84	45.81	43.50	44.50	49.70	50.20	1.00
5 E2	45.43	44.98		0.00	51.46	52.64	50.40	50.24	-0.32
5G1	45.25	44.80	44.60	46.61	43.34	44.34	51.00	50.54	-0.91
5G3	44.68	44.23	43.21	45.15	42.78	43.76	50.40	50.63	0.45
3B1	46.4	45.94	44.33	46.32	44.23	45.25	50.50	50.64	0.28
5F1	46.59	46.12	45.27	47.31	44.68	45.71	50.80	51.00	0.39
5D4	44.67	44.22	42.89	44.82	42.64	43.62	50.10	51.02	1.80
5 E1	49.26	48.77			47.09	48.17	54.50	51.04	-6.78
8I3	36.03	35.67	35.93	37.55	31.33	32.05	52.00	51.26	-1.44
5D6	44.58	44.13	43.75	45.72	42.83	43.82	50.60	51.34	1.44
5G4	44.14	43.70	42.82	44.75	42.31	43.28	52.30	51.37	-1.81
3A1	52.12	51.60			52.41	53.62	54.00	51.60	-4.65
5G6	43.74	43.30	42.80	44.73	41.93	42.89	51.40	51.83	0.83
8I5	38.13	37.75	39.37	41.14	34.70	35.50	51.10	52.14	1.99
8I4	36.03	35.67	37.79	39.49	31.22	31.94	51.10	52.21	2.13
8H3	53.46	52.93			54.54	55.79	55.20	52.33	-5.48
8I2	37.23	36.86	36.67	38.32	31.94	32.67	52.20	52.56	0.68
8I1	42.73	42.30	40.25	42.06	37.86	38.73	52.20	52.91	1.34

Figure 19 compares the values of Z_0 measured by the TDR with the values measured by the network analyzer. These values compare favorably. This is important because it lends credibility to the measurement process and gives a reference for comparing the calculated values.

Figure 19. Measured $Z_0 (\Omega)$, TDR vs. Network Analyzer.

The scattering of the data in Figure 19 is $\pm 3.0\%$. The straight line has a slope of one and shows the deviation of the analyzer data from the TDR data. In all the subsequent plots, this line with the slope of one will be shown to highlight the deviation of the calculated data from the

measured data. As shown in Chapter 5, the TDR measurements may have a deviation of $\pm 2\%$ from the analytical result. Network analyzer measurements were taken at 100 MHz for measuring Z_0 .

As the data from the TDR and the network analyzer for characteristic impedance measurements compare favorably, the calculated data will mainly be compared with the TDR results. Table 6 below gives a comparison for the calculated and measured data for microstrips with 290 mils separation.

Table 6. Measured and Calculated Values of $Z_0(\Omega)$ For Microstrips At 290 mils Separation.

Section	$Z_0(\text{ohms})$			
	TDR	Analyzer	Contec	Calif
10H3	50.7	47.79	48.21	46.36
1A1	52.1	50.36	48.09	49.79
10H2	52.6	50.53	50.71	53.3
1A2	55.2	53.85	50.38	52.92
10H1	55.3	52.9	53.74	56.14
1A3	58.4	55.1	53.47	55.95

Referring to Table 6 and Figure 20 and Figure 21, a close correlation between the measured and the calculated values was observed. In comparing the calculated values, normalized values as explained in Chapter 6 were used. These data compared very well with the measured data. A best fit line for each set of data was plotted using a

linear regression. The deviation from the unit slope line was used to measure the difference between the measured and calculated values. This approach was followed in all subsequent data analysis and plots. The maximum difference for Calif results was 2 percent and for Contec was 5 percent from the TDR measurements. This showed that for 290 mils separation both the field solvers produced good results. Figure 21 presents the same data compared to network analyzer measurements. The calculated values of Calif were

Figure 20. Measured Z_0 And Calculated Z_0 At 290 mils Separation, TDR Measurements.

Figure 21. Measured Z_0 And Calculated Z_0 At 290 mils Separation, Network Analyzer Measurements.

higher by 2 percent and the values from Contec were lower by 2 percent than the measured values of the network analyzer. Therefore it can be inferred that at large separation both of these field solvers worked well.

In reviewing the data for the microstrips with a separation distance between 3.5 mils and 10 mils, it was observed that as the separation distance decreased, the calculated values of the characteristic impedance started falling below the measured values. This effect became apparent below 10 mils separation. The values obtained from Quad design compared

best with the measured data in the separation range of 3.5 mils to 10 mils. At 1 mil separation, these differences became more prominent, with some values given by Calif differing by as much as 19%. The values obtained from Contec showed similar trends as Calif. These observations are presented in Tables 7 and 8 and Figures 22-24. At 10 mils separation, calculated values obtained from all the

Table 7. Measured and Calculated Values of Z_0 For Microstrips with Separation Distance Between 3.5-10 mils.

Section	S in mils	$Z_0(\text{ohms})$				
		TDR	Analyzer	Contec	Quad	Calif
1C3	4.00	47.70	47.59	44.49	46.92	45.11
1C4	4.00	47.80	47.48	45.01	47.72	45.66
1B2	3.50	48.40	47.34	44.13	47.79	44.61
1C2	4.00	48.40	47.82	44.45	47.23	45.08
10C2	9.60	49.80	48.88	50.41	52.18	51.40
10C3	9.50	50.20	52.30	50.26	52.20	51.28
10C1	9.60	50.30	52.60	50.57	52.13	51.59
1C5	4.00	50.40	50.05	46.78	49.29	47.59
1C1	4.00	50.90	50.41	46.49	49.05	47.30
1B3	3.50	51.00	50.60	45.85	48.44	46.50
1B1	3.60	51.10	51.00	46.55	48.68	47.21

three solvers were within 5 percent of the measured data. At 3.5 mils, results from Contec and Calif varied by as much as 7 percent. The variations for Quad in this range were the lowest amongst the three at approximately 4 percent. All three solvers produced results that were still well

below 10 percent range and still can be used to predict the characteristic impedance within an acceptable limit. This was not true in the case of 1 mil trace separation, as is evident from the data presented in Table 8 and Figure 24.

Table 8. Measured and Calculated Values of Z_0 For Microstrips with Separation Distance of 1 mil.

Section	$Z_0(\text{ohms})$				
	TDR	Analyzer	Contec	Quad	Calif
10I3	50.90	48.54	42.27	45.43	40.23
10I2	50.90	51.65	42.44	45.40	40.22
10I5	50.90	52.44	46.81	47.94	45.60
10I4	51.10	51.65	42.30	46.14	40.49
10I1	51.90	52.37	46.50	47.93	45.75

Figure 22. Measured Z_0 And Calculated Z_0 At 3.5-10 mils Separation, TDR Measurements.

Figure 23 Measured Z_0 vs. Calculated Z_0 , For Microstrips
At 3.5-10 mils separation, Network Analyzer
Measurements

From Figure 23, comparing the best fit line of the three software values respectively with the unit slope line, it was observed that results from Quad varied by 1.6 percent from the measured analyzer values. The values given by Calif and Contec varied by 4.6 and 6.4 percent respectively. It can be inferred that at small separation distances Quad produced comparatively better results. From the above discussions, it was observed that at separation distances of 3.5 mils and above, all the three software values were within 7 percent of the measured values whereas at 1 mil

separation, the differences tend to be much more as shown in Figure 24.

Figure 24. Measured Z_0 vs. Calculated Z_0 For Microstrips At 1 mil separation, TDR measurements.

No effort was made to plot best fit lines with the data of Figure 24. The scatter in the data was very high. From Table 8 it was calculated that in an average, the values given by Contec, Quad, and Calif differed by 13.84, 8.95, and 17.00 percent respectively from the TDR measured values, with maximum differences of 17.22, 10.80, and 20.99 percent respectively. Obviously at such close separation none of the software produced acceptable results. It is worth mentioning that it is very difficult to maintain a constant

physical separation of 1 mil along the length of the conductor. The error in the physical separation along the length of the conductor may be as high as 10 percent. The noise in such close coupled line also will effect the measured value to a great extent. The combination of these two factors alone may skew the calculated results.

The data from stripline measurements and software calculations was analyzed next. The values for asymmetrical striplines at 290 mils separation are shown in Table 9 and are plotted on Figure 25.

Table 9. Measured vs Calculated Z_0 For Asymmetrical Striplines AT 290 mils Separation.

Section	w in mils*.	Z_0 (ohms)			
		TDR	Analyzer	Contec	Calif
3A3	8.25	48.20	46.41	45.65	48.10
8H1	7.85	48.60	46.31		49.03
3A2	7.30	50.60	50.15	48.35	52.38
8H2	6.85	52.30	49.35	49.68	53.91
3A1	6.30	54.00	51.60	51.60	53.62
8H3	5.90	55.20	52.33	52.93	55.79

* w = average width of the traces in mils.

From the above it was observed that the values given by both the field solvers were within 5 percent of the measured values of the TDR. These values were plotted in Figure 25 and the close correlation was evident from the plot. This further strengthened the observation made during the micro-

strip analysis that both Contec and Calif performed satisfactorily for large separation between conductors.

Figure 25. Measured Z_0 vs. Calculated Z_0 For Asymmetrical Striplines At 290 mils Separation

The calculated values and measured values for separation distance of 5.0-10 mils are shown in Table 10. Traces in the respective layers, namely layer 3, section B and section D, and layer 8, section F, were symmetrical striplines. The corresponding plot is shown in Figure 26. As can be seen from Figure 26, the values given by Quad and Calif followed a pattern that was consistently lower by 6 to 10 percent

respectively for 5 mil separation than the analyzer values.
The values for 10 mil separation compared better with the

Table 10. Measured vs. Calculated Z_0 For Symmetrical Striplines At 5.0-10 mils separation.

Section	$Z_0(\text{ohms})$				
	TDR	Analyzer	Contec	Quad	Calif
3D3	49.10	46.25		46.15	43.54
3D4	49.00	48.82		46.87	43.83
3D2	49.00	49.08		46.19	43.55
8F3	52.30	49.20	46.72	48.52	47.55
8F2	52.30	49.30	49.68	47.29	46.73
8F1	52.30	49.38	52.93	48.04	47.09
3D5	49.60	49.56		47.34	44.97
3B2	49.30	49.90	44.04	45.11	43.19
3D1	50.00	50.10		47.23	45.17
3B3	49.70	50.20	45.17	45.81	44.50
3B1	50.50	50.64	45.94	46.32	45.25

Figure 26. Measured vs. Calculated Z_0 For Symmetrical Striplines At 5.0-10 mils Separation.

measured values and was 2.6 percent lower than the measured value for Quad and 4.3 percent lower than the measured value for Calif. The values obtained from Contec showed two different trends. The values from Contec for symmetrical striplines were 5 to 7 percent higher than the measured values for 10 mils separation and approximately 10 percent lower than the measured values for 5 mils separation. The trend can be clearly seen in Figure 26. The values for offset striplines are shown in Table 11 below.

Table 11. Measured and Calculated Z_0 For Offset Striplines At 290 mils Separation.

Section	w in mils*	$Z_0(\text{ohms})$			
		Contec	Calif	TDR	Analyzer
5 E3	8.5	42.62	40.68	47.9	48.77
5 E2	7.6	44.98	52.64	50.4	50.24
5 E1	6.35	48.77	48.18	54.5	51.04

*w = average width of the trace in mils.

These values differed by more than 13 percent for Calif and Contec.

Next, the two broadside coupled sets of striplines were investigated. In each layer, namely layer 5/6, section D and section G, the trace geometry was similar, the separation between each layer was also equal. But in layer D, the trace separation was 5.5 mils, and in layer G, the trace

separation was 10.3 mils. The results for layer 5/6 D and layer 5/6 G are shown in Table 12 and Table 13 respectively.

Table 12. Measured vs. Calculated Z_0 For Broadside Coupled Striplines At 5.5 mils Separation.

Section	$Z_0(\text{ohms})$				
	TDR	Analyzer	Contec	Quad	Calif
5D2	48.40	45.90	43.27	44.94	42.49
5D3	49.00	49.27	44.40	45.53	43.74
5D4	50.10	51.02	44.22	44.82	43.62
5D5	50.40	47.76	43.23	44.53	42.53
5D1	50.60	49.81	44.61	45.84	43.95
5D6	50.60	51.34	44.13	45.72	43.82

Table 13. Measured vs. Calculated Z_0 For Broadside Coupled Striplines At 10.0 mils Separation.

Section	$Z_0(\text{ohms})$				
	TDR	Analyzer	Contec	Quad	Calif
5G3	50.40	50.63	44.23	45.15	43.76
5G2	50.80	47.52	44.14	45.47	43.64
5G5	51.00	48.72	43.21	44.61	42.78
5G1	51.00	50.54	44.80	46.61	44.34
5G6	51.40	51.83	43.30	44.73	42.89
5G4	52.30	51.37	43.70	44.75	43.28

As can be observed from Table 12 and Table 13, all the three field solvers calculated values for Z_0 that were consistently lower than the values measured by either the TDR or the network analyzer. The results of 5.5 mils and 10 mils separation did not show any significant variations

amongst the three. The plots for these two configurations are shown in Figure 27 and Figure 28 respectively.

Figure 27. Measured vs. Calculated Z_0 For Broadside Coupled Striplines At 5 mil separation.

From Figure 27 it is seen that for 5 mil separation and broadside coupled striplines, the values calculated by Calif and Contec differed from network analyzer measurements by 10 percent and 11 percent respectively. Calculated values from Quad varied by 7 percent. From Figure 28, all the above three variations are observed to be 12.8, 12.4, and 9.6

percent respectively for Calif, Contec and Quad for the same structure and 10 mil separation. All the values for broadside coupled striplines were consistently lower than the measured values obtained from both the TDR and the network analyzer. This suggests that though these structures can be adequately modeled for an initial design calculation by using any of the three field solvers, for actual design of the structures, the field solvers may produce erroneous results.

Figure 28. Measured and Calculated Z_0 For Broadside Coupled Striplines At 10 mils Separation.

CHAPTER 8

DISCUSSION

The measured data from the TDR and the network analyzer compared very well. The values of characteristic impedance obtained from the analyzer measurements were generally 2 to 4 percent lower than the measured values from the TDR. In cases where the separation distance was 1 mil and in a few cases of broadside coupled striplines, the data from the analyzer was approximately 3 percent higher than the values measured by the TDR. Thus both the TDR and the analyzer data can be used as a reference for comparison. In the plots, Figure 20 through Figure 28, the straight lines drawn with a slope of one show the expected behavior of the calculated values compared to the measured values.

In case of microstrips, the transition point for the calculated values seems to be between 10.0 mils and 3.5 mils separation distance. Till 10 mils separation, the values calculated by the field solvers were on average 2 to 3 percent higher than the network analyzer results. Below 10 mils, the values started differing by as much as 5 percent for 3.5 mils separation and by 8-13 percent for 1 mil separation. Below 10 mils separation, all the calculated values were lower than the measured values. This suggests

that up-to 3.5 mils separation distance, all three field solvers used in the study can be expected to give a satisfactory result. Below 3.5 mils separation, the field solver results are not useful. For close coupled lines, Quad produced results that varied the least from the measured data.

For loosely coupled symmetrical and asymmetrical striplines, the transition point was above 10 mils separation. Calif and Contec calculated results that deviated by 4 percent from the data measured by the analyzer for trace separation of 290 mils. These values were higher than the measured values. For separation of 10 mils or below, the results from all the field solvers were uniformly lower than the measured data by 4 to 12 percent. Here also results from Quad were better in comparison. Only three data points for offset striplines were available and the separation distance was 290 mils. This did not provide enough data for comparison.

In calculating the value of the relative dielectric constant, ϵ_r , the values obtained from the loosely coupled lines were considered to ward off the effect of coupling. The average values of the effective relative dielectric constant to be used with microstrip and stripline layers were calculated as 3.6 and 4.33 respectively. The value of ϵ_r for the stripline layers compared well with the vendor

supplied data of 4.5 ± 0.3 . As Calif and Quad did not display the values of the effective relative dielectric constant, these values were not compared.

This study provides a groundwork for analyzing the applicability of field solvers in the initial design process of printed circuit boards. More research needs to be done to achieve a comprehensive understanding of the suitability of the field solvers in the design process.

CHAPTER 9

CONCLUSION

The objective of this study was to evaluate commercially available software tools for modeling printed circuit board interconnects. The applicability of the tools in the PCB design process was also analyzed. This objective was largely satisfied based on the following conclusions:

1. All the three field solvers produced satisfactory results for loosely coupled lines. The calculated values of Z_0 were within 5 percent of the measured values.
2. The effect of coupling became prominent as the separation distance decreased, specially below 10 mils when the ratio of the separation distance to the width of the conductor became small. For microstrips, the calculated values started deviating from the measured values around this point. For striplines the transition point, where the calculated values started deviating from the measured values, was above 10 mils spacing. All the calculated values for striplines were lower than the measured values below 10 mils separation. The values were still approximately within 10 - 15 percent of the measured values. Caution should be applied in using the field solvers for close coupled lines.

3. None of the three field solvers produced satisfactory results for close coupled lines (3.5 mils or below).

4. As the field solvers were very easy to use, adding them in the initial design process would help the designer to cut the design time. This would also help in the initial discussions with the PCB fabrication vendors regarding selection of interconnect geometry.

One observation is appropriate at this point. As the field solvers were based on the geometry as well as the material data, it was essential that the measurements for the relative dielectric constant should have been done before the modeling process. This could not be done during this study because of delay in getting access to the lab equipment.

9.1 Suggested Future Research

All the comparisons in the study were based on interconnect separation distances. The field solvers produced information about cross-talk and coupling. These should be verified by cross-talk measurements. In the present study, data from only one test board was used. More data from different boards will permit arriving at a better correlation about the applicability of the field solvers.

In this study, only three field solvers were used. In the market there are several more field solvers and simulators available. To get a comprehensive evaluation, it is necessary to compare more of them. The effect of operating frequency was not studied in this project. Quad and Calif did not use frequency as an input. The effects of frequency need to be investigated.

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