1995

Copper tin intermetallic compounds in flip chip interconnections

B. J. (Brian John) Lynch
San Jose State University

Follow this and additional works at: https://scholarworks.sjsu.edu/etd_theses

Recommended Citation

Lynch, B. J. (Brian John), "Copper tin intermetallic compounds in flip chip interconnections" (1995).
Master's Theses. 1087.
DOI: <https://doi.org/10.31979/etd.g3jg-zjcd>
https://scholarworks.sjsu.edu/etd_theses/1087

This Thesis is brought to you for free and open access by the Master's Theses and Graduate Research at SJSU ScholarWorks. It has been accepted for inclusion in Master's Theses by an authorized administrator of SJSU ScholarWorks. For more information, please contact scholarworks@sjsu.edu.

INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps. Each original is also photographed in one exposure and is included in reduced form at the back of the book.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

UMI

A Bell & Howell Information Company
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
313/761-4700 800/521-0600

**COPPER TIN INTERMETALLIC COMPOUNDS IN FLIP CHIP
INTERCONNECTIONS**

A Thesis

Presented to

**The Faculty of the General Engineering Department
San Jose State University**

**In Partial Fulfillment
of the Requirements for the Degree
Masters of Science**

by

Brian John Lynch

August 1995

UMI Number: 1375711

Copyright 1995 by
Lynch, Brian John
All rights reserved.

UMI Microform 1375711
Copyright 1995, by UMI Company. All rights reserved.

This microform edition is protected against unauthorized
copying under Title 17, United States Code.

UMI

300 North Zeeb Road
Ann Arbor, MI 48103

© 1995

Brian John Lynch

ALL RIGHTS RESERVED

APPROVED FOR THE GENERAL ENGINEERING DEPARTMENT

Dr. Guna S. Selvadurai

Dr. Avtar Singh

Dr. Peter Gwozdz

APPROVED FOR THE UNIVERSITY

M. Lou Lewandowski

ABSTRACT

COPPER TIN INTERMETALLIC COMPOUNDS IN FLIP CHIP INTERCONNECTIONS

by Brian John Lynch

Copper tin intermetallic compounds found in flip-chip type microelectronic interconnections were investigated, with a focus on the thermal-mechanical and electrical reliability of these intermetallic compounds during temperature cycling and high temperature aging. In addition to electrical and mechanical testing, the ratios and growth rate of the Sn rich Cu_5Sn_6 (η -phase) and the Cu rich Cu_3Sn (ϵ -phase) phases were measured and are reported. Specimens were fabricated by forming a copper core bump covered with eutectic Pb-Sn solder on Si wafers. The wafers were then sawed into dies and attached to alumina substrates. The assembled units and individual die were then divided into groups and subjected to various tests. The results show that two the Cu-Sn intermetallic compounds which form are the Sn rich Cu_5Sn_6 (η -phase) and the Cu rich Cu_3Sn (ϵ -phase) phases. Their presence does not significantly affect the reliability of the microelectronic interconnect.

ACKNOWLEDGMENTS

I would like to thank two companies, LSI Logic and Amkor Electronics, and their management for supporting my research efforts over the past two years. My managers have been extremely understanding in accommodating my educational advancement while continuing my professional career.

I would like to acknowledge my advisor Dr. Guna S. Selvaduray. He has helped guide this research and helped in making this work possible. He continued to support my research efforts and the writing of this thesis even after I relocated out of the area. For his understanding and patience I am eternally grateful.

Most of all I would like to thank Elizabeth, my wife, for her support and understanding while I attended the University over the past three years. Her unselfish acts and sacrifices have made this work possible.

TABLE OF CONTENTS

Abstract	iv
Acknowledgments	v
List of Tables	vi
List of Figures	vii
Chapter	
1. Introduction to Microelectronic Interconnections	1
1.1 Wire Bonding	1
1.2 Tape Automated Bonding	5
1.3 Flip Chip	6
2. Literature Review.	13
3. Research Objective	21
4. Methodology	22
4.1 Test Silicon Fabrication	22
4.2 Test Vehicle Fabrication	24
4.3 Thermal Aging	25
4.4 Thermal Cycling.	25
4.5 Metallographic Preparation	26
4.6 Microscopy and Chemical Analysis	26
5. Results	28
5.1 Thermal Aging	31

5.2 Thermal Cycling.	.	.	.	.	.	.	36
6. Discussion.	.	.	.	.	.	.	40
7. Conclusions	.	.	.	.	.	.	42
8. References	.	.	.	.	.	.	43

Tables

Table	Page
1. Pad Count for Various Die Sizes for Perimeter and Area Array Pads	8
2. Crystal Structure of Phases Present in Cu/Pb-Sn Solder Joints	16
3. Physical Properties of Package Components at 20°C .	20
4. Intermetallic Thicknesses and Phase Percentages . .	33
5. Electrical Yield after Thermal Aging	35
6. Electrical Resistance after High Temperature Aging. .	35
7. Electrical Yield after Thermal Cycling	36
8. Electrical Resistance after Thermal Cycling	37

Figures

Figure	Page
1. Thermosonic Wire Bonding	2
2. Scanning Electron Micrograph of Thermosonic Wedge Bond	3
3. Thermocompression Wire Bonding	4
4. Scanning Electron Micrograph of Thermocompression Wire Bond Type Interconnect	4
5. Tape Automated Bonding Type Interconnect.	5
6. Scanning Electron Micrograph of TAB Type Interconnect	6
7. IBM C4 Flip Chip Type Interconnect	7
8. Number of I/O Terminals vs. Electronic Content	8
9. Basic Processing Steps for An Evaporated C4 Interconnect	10
10. Micrograph of C4 Solder Bump	10
11. Pb - Sn Phase Diagram	13
12. Cu - Sn Phase Diagram	14
13. Calculated Ratio of the ϵ -Phase Thickness to the η -Phase Thickness, as a Function of Temperature.	17
14. Package Substrate Coefficient of Thermal Expansion Effect on Fatigue Life Cycles (N_{50})	19
15. Process Flow of Wafer Bumping	23
16. Chip Attach Oven Temperature Profile	24

17. Copper Core Bump After Initial Fabrication and Before Chip Attach	28
18. Energy Dispersive X-Ray Analysis of Solder Composition (Point 2)	29
19. Digital Scanning Calorimeter Plot of Copper Core Bump	29
20. Non-Wet of Copper Core Bump to Substrate Land.	30
21. Micrograph of Copper Core Bump After 100 Hours @ 170°C	31
22. Micrograph of Copper Core Bump After 1000 Hours @ 170°C	32
23. EDX Line Scan After 100 Hours @ 170°C	33
24. EDX Line Scan After 1000 Hours @ 170°C	34
25. Micrograph of "Good" Flip Chip Joint Before Underfilling	38
26. Micrograph of "Good" Flip Chip Joint Showing Cu-Sn Intermetallic Compounds	39
27. Micrograph of Flip Chip Joint After Epoxy Underfill.	39
28. Average Intermetallic Compound Thickness Versus Thermal Aging Time @ 170°C	41

Chapter 1

Introduction to Microelectronic Packaging Interconnections

Microelectronic technology has been rapidly advancing since its introduction. Current semiconductor devices can be as large as 20 mm per side and have over 2,000,000 usable gates. These VLSI (very large scale integration) devices have up to four layers of metal on the chip and attain clock speeds as high as 200 MHz. As clock speeds and logic depths increase, the packaging connecting the outside world to the chip becomes of paramount concern. The main purpose of the microelectronic interconnect is to conduct electrical signals from the outside world, through the interconnect, to the semiconductor device. The two major factors which determine the performance of an interconnect are the length of the connection from the semiconductor to the package and the number of connections which can be made to the semiconductor device. There are three distinct ways in which a semiconductor interconnection can be made.

1.1 Wire Bonding

Wire bonding is a technique where a thin wire is "stitched" from the semiconductor device bond pads to bond fingers on the package. The two major limitations of this technology are the pitch (or distance between connections) which can be attained and the inability to bond over active circuitry on the

semiconductor device. This requires that the bond pads be located on the perimeter of the semiconductor, thus limiting the number of available connections. The materials most commonly used for the wire are aluminum and gold. There are two methods for making a wire bond: thermosonic and thermocompression. Thermosonic wire bonding uses ultrasonic energy and temperature to attach the wire from the semiconductor to the package. An illustration of the wire bonding process using thermosonic or "wedge bonding" is shown in Figure 1. A scanning electron micrograph of an actual interconnection with the wedge bonds formed is shown in Figure 2.

Figure 1. Thermosonic Wire Bonding^[1]

An alternative method of wire bonding is thermocompression. A thin wire is feed through a capillary where the end of the wire is melted prior to attachment

to the semiconductor. This forms a ball on the semiconductor side of the wire; the other end of the wire is stitched to the package bond finger.

Figure 2. Scanning Electron Micrograph of Thermosonic Wedge Bond

This method, in conjunction with Au wire, limits the pad pitch to approximately 100 μm , due to the diameter of the Au wire (normally 25 to 33 μm) and the surface tension of the wire material. The ball diameter on the semiconductor pad after attachment is typically 2 to 3 times the initial wire diameter. An illustration of the wire bonding process using thermocompression or “ball bonding” is shown in Figure 3. A scanning electron micrograph of actual interconnections with the ball bonds formed is shown in Figure 4.

Figure 3. Thermocompression Wire Bonding^[2]

Figure 4. Scanning Electron Micrograph of Thermocompression Wire Bonding Type Interconnect

1.2 Tape Automated Bonding (TAB)

A technology which has been around since the 1960s is finding a rebirth because of the demands of today's semiconductor devices. Tape Automated Bonding (TAB) is an alternative method of chip to package interconnection. In this technology, the semiconductor is attached by bumps to a tape based substrate instead of a ceramic, plastic, or lead frame type package. This tape typically consists of an etched copper pattern supported on a polyimide film. Interconnect densities on the semiconductor are 1.2 to 2 times higher than that for wire bonded devices. This increase in density allows for more inputs/outputs and shorter conduction paths for the electrical signals. But like wire bonding, the bonding pads must be located on the perimeter of the semiconductor device (because of the high bonding forces required to effect the connection). An illustration of the TAB bonding process is shown in Figure 5. A scanning electron micrograph of an interconnection formed with TAB is shown in Figure 6.

Figure 5. Tape Automated Bonding Type Interconnection^[3]

Figure 6. Scanning Electron Micrograph of TAB Type Interconnect

1.3 Flip Chip

The third category of semiconductor interconnection is "flip chip." In this method bumps are deposited onto the semiconductor which is then mounted junction side down onto a substrate which has the interconnection pattern mirrored on its surface. The package is then placed into an oven and all of the joints are made simultaneously by reflowing the bumps. Since the only force acting on the chip is gravity, the bond pads can be placed over active circuitry on the semiconductor. This allows the highest possible interconnection density because of the area array pattern, while offering the shortest interconnection

length from the semiconductor to the package. An illustration of this type of interconnection is shown in Figure 7.

Figure 7. IBM C4 Flip Chip Type Interconnection^[4]

The major challenges of this technology are in the materials selection and process development. As gate widths continue to decrease beyond the sub-micron level (they are currently at 0.5 μm), and the number of layers of interconnect on the semiconductor increases, the number of required connections to the package will continue to increase. The number of pads available versus the pad pitch, for perimeter and array area type connections, for different die sizes is shown in Table 1. Thus an increasingly large number of semiconductor devices will require a "flip chip" type of interconnection in order not to increase the size, i.e., cost, of the semiconductor solely for the purpose of accommodating the number of required perimeter bond pads. The generally

accepted relationship between the number of input/output terminals required for an integrated circuit and the number of circuits supported on a chip is called Rent's rule.^[5] This relationship is represented graphically in Figure 8 and given in Equation 1.

Table 1. Pad Count for Various Die Sizes for Perimeter and Area Array Pads.

Die Size (mm)	Perimeter Pad Pitch (150 μ m)	Perimeter Pad Pitch (125 μ m)	Perimeter Pad Pitch (76 μ m)	Area Array Pad Pitch (250 μ m)
5.0	128	160	290	400
10.0	260	324	584	1521
15.0	388	488	880	3510
20.0	520	652	1178	6241

Figure 8. Number of I/O Terminals vs. Electronic Content^[6]

$$ckt = \left(\frac{N}{K} \right)^n \quad (1)$$

where

ckt = average number of circuits supported by N

K = constant, the value of which depends on the ability to share signal lines. For high performance applications, K = 2.5

n = another constant, in the 1.5 to 3.0 range. 1.79 is selected for the high performance packages in the 10 to 100,000 circuit range

N = number of signal terminals required (pinout)

For high end logic devices, such as Application Specific Integrated Circuits (ASICs) and other high end peripherals (devices which regulate memory, microprocessors, and other devices) an area array type interconnection is required in order not to increase the semiconductor size solely for the number of available I/O terminals. Such a device is referred to as "pad limited."

The industry leaders in area array interconnection have historically been IBM Corp. and Bell Laboratories. They both introduced systems using "flip chip" type technology in the mid 1960s. The bumps were deposited on the semiconductor (in the wafer form) by evaporation of high Pb content solder through a metal mask. The first layers were the barrier and ball limiting metals, followed by Pb and then Sn. After deposition, the bumps were reflowed in a H₂ furnace at about 350°C. This results in a bump with a spherical shape. The basic fabrication process is shown in Figure 9 and a micrograph of a flip chip bump is shown in Figure 10.

Figure 9. Basic Processing Steps for An Evaporated C4 Interconnection^[7]

Figure 10. Micrograph of C4 Solder Bump

All of the early work done at IBM targeted a high Pb solder, typically in the 95 to 99 % range. The substrate material was an alumina(Al_2O_3) type ceramic. The high Pb solder was used for two reasons. In the mid-sixties, ceramics were predominantly used because of their hermiticity and proven reliability. These ceramics were stable at the high temperatures used to reflow the high lead solders used in early flip chip work. The other reason was the use of near eutectic Pb/Sn solders for board attach (placement and connection of the semiconductor packages to a printed circuit board). Because the semiconductor package would be exposed to temperatures above 240°C during the package to board attach process, a higher melting solder was determined to be required at the semiconductor to package interface to prevent remelting of the connections during package to board assembly.

With the advent of reliable plastic packages and the use of epoxy based chip underfills, the requirement for high melting flip chip interconnects solely onto ceramic packages has diminished. The migration towards plastic surface mounted packages continues to be the industry direction. The use of flip chip type interconnections in plastic packages increases the demand for high thermo-mechanical performance for the interconnects due to the higher coefficient of thermal expansion (CTE) mismatch between the semiconductor and the package materials. This requirement is unique to flip chip type interconnects because of the need for the connections to provide both electrical contact and mechanical

support of the semiconductor to the package. The microelectronics industry is seeking for a low cost, highly reliable flip chip type interconnection which can be easily attached to a plastic substrate or directly to the printed circuit board. Ideally the interconnection would be easy to fabricate, melt at temperatures below 220°C, and exhibit excellent thermo-mechanical strength.

Chapter 2

Literature Review

The most widely used soldering alloys in electronics are Pb-Sn based, and the most commonly used substrate metal is copper. The Pb-Sn solder bonds to Cu by forming a layer of Cu-Sn intermetallic compound at the wetted surface.^[8] The reliability of the joint is dependent on the integrity, adhesion, and mechanical properties of the intermetallic layer. Several different Cu-Sn intermetallic compounds can form, depending on the temperature and the duration of the soldering process. Figure 11 shows the phase diagram for the Pb-Sn system and Figure 12 shows the Cu-Sn phase diagram. These phase diagrams are critical in evaluating and understanding Pb-Sn soldering to Cu.

Figure 11. Pb - Sn Phase Diagram^[9]

Figure 12. Cu - Sn Phase Diagram^[9]

The low temperature (< 400°C) intermetallic compounds formed by Sn and Cu are the Sn rich Cu_5Sn_6 (η -phase) and the Cu rich Cu_3Sn (ϵ -phase) phases. Several studies which examined the formation kinetics of the Cu-Sn intermetallics at the Cu / Pb-Sn interface have been completed, and are reviewed here.

Sunwoo, Morris, and Lucey^[10] confirmed earlier work that the η -phase forms first upon soldering and then transforms to the ϵ -phase upon high temperature aging at 70°C and 170°C. Their work focused on pre-tinned copper-

solder interfaces. The samples were oxygen free copper substrates with coatings of eutectic or high Pb (97 wt%) solders. The samples were aged at both 70°C and 170°C for up to 54 days.

Mei, Sunwoo, and Morris ^[11] developed a multiphase diffusion model to predict the growth of the ϵ - and η -phase intermetallic compound layers at a Cu-Sn interface in a semi-infinite diffusion couple. This theoretical model correlated well with Morris's later work with Lucey and also with earlier work completed by Cogan, Kwon, Klein, and Rose.^[12]

Felton ^[13] completed the first and only known work to date using TEM techniques to analyze Cu-Sn intermetallic compounds. His work focused on the morphology of the intermetallic compounds and how morphology could be controlled through the use of lasers for solder reflowing. He concluded that the existence of a particle morphology depends on the conditions under which it was reflowed and the thickness of the intermetallic compounds increased with the time of the reflow. Felton's research details the morphology of Cu-Sn intermetallics, but does not extend to predictions of mechanical properties.

Tu ^[14] reported the crystal structures of the possible phases present in a Cu-Sn solder joint. The η -phase (Cu_5Sn_6) forms a long-period superlattice at temperatures below 190°C. The ϵ -phase has a long-period superlattice and is based on the ordered orthorhombic unit cell. A summary of the possible crystal

structures of the phases present in Cu/Pb-Sn solder joints is given in Table 2, based on the work completed by Tu.

Table 2. Crystal Structure of Phases Present in Cu/Pb-Sn Solder Joints ^[13]

Phase	Structure	Lattice Parameters (Å)		
		a	b	c
Cu	fcc	4.0504		
Pb	fcc	3.6418		
Sn	bct	5.8317		3.1815
ϵ -Cu ₃ Sn	ordered orthorhombic	5.516	38.160	4.329
η -Cu ₆ Sn ₅	NiAs	4.20		5.09

Several researchers have found that both intermetallic compounds form when soldered samples containing Cu and Sn are aged at temperatures from 135 °C to 220 °C. ^{[10],[11],[13],[15]} The Cu rich Cu₃Sn (ϵ -phase) was found to form next to the Cu, and the Sn rich Cu₅Sn₆ (η -phase) next to the solder. Figure 13 shows the calculated ratio of the ϵ -phase thickness to the η -phase thickness, as a function of temperature, from the work completed by Mei, Sunwoo, and Morris. ^[10] At lower temperatures (20°C to 70°C), only the Sn rich η -phase develops. ^[16]

Four studies to date have evaluated the effects of intermetallic compound formation on the mechanical properties of Cu/Pb-Sn solder joints. Three of these studies focused on the tensile strength of the solder and one investigated controlling the Cu-Sn intermetallic compounds through controlling the available Cu and Sn.

Quan, Frear, Grivas, and Morris ^[17] studied the tensile strength of Cu/Pb-Sn-X solder joints, where X = In, Ag, Sb, or Bi. They found the main cause of failure to be due to the formation of η -phase (Cu_5Sn_6) whiskers in the solder. They also found that keeping the solder joint above 200°C for 6 hours produced large quantities of whiskers which reduced the tensile strength of the solder from 12,000 to 6,700 psi.

Figure 13. Calculated Ratio of the ϵ -Phase Thickness to the η -Phase Thickness, as a Function of Temperature ^[10]

Parent, Chung, and Bernstein ^[18] studied the tensile strength of eutectic solder and copper as a function of temperature and reflow time. Their findings indicated that failures always occurred in the intermetallic compound layers at the Cu/solder interface. They concluded that the primary factor in joint strength was controlled by the reflow temperature and that reflow time was a secondary factor.

Frear, Grivas, and Morris ^[19] studied the effects of Cu concentration on the mechanical properties of 60Sn-40Pb solder. They measured stress-strain curves for this near eutectic solder and the Pb-Sn-Cu alloy at various temperatures. They concluded that the addition of Cu did not significantly increase the yield strength of the solder, but that it did reduce the ductility of the alloy.

Aggarwal and Selvaduray ^[20] studied controlling the formation of Cu-Sn intermetallic compounds by controlling the available Cu and/or Sn in a solder bump. The thickness of the Cu layer and the concentration of the Sn in the solder bump were varied. They concluded that the stoichiometry of the Cu-Sn intermetallic compound was dominated by the kinetics of Sn transport through the liquid Pb contained in the bump and not by the overall concentration of available Cu or Sn.

In all four of these studies, no information was gathered on the performance of the Cu-Sn intermetallic compounds under thermal cycling conditions. Most solder joints will undergo some form of thermal cycling during their expected service life.

Thermal cycling is a commonly used method for simulating the temperature variations seen by electronic components. The package is transferred between air chambers at -55°C and 125°C (MIL STD 883, Condition B) or 0°C and 100°C (MIL STD 883, Condition A) at a rate of 2 cycles per hour. This test accelerates failure mechanisms related to mismatches in the thermal

expansion coefficients of the materials used in the package, interconnects, and the semiconductor. Listed in Table 3 are the material properties for the individual components found in a typical flip chip package. Figure 14 shows the effect of package substrate coefficient of thermal expansion on expected fatigue life cycles. The reduction in expected life cycles is inversely proportional to the package substrate coefficient of thermal expansion. This is attributed to an increasing thermal expansion coefficient mismatch between the package and a semiconductor connected using a 97/3 Pb/Sn flip chip interconnect.

High temperature storage is used to accelerate temperature related failure mechanisms, such as intermetallic compound formation.

Figure 14. Effect of Package Substrate Coefficient of Thermal Expansion on Fatigue Life Cycles (N_{50})^[21]

Table 3. Physical Properties of Package Components at 20°C

Material	Elastic Modulus (MPa)	Poisson's Ratio	TCE (ppm/°C)
Silicon	1.298×10^6	0.278	2.56
Copper (ED)	3.62×10^4	0.4	16.65
Alumina	3.723×10^5	0.2	7
Eutectic Solder	1.72×10^4	0.4	23.2
Underfill Epoxy	8.963×10^3	0.4	22

All of the work done to date on the formation of copper tin intermetallic compounds has focused on the rate, structure, and ratios of the intermetallic compounds present. All of the previous work has focused on the effect of intermetallic compounds on joints which are typically much larger than those used in the microelectronic packaging industry. What has not yet been researched is the effect of the intermetallic compound formation on the mechanical integrity of small solder joints.

Chapter 3

Research Objective

The goal of this project was the investigation of the composition and growth rate of the copper tin intermetallic compounds in flip chip interconnects and the determination of the thermo-mechanical reliability of these interconnects. The solder joints in this study were approximately 100 μm in diameter and connected a “flip-chip” type semiconductor device to an alumina ceramic package. The mechanical integrity of the solder joint was determined by electrical resistance measurements after high temperature aging and thermal cycling of the solder joints, according to applicable industry standards. The intermetallic compound thicknesses and compositions were measured after high temperature aging.

Chapter 4

Methodology

4.1 Test Silicon Fabrication

Semiconductor wafers were fabricated using a 0.7 μm , two layer metal CMOS process with a "daisy chain" type pattern. The die size was 13.33 mm per side and contained 240 pairs of pads on an effective pad pitch of 250 μm . The bumps (flip chip interconnections) were produced by sputtering a thin layer (1000 $\text{\AA}$) of Ti followed by a layer (5000 $\text{\AA}$) of Cu onto the semiconductor wafers. These were then coated with a thick layer of photosensitive resist, and patterned using standard wafer bumping techniques.^[22] Vias were opened in the photoresist by exposing and developing the photoresist over the bond pads of the semiconductor device. Copper was plated into the vias using electrolytic plating, resulting in a copper core of approximately 30-40 μm thick over the bond pads. With the resist still in place, 40-60 μm of eutectic solder was electrolytically plated over the copper. The height of copper and solder plated exceeded the resist thickness, thus producing a mushroomed shaped bump. The photoresist was then removed, and the sputtered Ti and Cu layers, which were not protected by the copper core, were chemically etched away. The wafers were then coated with a RMA type flux and placed in a reducing atmosphere (95% H_2 / 5% N_2) furnace at 300°C for twenty minutes. The wafers were removed and allowed to cool before the residual flux was removed with an organic based solvent

(xylene). The final shape of the bump was spherical, with a height of 95 to 105 μm . The process flow is illustrated in Figure 15.

Figure 15. Process Flow of Wafer Bumping

The wafers were then sawed into dies. The solder composition of the bumps was verified as being eutectic by physically removing the bumps from a

After chip attach, the substrates were first cleaned using xylene, an organic solvent, and then individually tested with an ohmmeter to determine the electrical resistance of the package interconnections.

4.3 Thermal Aging

Six unattached dies and 8 assembled units were subjected to high temperature storage in air at 170°C for 1000 hours.

Electrical testing of the interconnection resistance using an ohmmeter was performed on the assembled units to determine if the resistance had increased or if any of the interconnections had failed. The unattached dies were used to study intermetallic compound growth.

4.4 Thermal Cycling

The remaining 25 assembled units were then divided into two groups. Group one contained 14 units and was underfilled with an epoxy, with the expectation that the fatigue lifetime of the interconnect will be increased. Group two contained 11 units and was not underfilled. Five underfilled and four non-underfilled assembled packages were then subjected to Condition A (0 to 100 °C) temperature cycling. Nine underfilled and seven non-underfilled assembled packages were then subjected to Condition B (-55 to 125°C) temperature cycling.

4.5 Metallographic Preparation

The dies exposed to high temperature storage were coated with M-Bond® to prevent the solder from smearing during polishing, mounted onto cross sectioning stubs, and then ground using 9 and 3 μm diamond impregnated films. The samples were then polished using a slurry containing 1.0 and then 0.5 μm Al_2O_3 powders using an ECOMET 3® variable speed grinder/polisher.

The packaged units were ground using a cloth containing diamond studs. The stud sizes were 200, 68, 15, and 9 μm . After grinding, the units were then polished in a manner similar to the dies. All of the cross sectioning occurred through the bumps, perpendicular to the die surface and parallel to the die edge. After cross sectioning, the units were chemically etched with a mixture of 40% ammonium peroxide, 40% hydrogen peroxide, and 20% water for 30 seconds at room temperature. The units for EDX analysis were coated with carbon. The units for scanning electron microscopy were coated with gold. A Denton Desk II® coating system was used for coating the samples with gold or carbon.

4.6 Microscopy and Chemical Analysis

A JEOL JSM-6400 F with a Princeton Gamma-Tech EDX system was used for both the EDX analysis and scanning electron microscopy. The scanning electron microscope is made up of five major components. The vacuum pumping system is used to evacuate the specimen chamber to allow the electron beam to

act without the interference of gas atoms. The electron gun provides a narrow beam of electrons directed down the center line of the column. The magnetic lens produce a magnetic field which allows the electron beam to be focused to a very fine diameter. The scan coils cause the electron beam to scan the sample in a predetermined area, which is called the raster. The detectors are used for image formation, secondary electron detection, and X-ray signal acquisition. The primary use of a scanning electron microscope (SEM) is to produce high-resolution and depth-of-field images of sample surfaces. A secondary use is to provide chemical analyses of micron sized areas. EDX or X-ray fluorescence is an emission spectroscopic technique for determining elemental identification. The technique depends on the emission of characteristic X-rays from the excitation of atomic electron energy levels by an external energy source, such as an electron beam. A detailed description of the operations and techniques used in these systems is given in references 23, and 24. For this study, an EDX line scan analysis was used to identify the interfaces of the Cu-Sn intermetallic compounds.

Chapter 5

Results

A micrograph of a cross-section of the copper core bump, after initial fabrication, is shown in Figure 17. The elements present within the solder were identified using an EDX microprobe, at four locations within the solder, as shown in Figure 17. An EDX chemical analysis of Point 2 is shown in Figure 18. The composition of the bulk solder was verified by using a differential scanning calorimeter (DSC). The plot of the DSC scan is shown in Figure 19.

Figure 17. Copper Core Bump After Initial Fabrication and Before Chip Attach

Figure 18. Energy Dispersive X-Ray Analysis of Solder Composition (Point 2)

Figure 19. Differential Scanning Calorimeter Plot of Copper Core Bump

The phase transition temperature on the bulk solder was measured at 182.93°C, which is acceptably close to that of the eutectic temperature of 183°C shown on the Pb-Sn phase diagram in Figure 11, thus confirming that the solder was of eutectic composition.

Three of the thirty six units started into assembly had electrical opens after chip attach. All of the failures were attributable to non-wetting of the package substrate metallization by the solder bump, caused by heavy copper oxidation of the package metallization. One of the defective parts was cross sectioned and a micrograph showing the non-wetted substrate land after underfill is shown in Figure 20.

Figure 20. Non-Wet of Copper Core Bump to Substrate Land

5.1 Thermal Aging

The intermetallic compound layer thicknesses were measured using calipers on the micrograph of the samples cross sectioned after high temperature aging. The estimated average, minimum, and maximum intermetallic compound layer thicknesses were measured at various points on the copper core. The percentage of the ϵ - and η -phase intermetallic compound was determined based on the optically estimated average intermetallic compound thickness on the copper core. Micrographs of the cross sectioned copper core bumps after 100 and 1000 hours of high temperature storage are shown in Figures 21 and 22.

Figure 21 Micrograph of Copper Core Bump After 100 Hours @ 170°C

Figure 22. Micrograph of Copper Core After 1000 Hours @ 170°C

EDX line scans were taken on cross sectioned samples after 0, 100, 200, 500, and 1000 hours in high temperature storage. The scans were taken at approximately 30 μm upward from the base (Al pad / Cu core bump interface) of the copper core bump. The plots for the EDX line scans are shown in Figures 23 and 24. In both cases, the lighter colored line is the Cu line, the darker line which starts higher in the vertical direction is the Sn line, and the other line represents Pb.

The intermetallic compound thicknesses and phase compositions are shown in Table 4 for samples after high temperature (170°C) aging.

Figure 23 EDX Line Scan After 100 Hours @ 170°C

Table 4. Intermetallic Compound Thicknesses and Phase Percentages

Time Point (Hrs.)	Aging Time (Hrs.) ^{0.5}	Min. (μm)	Avg. (μm)	Max. (μm)	% ϵ -phase	% η -phase
T_0		1.1	2.1	4.2		
After Chip Attach		1.7	3.5	6.1	34	66
100 Hrs.	10	4.2	7.5	11.7	44	56
200 Hrs.	14.14	6.7	8.3	10.8	40	60
500 Hrs.	22.36	9.1	11.7	14.2	38	62
1000 Hrs.	31.62	12.5	15	18.3	40	60

Figure 24 EDX Line Scan After 1000 Hours @ 170°C

Both EDX line scans show changes in the concentrations of Cu, Sn, and Pb present in the four distinct layers present. The inner copper core is entirely copper. The layer next to the copper core, Cu_3Sn (ϵ -phase), contains both copper and tin. The intensity levels (vertical height) of the copper and tin are approximately the same on the scan. The intensity levels of an EDX scan are based on the atomic percentages of the elements detected. Copper has an atomic weight of 63.55 gm/mole, tin has an atomic weight of 118.69 gm/mole. For equivalent intensity levels, the atomic concentration of copper will be 1.87

times that of tin. The layer next to the bulk solder contains the Sn rich Cu_5Sn_6 (η -phase). The other layer is the bulk solder containing lead and tin.

The discrepancy between the expected and measured intensity levels for the EDX line scans can be attributed to not having Cu and Sn calibration standards. The percentage of the ϵ -phase and η -phase was consistent throughout all of the high temperature aging samples.

Electrical resistance measurements of the samples were taken after 0, 168, and 500 hours of thermal aging at 170°C . There were 480 flip chip joints per chip or 120 joints per side. Table 5 shows the number of sides of the units that passed the electrical resistance test requirement versus the number of sides tested. The actual average resistance values of all the unit's sides are shown in Table 6.

Table 5. Electrical Yield after Thermal Aging

Reliability Test	0 Hours	168 Hours	500 Hours
High Temp. Storage (170°C)	29/32	29/29	21/29

Table 6. Electrical Resistance After High Temperature Storage (120 Joints)

Resistance	0 Hours	168 Hours	500 Hours
Min. (ohms)	46.32	44.68	44.43
Max. (ohms)	48.94	48.04	117.32
Avg. (ohms)	46.92	45.50	71.69

The results in Tables 5 and 6 show failures start to occur after 500 hours of thermal aging at 170°C. The samples which electrically failed were cross sectioned, but the exact failure mechanisms were not determined.

5.2 Thermal Cycling

Electrical resistance measurements of the samples were taken after 0, 100, 200, 500, and 750 temperature cycles at various conditions. The numbers shown in Table 7 are number of good units versus the total number of units tested. Each side of the units was tested and is reported individually. There were 480 flip chip joints per chip or 120 joints per side. The actual average resistance values of all the unit's sides are shown in Table 8.

Table 7. Electrical Yield after Thermal Cycling

Temperature Cycling	0 Cycles	100 Cycles	200 Cycles	500 Cycles	750 cycles
Condition A (0 to 100°C) with Underfill	18/20	18/18	18/18	18/18	18/18
Condition B (-55 to 125°C) with Underfill	35/36	35/35	35/35	31/31	31/31
Condition A (0 to 100°C) without Underfill	14/16	14/14	13/14	0/14	
Condition B (-55 to 125°C) without Underfill	27/28	0/27			

Table 8. Electrical Resistance After Thermal Cycling

Group		0 Cycles	100 Cycles	200 Cycles	500 Cycles	750 cycles
Condition A (0 to 100°C) with Underfill	Min.	46.22	45.28	45.22	45.02	44.40
	Max.	52.62	50.48	50.47	51.87	52.11
	Avg.	48.09	47.05	46.97	46.14	46.02
Condition B (-55 to 125°C) with Underfill	Min.	45.38	44.22	43.97	44.03	43.90
	Max.	55.77	50.38	110.10	49.45	49.34
	Avg.	48.36	46.90	54.20	46.25	46.17
Condition A (0 to 100°C) without Underfill	Min.	45.83	45.78	45.89	All Opens	
	Max.	49.54	49.67	49.73		
	Avg.	47.13	47.18	47.81		
Condition B (-55 to 125°C) without Underfill	Min.	45.87	All Opens			
	Max.	47.51				
	Avg.	46.67				

The results from Tables 7 and 8 show three distinct trends. Units which were underfilled had a dramatically improved resistance to thermal cycling fatigue, regardless of the temperature cycling conditions. Units which were temperature cycled to the more extreme condition without underfill failed earlier. The other trend was the stability of the electrical resistance of the interconnection until failure. This indicates that resistance measurements should be monitored during the temperature cycling in order to determine the exact failure time.

Scanning electron micrographs of a good flip chip joint are shown in Figures 25 and 26. A layer of intermetallic compounds is visible at the bump to package interface. A scanning electron micrograph of an epoxy underfilled package is shown in Figure 27. The filler dispersed in the epoxy is used to

increase the thermal conductivity and lower the coefficient of expansion of the epoxy.

Figure 25. Micrograph of "Good" Flip Chip Joint Before Underfilling

Figure 26 Micrograph of "Good" Flip Chip Joint Showing Cu-Sn Intermetallic Compounds

Figure 27. Micrograph of Flip Chip Joint After Epoxy Underfill

Chapter 6

Discussion

The thermo-mechanical reliability of copper core bumps proved to be capable of withstanding 750 temperature cycles from -55°C to 125°C if underfilled. No major increase in electrical resistance was observed through 750 temperature cycles for samples with an epoxy underfill. Samples without underfill failed after only 100 cycles of condition B, and 500 cycles of condition A temperature cycling. The improved thermo-mechanical performance of the interconnects with the less severe temperature cycling is consistent with previously published work. This failure rate is comparable to other non-underfilled flip chip type packages with large die. The presence of an underfill is the key to assuring a reliable flip chip type package assembly, regardless of the interconnect material.

The growth rate of the Cu-Sn intermetallics was consistent with the work published by Fleischner^[25] and Mei.^[10] The intermetallic compound growth rate was linear at constant temperature, with respect to the square root of time. A plot of the average total Cu-Sn intermetallic compound thickness versus time is shown in Figure 28. The average percentage of the ϵ - and η -phase for aging at 170°C was approximately 39/61 (64%) which was slightly higher than the 53% previously modeled by Sunwoo.^[9]

Figure 28. Average Intermetallic Compound Thickness vs. Thermal Aging Time at 170°C

This 10 percent discrepancy can be attributed to variations in the oven temperature, cross sectioning techniques, and intermetallic compound thickness measurements.

Changes in the electrical resistance of the samples stored in thermal aging occurred earlier than expected. After 500 hours at 170 °C, failures (opens) and high resistance readings began to occur. Due to difficulties in isolating the exact location of the “open” within the series, no failure analysis could be successfully completed on these parts. It is expected that the connection of the copper core bump to the copper land of the substrate was initially marginal (see Figure 20), and additional thermal aging caused premature failures.

Chapter 7

Conclusions

The growth rate of Cu-Sn intermetallic compounds was found to be linear with respect to the square root of time. The ratio of the ε -phase to η -phase was constant throughout the thermal aging process, at constant temperature. Cu-Sn intermetallic compounds will be present at any copper and tin based solder joint. The formation rate and composition of the intermetallic compounds are determined by the temperature history of the joint. For flip-chip type interconnections, the use of epoxy underfills significantly extends the thermo-mechanical life of the solder joints by evenly distributing the stresses caused by the thermal expansion mismatches of the materials used within the package. The addition of a copper core within the solder joint did not significantly improve the thermo-mechanical property of the solder flip chip interconnection. Future studies should investigate alternative solder systems and material properties of epoxy underfills for extending flip chip type interconnection reliability. A recommended future study would include flip chip type interconnects to laminate-based substrates. The increased mismatch in the coefficients of thermal expansion of the package materials will place more demands on the thermal-mechanical performance of the flip chip interconnect. As the microelectronic industry continues to increase interconnect densities for cost effective solutions, flip chip type interconnections will play a more vital and important role in microelectronics.

References

- ¹ Singer, P.H., "Hybrid Wire Bonding Advances." *Semiconductor International*, 7(7): p. 66, July 1984
- ² Steidel, C.A., "Assembly Techniques and Packaging," in VLSI Technology, ed by S.M. Sze, p. 551, McGraw-Hill, New York, 1982.
- ³ Koopman, Nicholas G. "Chip to Package Interconnections," in Microelectronics Packaging Handbook, ed by R.R. Tummala, p. 411, Van Nostrand Reinhold, New York, 1989.
- ⁴ Miller, L.F., "Controlled Collapse Reflow Chip Joining," *IBM J. Res. Develop.*, 13: pp. 239-250, May 1969.
- ⁵ Rent never published. See B.J. Landman and R.L. Russo. "Pin vs. Block Relationship for Partitions of Logic Graphs," *IEEE Transactions*, C20(12): pp.1469-1479, December 1971.
- ⁶ Rymaszewski, Eugene J., "Microelectronics Packaging - An Overview," in Microelectronics Packaging Handbook, ed by R.R. Tummala, p. 14, Van Nostrand Reinhold, New York, 1989.
- ⁷ Brownell, D.L., and G.C. Waite. "Solder Bump Flip-Chip Fabrication Using Standard Chip and Wire Integrated Circuit Layout," 1974 ISHM Conf. Proc., p. 77, September 1974.
- ⁸ Manko, H.H., "Solder-Bond Formation," in Solders and Soldering, pp. 1-19, McGraw-Hill, New York, 1992.
- ⁹ Massalski, T.B., ed., Binary Alloy Phase Diagrams, American Society of Metals, Metals Park, Ohio, 1986
- ¹⁰ Sunwoo, A.J., J. W. Morris, and G. K. Lucey, "The Growth of Cu-Sn Intermetallics at a Pretinned Copper - Solder Interface," Metallurgical Transactions, Volume 23A, April 1992
- ¹¹ Mei, Z., A.J. Sunwoo, and J.W. Morris, "Analysis of Low-Temperature Intermetallic Growth in Copper-Tin Diffusion Couples," Metallurgical Transactions, Volume 23A, March 1992

¹² Cogan, S.F., S. Kwon, J.D. Klein, and R.M. Rose, "Diffusion in the CuSn Binary System: Application to Nb₃Sn Composites", Journal of Material Science **19**, 497, 1984

¹³ Felton, Lawrence E., "Copper-Tin Intermetallics in Solder Joints", Doctoral Thesis, Rensselaer Polytechnic Institute, April, 1991

¹⁴ Tu, K. N., "Interdiffusion and Reaction in Bimetallic Cu-Sn Thin Films", Acta Metallurgica **21**, 347, 1973

¹⁵ Davis, P.E., M.E. Warwick, and P.J. Kay, Plating Surface Finishing, 1982, vol. 69, p. 72-76

¹⁶ Tu, K.N., and R.D. Thompson, Acta Metallurgica **30**, p. 947-952, 1981

¹⁷ Quan, L., D. Frear, D. Grivas, and J. W. Morris, "Tensile Behavior of Pb-Sn Solder/Cu Joints", Journal of Electronic Materials **16**, 204, 1987

¹⁸ Parent, J.O.G., D.D.L. Chung, and I.M. Bernstein, "Effects of Intermetallic Formation at the Interface Between Copper and Pb-Sn Solder", Journal of Material Science **23**, 2564, 1988

¹⁹ Frear, D., D. Grivas, and J.W. Morris, "A Microstructure Study of the Thermal Fatigue Failures of 60Sn-40Pb Solder Joints", Journal of Electronic Materials **17**, 171, 1988.

²⁰ Aggarwal I., and G. Selvaduray , "Intermetallic Compound Formation in Flip-Chip Bonding," Proceedings 8th Electronic Materials and Processing Congress, San Jose, 1993

²¹ Koopman, Nicholas G., "Chip To Package Interconnections," in Microelectronics Packaging Handbook, ed by R.R. Tummala, p. 388, Van Nostrand Reinhold, New York, 1989.

²² Chikawa, Y., K. Mori, S. Sasaki, T. Maeda, and M. Hayakawa. "Bumping Technology for Tape-Automated Bonding," Proceedings 1st IEEE CHMT Symposium, 1984, p. 227-232.

²³ Leyden, Donald E., "X-Ray Spectrometry," in ASM Handbook Vol. 10, Materials Characterization, p.82-101, ASM International, Ohio, 1986

²⁴ Verhoeven, John D., "Scanning Electron Microscopy," in ASM Handbook Vol. 10, Materials Characterization, p.491-515, ASM International, Ohio, 1986

²⁵ Fleischner, Robert Alfred, "Solderability Preservation Through Low-Temperature Storage", Masters Thesis, California State University, Long Beach, December 1987