1997

Development of a new 12 volt bipolar analog process

Steven R. White
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Development of a New 12 Volt Bipolar Analog Process

A Thesis

Presented to

The Faculty of the Department of Materials Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Steven R. White

December 1997

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ABSTRACT

DEVELOPMENT OF A NEW 12 VOLT BIPOLAR ANALOG PROCESS

By Steven R. White

Computer simulations of the doping and diffusion processing were employed in the development and characterization of a new bipolar analog fabrication process. The new process takes advantage of an up-down isolation scheme which allows circuit size reduction and fabrication of a floating vertical PNP transistor. The simulations were first verified against historical processing data. Simulated experiments were done to determine processing times, temperatures, diffusion depths, and layer thicknesses. From these results, wafer experiments were designed and processed.

The results show that successful fabrication of 12 volt integrated circuits using the up-down isolation scheme is possible. The fabrication of the floating vertical PNP transistor is also possible. The epitaxial layer thickness was shown to be the most important factor. The goal of fabricating a PNP transistor able to sustain 12 volts was not achieved. However, identification of the need for a thicker epitaxial layer was accomplished. The results of these experiments show that the ultimate goal of circuit size reduction to enable lower manufacturing costs is possible using the processing methods developed.

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Chapter 1. Introduction

1.1 Economic motivation

It is estimated that in 1997 the world-wide semiconductor industry will manufacture over \$159 billion dollars worth of integrated circuits⁽¹⁾. These circuits are used for a myriad of applications ranging from computers of all types to the simplest household appliance. They are found in sophisticated medical equipment and the latest military hardware. Toys, televisions, automobiles, industrial equipment; almost everything in modern society contains silicon integrated circuits. The functions that these circuits perform vary from extremely complex, user programmable functions to simple logic and analog functions. For example, the latest application of integrated circuits being introduced in the United States is the smart card. These cards are disposable repositories for cash, each containing an integrated circuit which electronically stores and disburses “money” for the holder. The widespread use of integrated circuits will expand tremendously in the foreseeable future as technology progresses and new applications for semiconductor integrated circuits are introduced.

Not all of the circuits manufactured are sub-half micron microprocessor or memory circuits. Many are simple circuits that have a wide range of applications and have become the building blocks for circuit and system design. Most of these types of circuits were designed 10, 20, even 30 years ago and are still in demand for many applications. These types of circuits are manufactured by most major semiconductor manufacturers and are considered commodities in the market place. Thus, the average selling price (ASP) of

each producer determines what percentage of the market he will control. A difference of a few pennies in price for each chip can make the difference between high market share and profitability and low market share and loss of profitability. For example, there are many producers such as Philips, National, and Motorola in competition with each other. They all have many inexpensive commodity circuits on the market. These circuits have profit margins of a few pennies per circuit. However, with production and sales volumes for each circuit in the many millions per year, no manufacturer can afford to be undersold by his competition. A small difference in ASP can drastically affect the percentage of market share controlled by a producer. Loss of even a small percentage of market share can mean the loss of hundreds of thousands of dollars of profit. Therefore, it is imperative that each producer continually cut his costs and improve his manufacturing capability to remain competitive.

One manner to cut the manufacturing cost is to shrink the size of the circuit and, therefore, manufacture more on each silicon wafer. In order to accomplish this, wafer fabrication processes must be changed and improved to allow the shrink in circuit size. This is especially true if the circuit design is old, and newer fabrication technology can be employed. The development and characterization of these new fabrication processes was the focus of this thesis. The emphasis was on the doping processes, impurity diffusion and impurity ion implantation.

1.2 Project Objective

The goal of this thesis was to develop and characterize a new 12 volt bipolar

analog process. It is intended to replace the existing 12 volt process that is currently in production at Philips Semiconductors in Sunnyvale, California. The new process was developed using an up-down isolation scheme and an implanted antimony N+ buried layer. Modifications to the epitaxial layer thickness were also investigated. The advantages of the new process are shallower junctions, with less lateral diffusion, and better parametric stability from lot to lot. A significant shrink in the design rule requirements which will potentially lead to a die size reduction can be made due to the reduced lateral diffusion. Using the up-down isolation process, we are also able to fabricate a floating vertical PNP transistor. The floating vertical PNP transistor is capable of handling higher current density than existing lateral PNP transistors. It also has a more stable gain as a function of current compared to lateral PNP transistors. The higher current carrying capability and gain stability of the vertical PNP transistor gives more design flexibility for circuit size shrinks and it is beneficial for potential new 12 volt product designs.

1.3 Background

The 12 volt process is one of approximately ten bipolar analog processes currently run at Philips Semiconductors in Sunnyvale, California. It is a simple junction isolated bipolar process developed over 20 years ago. The products fabricated on this process are designed such that the maximum voltage encountered during normal operation is 12 volts. Other processes running at Philips are designed for maximum operating voltages of 20, 25, and 40 volts. Because the design rules on this process are so old, the components and spacing between them are large and the alignment tolerances are loose. This is true of all

the older analog product lines at Philips Semiconductors.

Characterization work similar to that done on the 12 volt process has also been completed for higher voltage products which run on processes similar to the 12 volt process. This characterization work has been initiated at the request of the product marketing group in order to shrink the die, reduce the cost per die, and enable Philips to reduce the price. This will increase market share for several commodity parts. As an example of the potential benefit, the gross die per wafer of one product, running on a newly developed 40 volt process, has been increased from approximately 900 die per wafer to approximately 1900 die per wafer.

Also, there are new designs in development that will use the floating vertical PNP transistor available on the new 40 volt process. The 12 volt process benefits similarly with the addition of the floating vertical PNP transistor.

In addition to the benefits of a new 12 volt analog process, we also will gain significant knowledge and experience that will be transferable to other bipolar analog processes.

1.4 Die Size Reduction

There are several methods readily available which allow us to shrink the size of the circuit. They include reduction of the alignment tolerances, implementation of an oxide/nitride capacitor process, and implementation of an up-down isolation process. Any one of them, taken alone, cannot provide enough benefit to make its implementation economically feasible. However, implementation of all or most of them together could

provide the incentive to retool old designs and attract new designs. These methods are described below.

1.4.1 Photolithography and Alignment Tolerances

When these processes were developed, contact photolithography was the means by which the components of the circuits were patterned on the wafers. At that time, the alignment of one layer to the next had an allowed tolerance of 2.0 μm . Obviously, the photolithography process has improved tremendously over the last 20 years. Scanning projection photolithography, which is available at Philips Semiconductors, while not state of the art by today's standards, is a considerable step above contact lithography. Using projection lithography the alignment tolerances have been tightened from 2.0 μm to 1.0 μm on new designs and retooling of old designs. The improvement in alignment tolerance alone would allow a shrink in the design rules. However, the cost of retooling and redesigning the mask sets based on improved alignment tolerances alone cannot be justified.

1.4.2 Capacitor Fabrication

Another means to shrink the die is to reduce the size of the capacitors on those circuits having them. All of the bipolar analog processes at Philips have an optional capacitor. The capacitor employs N⁺ doped silicon as one plate, thermal silicon dioxide as the dielectric, and aluminum as the other plate. Typically, these capacitors take up between 25% and 50% of the total chip area. Recently, a silicon nitride/silicon dioxide sandwich dielectric has been successfully developed and implemented on the new 40 volt

process. This new dielectric has doubled the capacitance per unit area, allowing a 50% reduction in capacitor area. Where feasible, it has greatly reduced the size of each die and increased the number of die per wafer. The cost, however, is a much more complicated processing sequence. An oxide layer, albeit thinner, is still required. An LPCVD silicon nitride deposition has been added to complete the sandwich dielectric layer. After the silicon nitride deposition, an additional masking and etch step is required to pattern the nitride over the capacitor area. Because of the added cost of these steps, significant reduction in the die size must be realized in order to justify a redesign to include the nitride/oxide capacitor. Again, the cost of the redesign, as well as the cost of the added processing steps, precludes a retooling on many products.

1.4.3 Up-Down isolation

The component regions on the existing 12 volt process are isolated by diffusing boron from the surface of the N-type epitaxial layer through to the P-type substrate below it. The up-down isolation process employs an additional boron diffusion beneath the epitaxial layer. This boron layer diffuses up through the epitaxy and meets the boron which is diffusing down. Thus, the diffusion time and junction depth for isolation can be greatly reduced. By reducing the junction depth of the boron isolation and, hence, the amount of lateral diffusion, closer spacing between circuit components is possible. This reduces the area required for the circuit layout. Up-down isolation also provides the benefit of the floating vertical PNP transistor. Availability of this transistor is extremely attractive. It allows the designers to use it, rather than the lateral PNP transistor which

needs significant area for large current carrying capability. Also, as mentioned, the gain of this transistor is more stable. The up-down isolation will be discussed in the following sections, as it was the major area of work in this thesis.

1.5 Existing 12 volt Process Description

The following section describes the existing 12 volt process at Philips. The flowchart available in Figure 1 provides diagrams showing the fabrication of the NPN transistors. All processes run at Philips use oxidized P-type, $\langle 111 \rangle$ silicon wafers as the starting material.

1.5.1 N+ Buried Layer

Following the initial masking and etch operations, the N+ buried layer diffusion is done. It employs arsenic doped spin-on glass as the dopant source. The glass is spun on and baked. The silicon is doped during a short furnace cycle at 1180 °C. After doping the silicon, the glass is dipped off in 1:10 HF and the arsenic is diffused to the proper depth at 1250 °C. The sheet resistance of the buried layer is approximately 7 $\Omega/\square$. The junction depth is approximately 7.0 μm .

1.5.2 Epitaxial Layer Growth

The oxide is removed and the N type epitaxial layer is grown. This step grows a single crystal layer of silicon on the surface of the substrate by the chemical decomposition of dichlorsilane (SiCl_2H_2). The dopant used in the epitaxial process is arsenic. The

1) Arsenic is diffused into the P type silicon substrate to form the N+ doped buried layer.

2) A N- doped single crystal epitaxial layer is grown on the surface of the silicon. The dopant is arsenic.

3) Boron is diffused into the epitaxial layer to electrically isolate the regions where the transistors and other components are fabricated.

4) Phosphorus is diffused in to the epitaxial layer to form an N+ contact to the buried layer. Boron in the isolation regions diffuses further to complete the isolation. Collector plug is an optional step.

5) Boron is diffused into the epitaxial layer to form the base regions of the NPN transistors. Boron resistors are also fabricated from this diffusion.

6) Phosphorus is diffused to form the emitters of the NPN transistors. N+ contacts are also fabricated during this step to insure ohmic contact to the epitaxial layer.

Figure 1. Existing 12 Volt Philips Process Flowchart

epitaxial thickness and resistivity targets are 6.5 μm and 0.9 $\Omega\text{-cm}$ respectively. After the epitaxial layer is grown, the surface of the silicon is reoxidized.

1.5.3 Isolation Diffusion

The wafers are masked and the pattern for the isolation diffusion is etched into the oxide. A boron doped glass that is spun on is used as the boron source. Isolation diffusion is done at high temperature, 1220 $^{\circ}\text{C}$, and the boron is diffused approximately 9.0 μm to insure complete electrical isolation of the device regions. The time of the isolation diffusion varies depending upon whether an optional phosphorus collector plug is used. If a plug is used, the isolation is completed during the subsequent collector plug diffusion. The thermal oxide and spin on glass are stripped after isolation diffusion and the surface is reoxidized.

1.5.4 Lateral Diffusion of the Boron Isolation

The lateral diffusion can be estimated to be 80% of the vertical diffusion in the silicon. This means that each isolation line becomes 7.2 μm wider per side, or a total of 14.4 μm wider overall. Spacing of other diffused regions to the isolation must be sufficient so the device can sustain the required voltage during operation. The large amount of lateral diffusion makes the up-down isolation processing scheme attractive for reducing the circuit layout area while maintaining the design rule spacing requirements.

1.5.4.1 Junction breakdown

The breakdown of a reversed biased P/N junction which is remote from any other diffusion is dependent upon the resistivity of the N type and P type regions and the radius

of curvature of the junction. When the junction is reversed biased, the depletion region extends into both N and P type silicon until the critical field is reached and avalanche breakdown occurs. The critical field is determined by the amount of charge contained in the depletion region. Higher impurity doping increases the charge per unit volume and reduces the voltage which must be applied across the junction to induce avalanche breakdown. A smaller radius of curvature of the junction also lowers the voltage required to cause avalanche breakdown of the junction.

1.5.4.2 Punch-through breakdown

If the depletion region extends far enough to contact another junction, punch through breakdown will occur. For example, if the reversed biased base-epitaxy depletion region extends to and contacts the epitaxy-isolation junction, the base and isolation will be shorted through the depletion region. The breakdown is now controlled by the much higher doped isolation and occurs at a lower voltage. Preventing this mechanism from occurring requires maintenance of the proper spacing between the various diffusions.

1.5.4.3 Reduction of the Isolation Lateral Diffusion

As mentioned previously, the deep boron isolation diffusion required to electrically isolate the different components in the silicon results in large lateral diffusion of the boron. If the lateral diffusion is reduced, the design spacing between each diffusion can be reduced by a similar amount. The physical distance between the diffusions will be maintained. This is shown in Figure 2. Reduction of the lateral diffusion and hence the design spacing is one of the major goals of the process development.

Figure 2. Comparison of Isolation Lateral Diffusion

1.5.5 Base Diffusion

The base masking and etch steps are done next, followed by the NPN base process. It is done in three steps. First, the boron deposition, done at 935 °C, dopes the silicon, using solid source boron nitride wafers that are in proximity to the silicon wafers. The deposition is followed by a low temperature oxidation at 750 °C that aids in the removal of a boron rich surface phase. Finally, the base diffusion is done at 1050 °C which drives the boron to a depth of 1.2 μm. The target sheet resistance of the base layer is 200 Ω/□. The oxide thickness target after base diffusion is 4500 Å in the base regions.

1.5.6 Emitter Diffusion

Another masking and etch step is done to define the emitter and collector contact areas. The two step emitter process begins with the phosphorus deposition using PH₃ in O₂ as the phosphorus source. This is done at 930 °C. The deposition time is varied to target the NPN transistor gain. The phosphorus is then diffused to a depth of approximately 1.0 μm. The oxide thickness target after emitter diffusion is 3000 Å in the emitter and collector contact regions.

1.5.7 Other Processing Steps

The contact masking and etch step is next and it is followed by metallization, metal masking, passivation, and pad mask. Besides the optional collector plug step, several other options are available for the 12 volt process. These are implanted boron resistors, SiCr thin film resistors, oxide capacitors, and dual layer metallization. Figure 3 shows the structure of a completed NPN transistor.

Figure 3. 12 Volt NPN Transistor Cross Section

1.6 Description of the Process Changes

In this section a description of the changes to the 12 volt process are discussed. The flowchart in Figure 4 provides diagrams showing the fabrication of the NPN transistors. The flowchart in Figure 5 provides diagrams showing the fabrication of the floating vertical PNP transistor.

1.6.1 N+ Buried Layer

The first change was the use of an implanted antimony process for doping the N+ buried layer. The spin on arsenic N+ buried layer process presents several problems that

- 1) Antimony is implanted and diffused into the P type silicon substrate to form the N⁺ doped buried layer.

- 2) Boron is diffused into the P type substrate to form the bottom portion of the isolation structure. The collector of the vertical PNP transistor is also formed during this step.

- 3) A N- doped single crystal epitaxial layer is grown on the surface of the silicon. The dopant is arsenic.

- 4) Boron is diffused into the epitaxial layer to electrically isolate the regions where the transistors and other components are fabricated. The buried P boron diffuses up toward the top isolation diffusion.

- 5) Phosphorus is diffused into the epitaxial layer to form an N⁺ contact to the buried layer. Boron in the top and bottom isolation regions diffuses further to complete the isolation. Collector plug is an optional step.

- 6) Boron is diffused into the epitaxial layer to form the base regions of the NPN transistors. Boron resistors are also fabricated from this diffusion.

- 7) Phosphorus is diffused to form the emitters of the NPN transistors. N⁺ contacts are also fabricated during this step to insure ohmic contact to the epitaxial layer.

Figure 4. Fabrication of an NPN Transistor using the Up-Down Isolation.

- 1) Antimony is implanted and diffused into the P type silicon substrate to form the N⁺ doped buried layer.

- 2) Boron is diffused into the P type substrate to form the bottom portion of the isolation structure. The collector of the vertical PNP transistor is also formed during this step.

- 3) A N- doped single crystal epitaxial layer is grown on the surface of the silicon. The dopant is arsenic.

- 4) Boron is diffused into the epitaxial layer to electrically isolate the regions where the transistors and other components are fabricated. The buried P boron diffuses up toward the top isolation diffusion. Contact to the buried P type PNP collector is also made.

- 6) Boron is diffused into the epitaxial layer to form the emitter regions of the VNP transistors. Boron resistors are also made from this diffusion. Diffusion of the boron during collector plug step completes isolation.

Figure 5. Fabrication of the Floating Vertical PNP Transistor

can be addressed by using implanted antimony as the dopant. First, the existing process is a two step furnace operation that can be simplified to an implant and one furnace operation. The spin-on glass process is time consuming and difficult to maintain. Also, the supply of the solution may become scarce, since few manufacturers use it. Most important, however, is that the up diffusion into and auto doping of the epitaxial layer is much greater with arsenic than with antimony. By reducing the amount of up diffusion, it is possible to get higher NPN transistor collector to emitter breakdown voltages with a thinner epitaxial layer. A thinner epitaxial layer is also easier to isolate, and greater reduction in component spacing may be possible because the isolation side diffusion has been further reduced.

1.6.2 Up-Down Isolation

The second change was the up-down isolation process. As mentioned previously, the existing 12 volt process has a large amount of lateral diffusion during isolation diffusion. This requires that the circuit layout area be large enough to account for the side diffusion and still maintain the required spacing to maintain breakdown voltages. Using the up-down isolation processing scheme, the amount of lateral diffusion can be minimized. An additional masking and etch step is done after the N+ buried layer diffusion prior to epitaxial growth. This step defines the isolation pattern and boron is deposited or implanted and diffused directly into the P-type silicon substrate. During the epitaxial processing and the subsequent reoxidation of the wafer surface, the boron that is underneath the epitaxial layer diffuses up. Thus, the depth that the top isolation must

diffuse to insure complete isolation is less. Because the diffusion depth has been reduced, the lateral diffusion is also reduced. This makes it possible to reduce the area required for circuit layout. In addition to the advantages described above, this buried layer of P-type doping is used to fabricate the collectors of the floating vertical PNP transistors. These transistors employ the epitaxy as the base and the NPN base diffusion as the emitter. They are used in many of the products that are run on the higher voltage processes using this isolation scheme.

1.6.3 Epitaxial Growth

After the P+ buried layer processing, the epitaxial layer is grown in the usual fashion. Because of the reduced up diffusion and auto-doping from the antimony N+ buried layer, a thinner epitaxial layer can sustain the required voltages. Therefore, a thinner epitaxial layer was investigated.

1.6.4 Subsequent Processing

All of the subsequent processing steps described in the preceding section remained unchanged. The collector plug processing, when employed, remained unchanged except for the diffusion time. It was changed depending on the final epitaxial layer thickness. The isolation diffusion time, again, depended upon whether this optional step is used.

Figure 6 shows the cross section of a completed NPN transistor fabricated on the 12 volt up-down isolation process.

Figure 6. Up-Down Isolation Process Cross Section

Figure 7 shows the structure of a completed floating vertical PNP transistor fabricated using the new 12 volt process. The P-type collector is surrounded by N-type buried layer. As can be seen in Figure 7, the NPN base diffusion becomes the vertical PNP (VPNP) emitter. The P+ buried layer diffused over the N+ buried layer becomes the collector of the VPNP. It is surrounded by the N+ buried layer to keep it isolated from the P- substrate and at a floating potential during device operation. Hence the description of this transistor is the floating vertical PNP transistor.

Figure 7. Vertical PNP Transistor Cross Section

Contact to the P+ buried layer collector is made via the isolation diffusion. The advantage the floating vertical PNP transistors offer is they replace lateral PNP transistors which must be large to provide adequate current carrying capability.

1.7 Requirements

1.7.1 Parametrics

If the new process is to be successful, the electrical parameters must be comparable to those of the existing process. The parameters of primary concern are the junction breakdown voltages. They include the NPN collector to base breakdown voltage (BVcbo), the NPN collector to emitter breakdown voltage (BVceo), the isolation breakdown voltage (BViso), and the field threshold voltage (MOS V_t). They must be above 12 volts to insure that the circuit functions over the expected operating voltage range. Table 1 shows the average values of the various breakdown voltages for the existing 12 volt process. Also included are the BVcbo and BVceo requirements of the vertical PNP (VPNP) transistor.

Parameter	Average Value	Controlled by	Comment
BViso	70.0 volts	Epitaxial Layer Resistivity	High enough to allow some drop with new 12 volt process.
NPN BVcbo	46.0 volts	Epitaxial Layer Resistivity	High enough to allow some drop with new 12 volt process.
NPN BVceo	20.0 volts	Base to Buried N+ Spacing	Minimal drop allowable with new 12 volt process.
MOS V_t	15.0 volts	Epitaxial Layer Resistivity & Oxide Thickness	Should be maintained with epitaxial resistivity and oxide thickness.
VPNP BVcbo	N. A.	Epitaxial Layer Thickness and Resistivity	Must be above 12 volts.
VPNP BVceo	N. A.	Epitaxial Layer Thickness and Resistivity	Must be above 12 volts.

Table 1. Critical breakdown voltages for Existing 12 volt process.

The data above show that the BV_{iso} and NPN BV_{cbo} are high enough to eliminate concern over maintaining them at a safe level. A slightly lower average value would still be sufficient to maintain circuit function. The NPN BV_{ceo} is lower, 20 volts, and is controlled by the vertical spacing between the base and N+ buried layer. Any drop in the NPN BV_{ceo} must be very minimal. It can be maintained with sufficient thickness of the epitaxial layer. The MOS V_t is controlled primarily by the epitaxial layer resistivity and oxide thickness. At 15.0 volts, it is already close enough to the 12.0 volt process limit and must be maintained at the current level. Other important parameters such as the sheet resistances, resistor values, and transistor gains were targeted by adjusting doping concentration, junction depths, epitaxy thickness, critical dimensions, and processing time and temperature.

1.7.2 Processing and Equipment

All of the new processing steps developed, besides providing the proper electrical parametric results, remained simple. The primary goal of this project was to reduce the manufacturing cost of each circuit produced. Therefore, elaborate processing steps were unacceptable. Also, in keeping with the idea of cost reduction, all new processes were developed on existing equipment in the fabrication area. And finally, reductions of wafer handling, processing steps, and process complexity were of major benefit to the cost reduction effort.

1.8 Summary

The scope of this project was the development and characterization of the doping,

diffusion, and epitaxial growth steps for a new 12 volt bipolar analog process. The development of ion implantation for doping processes, the up-down isolation scheme, and the floating vertical PNP transistor, in conjunction with improvements in the photolithography processing and the oxide/nitride capacitor will hopefully provide the incentive to redesign and retool older product designs. In addition, it is hoped that they will provide the incentive to design new products using them.

Once the new process is complete and successful in achieving the goals of reduced die size and reduced manufacturing costs, the benefits could be large. Increased market share would mean more production volume. The introduction of new designs would do the same, as well as providing a secure outlook in the future. The knowledge gained from our experiences developing these processes for the 12 volt product line is directly transferable to the other analog production processes. This will enable us to make similar process improvements on them, allowing similar cost reductions, similar potential for increased market share, and more stability for Philips in Sunnyvale.

Table 2 summarizes and compares the existing 12 volt process and the proposed 12 volt process.

Existing Philips 12 Volt Process

Process Step	Dopant	Source	Deposition	Diffusion/ Oxidation
Buried N+	As	Spin on Arsenic Doped Glass	Furnace 1070 °C	Furnace 1250 °C
Buried P+	N/A	N/A	N/A	N/A
Epitaxial Layer	As	Arsine Gas (AsH ₃)	Reactor 1080 °C	Furnace 1140 °C
Isolation	B	Spin on B Glass	Furnace 1220 °C	Furnace 1050 °C
Collector Plug	P	Phosphine Gas (PH ₃)	Furnace 930 °C	Furnace 1150 °C
Base	B	Solid BN Wafers	Furnace 935 °C	Furnace 750 °C Furnace 1050 °C
Emitter	P	Phosphine Gas (PH ₃)	Furnace 930 °C	Furnace 850 °C

12 Volt Up-Down Isolation Process

Process Step	Dopant	Source	Deposition	Diffusion/ Oxidation
Buried N+	Sb	Ion Implantation	N/A	Furnace 1250 °C
Buried P+	B	Ion Implantation	N/A	Furnace 1150 °C
Epitaxial Layer	As	Arsine Gas (AsH ₃)	Reactor 1080 °C	Furnace 1140 °C
Isolation	B	Solid BN Wafers	Furnace 935 °C	Furnace 1050 °C
Collector Plug	P	Phosphine Gas (PH ₃)	Furnace 930 °C	Furnace 1150 °C
Base	B	Solid BN Wafers	Furnace 935 °C	Furnace 750 °C Furnace 1050 °C
Emitter	P	Phosphine Gas (PH ₃)	Furnace 930 °C	Furnace 850 °C

Table 2. Summary and Comparison of 12 volt processes.

Chapter 2. Technical Background and Literature Search

2.1 Introduction

As detailed in Chapter 1, the changes to the 12 volt process involve several doping steps, diffusion steps and the epitaxial growth step. These steps are done at high temperatures to diffuse the dopants to the required depth into the silicon. Not only does the dopant introduced at each particular step diffuse, but so do the dopants introduced during preceding steps. Thus, the final dopant concentration profiles depend not only on the processing conditions when they were introduced into the silicon, but also on all the subsequent processing steps.

The processing temperature is not the only factor influencing how fast and in what manner the dopants diffuse. It is also affected by the oxidations normally done during each cycle, impurities introduced in prior steps, the impurity being introduced at a particular step, and defects which are present in the crystal.

In addition, during processing, the dopants diffuse out of the silicon and into the gaseous ambient. This causes redistribution of dopants onto the surface of the silicon and is especially a concern during the epitaxial layer growth step. It affects many of the electrical parameters that we try to control during the processing.

The new 12 volt process relies upon ion implantation as a method of introducing dopants into the silicon. This process disrupts the crystalline structure of the silicon. Unless this damage is removed, the semiconducting properties of the silicon are lost and the devices will not function. Thermal processing following the implant can anneal this

damage and restore the undisrupted crystal structure. However, if not done properly, it can also leave a crystalline layer which contains high concentrations of defects. These defects can cause high leakage currents through the junctions and render the devices unusable. Also, because ion implantation is not a thermally driven process, the dopant concentration profiles will differ from those obtained from the existing thermal deposition processes.

An extensive literature search was completed and has provided better understanding of the factors mentioned above. They all were accounted for and understood before any major development work was undertaken. The high level of interest in successful fabrication of integrated circuits using silicon wafers offers one a large amount of literature to draw from. There are many textbooks available which discuss the basic processing of silicon wafers. They provided much information regarding diffusion and ion implantation processing steps. There is also an abundance of research and review articles available in technical periodicals. Useful information was found in articles dating from the late 1960s to the present. In the following sections the results of this search will be discussed. The main points will include basic diffusion and ion implantation theory. There are differing opinions regarding the mechanisms of diffusion in silicon. These are also discussed. Articles discussed were chosen because the information they provided was directly relevant to the process development effort. The information presented has been gleaned from various textbooks, review articles, research reports, and the references found therein.

2.2 Diffusion and Fick's Laws

2.2.1 Fick's first Law

Diffusion of impurities in silicon or any other material is described using Fick's first and second laws⁽²⁻⁷⁾. The first law states that the flux of impurity atoms is directly proportional to the concentration gradient of the impurity. Stated mathematically in one dimension, Fick's first law is shown in Equation 1.

$$J = -D \frac{\delta C(x, t)}{\delta x} \quad (1)$$

Where: J - Impurity Flux (atoms / cm² sec)

D - Diffusivity (cm² / sec)

C - Concentration (atoms / cm³)

x - distance (cm)

t - time (sec)

2.2.2 Fick's second Law

Fick's second law describes the diffusion of impurities when the concentration gradient inside of a finite volume of material changes with time. Stated mathematically, again in one dimension, Fick's second law is shown in Equation 2.

$$\frac{\delta C(x, t)}{\delta t} = \frac{\delta}{\delta x} \left[D \frac{\delta C(x, t)}{\delta x} \right] \quad (2)$$

Solving Equation 2, with the proper boundary conditions, results in expressions used to determine the diffused impurity concentration as a function of time and depth. Classically there are two solutions to this equation which are most relevant to diffusion in

semiconductor processing. These two solutions arise from different boundary conditions which closely describe typical conditions under which diffusion takes place during silicon wafer processing. Both assume that the diffusion coefficient is not a function of concentration.

2.2.3 Boundary Condition: Constant Surface Impurity Concentration

In the first case, the boundary condition is that of constant surface concentration. Dopant deposition steps are processes which best fit the assumption of constant surface concentration. The supply of the diffusing dopant is continuously available while processing to maintain its concentration in the silicon surface. It is usually supplied by flowing a gaseous compound of the dopant and oxygen in the process ambient. A thin oxide with a high concentration of the dopant grows on the silicon surface. This doped oxide continually supplies the surface to maintain constant concentration. The solving of Equation 2 with the boundary condition of constant surface concentration gives the following result, Equation 3.

$$C(x, t) = C_s \operatorname{erfc} \left[\frac{x}{2(Dt)^{1/2}} \right] \quad (3)$$

Where: C_s - Surface Concentration (atoms / cm³)

The term “erfc” is the complementary error function and is tabulated for different values of $\left[\frac{x}{2(Dt)^{1/2}} \right]$ in most books which discuss diffusion processes.

2.2.4 Boundary Condition: Constant Impurity Quantity

In the second case the boundary condition is that of constant impurity quantity. The solution of Equation 2 for this case describes the diffusion of impurity already contained within the silicon with no supply of additional impurity. Dopant drive-in steps are best described by this assumption. During these steps, the dopant introduced during the deposition or ion implantation step is redistributed. Further addition of dopant does not occur because the processing ambient contains none. Also, any doped oxide layers have been removed. Solving Equation 2 with the boundary condition of constant impurity quantity results in the following, Equation 4.

$$C(x, t) = \frac{Q_0}{(\pi Dt)^{1/2}} \exp\left[\frac{-x^2}{4Dt}\right] \quad (4)$$

Where: Q_0 - Total dopant quantity (atoms / cm²)

This equation has the form of a Gaussian distribution.

2.2.5 Temperature Dependence of Diffusivity

In both Equation 3 and Equation 4 the diffusion coefficient, D , is assumed to be a function of temperature only. Empirical measurements at low impurity concentrations have shown that the diffusion coefficient can be expressed as a function of temperature by Equation 5. This type of equation is known as an Arrhenius relationship.

$$D(T) = D_0 \exp\left[\frac{-E_a}{kT}\right] \quad (5)$$

Where: D_0 - Frequency factor (cm^2 / sec)

E_a - Activation energy (eV)

k - Boltzmann constant (eV/ $^{\circ}\text{K}$)

T - Temperature ($^{\circ}\text{K}$)

This equation is typical of thermally controlled processes. The pre-exponential constant term, D_0 , called the frequency factor, is related to the frequency of lattice atom vibrations. The activation energy, E_a , is the energy barrier that an atom must overcome to move within the crystal lattice. Both D_0 and E_a can be determined from a linear Arrhenius plot of $\ln(D)$ versus $1/T$.

2.2.6 Concentration Dependence of Diffusivity

The simple solutions to Fick's second law described above are idealized cases. They are capable of adequately describing diffusion phenomenon only when the impurity concentration is low. When the concentration of impurity rises, the diffusion coefficient, D , becomes a function not only of temperature, but of impurity concentration as well. When this is the case, it is often impossible to obtain a solution to the differential equations describing the change in concentration as a function of depth and time. Methods are available, such as Boltzmann-Matano analysis, which can determine the diffusion coefficient, $D(C)$, as a function of concentration from experimentally determined data of concentration versus depth. This method has been successful, but entails considerable experimental work to extract $D(C)$.

In the pursuit of reliable computer models of impurity diffusion in silicon, many researchers have studied the interaction of point defects, silicon lattice vacancies and silicon self interstitials, with substitutional impurity diffusion in silicon^(5 - 15). It is generally agreed that the diffusion of substitutional impurities in silicon is controlled by interaction with these point defects. There is considerable disagreement among these researchers regarding which of these point defects plays the dominant role in controlling diffusion. However, their work has been successful in developing theories which account for the dependence of the diffusion coefficient on impurity concentration. The general equation for the diffusion coefficient as a function of concentration is given below.

$$D = D^x + \sum_{j=1}^r (D^{-r}) \left(\frac{n}{n_i} \right)^r + \sum_{j=1}^r (D^{+r}) \left(\frac{n_i}{n} \right)^r \quad (6)$$

Where: D^x - Impurity diffusivity due to neutral point defect interaction (cm^2 / sec)

D^{-r} - Impurity diffusivity due to negative point defect interaction (cm^2 / sec)

D^{+r} - Impurity diffusivity due to positive point defect interaction (cm^2 / sec)

r - Charge state of point defect

n - Electron concentration (e^- / cm^3)

n_i - Intrinsic electron concentration (e^- / cm^3)

Each of the diffusivities given in Equation 6, D^x , D^{-r} , and D^{+r} , has a temperature dependence which is given by the Arrhenius model described by Equation 5.

Equation 6 relates the observed diffusion coefficient to the concentration of vacancy and interstitial point defects in various charge states. These charge states have

values of 0, ± 1 , and ± 2 . Higher charge states have never been observed for vacancies or interstitials in silicon. The impurity concentration dependency is accounted for in the ratio of the free electron concentration, n , to the intrinsic free electron concentration at the temperature of interest, n_i . The impurities in the silicon lattice are assumed to be completely ionized at high temperature. Thus, the free electron concentration is approximately equal to the net concentration of donor impurities. The role of point defects on impurity diffusion in silicon will be discussed further in forthcoming sections.

Stated earlier was the assumption that, at the high temperatures employed in diffusion processing, all of the impurity atoms are ionized. The concentration gradient of ionized impurities sets up an electric field within the silicon crystal where impurity diffusion is taking place. This electric field has the effect of enhancing the ionized impurity diffusion. The electric field enhancement factor is given by the following Equation 7.

$$h = 1 + \frac{N_D}{2n_i} \left(\frac{1}{\left[\left(\frac{N_D}{2n_i} \right)^2 + 1 \right]^{1.2}} \right) \quad (7)$$

Where: N_D (or N_A) - Donor (Acceptor) concentration (atoms / cm³)

n_i - Intrinsic electron concentration (e⁻ / cm³)

The electric field enhancement of the diffusion coefficient is incorporated into

Equation 6 by multiplying the previous result by h . The equation for the concentration dependent diffusion coefficient is now given by Equation 8 below.

$$D = h \left(D^* + \sum_{j=1}^r (D^{-r}) \left(\frac{n}{n_i} \right)^r + \sum_{j=1}^r (D^{-r}) \left(\frac{n_i}{n} \right)^r \right) \quad (8)$$

When the impurity concentration is high (i.e. $N_D \gg 2n_i$ or $N_A \gg 2n_i$) h takes its maximum value of two. Thus, at most, doubling of the diffusion coefficient is possible due to the electric field from ionized impurities.

2.3 Ion Implantation

Ion implantation processes were also developed for introduction of substitutional impurities into the silicon^{(2-4), (8), (9)}. Ion implantation is a totally different means from that of diffusion and thermal processing to dope the silicon crystal with impurities. The profiles of the implanted impurities are much different than those obtained by diffusion. In addition, the bombardment of the silicon by energetic ions damages the crystal structure. An understanding of how this damage manifests itself and what means are available to minimize it was essential for the success of this thesis. Subsequent redistribution of the impurities by high temperature diffusion processes is identical to the dopant drive in processes discussed in the previous sections.

2.3.1 Projected Range and Ion Scatter

An implanted ion enters the silicon surface with an energy that can be very precisely controlled by the acceleration energy set on the ion implanter. As it travels through the crystal it loses its energy through collisions with the silicon atoms and by

coulombic interactions between the charged ions and electrons in the silicon atoms. The total number of collisions and interactions each ion undergoes before coming to rest in the silicon, and the energy lost per collision, are totally random quantities. Thus, the depth that any ion will penetrate is also random. The average depth of the implanted ions can therefore be approximated using a statistical approach and follows, to first order, a Gaussian distribution. The Gaussian model for the implantation of ions into silicon is the simplest model available and is shown in Equation 9. It assumes that the depth of the implanted ions in the silicon is controlled by an entirely random process.

$$C(x) = \frac{D}{(2\pi)^{1/2}} \exp \left[\frac{-(x - R_p)}{2\Delta R_p} \right] \quad (9)$$

where: D = impurity dose in atoms/cm²

R_p = projected range

ΔR_p = longitudinal range straggle

The parameters employed to quantify the depth and distribution of implanted ions are the projected range, R_p , analogous to the Gaussian distribution mean, and the ion straggle, ΔR_p , analogous to the Gaussian distribution standard deviation. These parameters have been extensively studied for the major impurities used in ion implantation processing. They are plotted as a function of implant energy in most books which discuss ion implantation.

2.3.2 Ion Channeling

Due to ion channeling along crystalline directions, the actual dopant distribution in

the silicon is not perfectly symmetrical. Several models are available which can account for the non-symmetrical dopant distribution. The Pearson model is one of these. Ion channeling manifests itself as an extended tail at the bottom of the distribution. Consideration of this asymmetric tail region is of primary concern with shallow dopant profiles where it can significantly affect the properties of the devices being fabricated.

2.3.3 Radiation Damage and Annealing

Also key to the success of the development effort was the removal of the radiation damage caused by the implanted ions. The proper thermal annealing techniques required to restore the crystal structure of the doped silicon must be defined for each step. Research carried out by K. S. Jones, S. Prussin, and E. R. Weber with the University of California at Berkeley addresses this issue⁽¹⁰⁾. Their research examined many wafers implanted with different impurities using various doses and energies. Their intent in conducting this study was to categorize the various defect types they encountered and determine the implantation and subsequent annealing conditions which minimizes the defect density. They have classified the defects into five different categories depending upon where in the silicon they occur and how they were formed. These categories are summarized in Table 3.

Their results show that in order to minimize the defect density after processing it is desirable during the implant to form an amorphous layer on the silicon surface. Subsequent annealing at temperatures of 500 °C to 600 °C will restore the crystalline structure by solid phase epitaxial growth. Formation of an amorphous layer is made more

favorable with lower implant energies, heavier ions, and maintaining the wafer near room temperature during the implantation process. Lowered energies were recommended with light doses in order to contain the damage to a thinner layer of the silicon. This increased

Category	Description
1	Defects resulting after annealing if an amorphous layer is not formed during ion implantation.
2	Defects resulting after annealing in regions below an amorphous layer formed during the ion implantation.
3	Defects resulting after solid phase epitaxial regrowth of the amorphous layer formed during ion implantation.
4	Defects resulting after solid phase epitaxial regrowth of buried amorphous layers. The defects result when two single crystal interfaces meet.
5	Defects resulting when the implanted dopant exceeds its solid solubility at annealing temperature.

Table 3. Defect categorization by Jones, *et al.* ⁽¹⁰⁾

the likelihood of the formation of an amorphous surface layer. Boron implantation can be done with BF_2^- which forms the amorphous layer more readily than the lighter B^{11} ion. Maintaining the wafers at room temperature during processing was accomplished by flowing Freon through the endstation of the implanter. This prevented annealing of the silicon by the ion beam, a phenomenon called ion beam induced epitaxial crystallization (IBIEC), and promoted the formation of the amorphous layer.

2.4 Oxidation of Silicon

Oxidation of silicon will occur whenever the process ambient contains oxygen or water vapor. The linear-parabolic theory developed by Deal and Grove⁽¹¹⁾ model the oxidation of silicon very accurately in most cases. According to this theory, the rate of

oxide growth is directly proportional to the flux of the oxidizing species in the growing oxide layer. The oxidation rate can be described by the following equations

$$\frac{dX_0}{dt} = \frac{B}{A + 2X_0} \quad (10)$$

$$A = 2D_{\text{eff}} \left(\frac{1}{k} + \frac{1}{h} \right) \quad (11)$$

$$B = 2D_{\text{eff}} \left(\frac{C^*}{N_1} \right) \quad (12)$$

where: X_0 = thickness of the oxide layer

t = time

D_{eff} = diffusivity of oxidant in the oxide layer

k = surface reaction rate constant

h = gas phase transport coefficient

C^* = equilibrium concentration of oxidant in the oxide layer

N_1 = number of oxidant molecules in oxide per unit volume

The linear-parabolic model accurately describes oxide growth when the thickness is greater than approximately 500 Å. Modified models are required for thin oxides, under 500 Å. These can be analytical or numerical oxidation models depending upon the accuracy required.

2.5 Point Defect Models of Diffusion in Silicon

Earlier, theories describing diffusion processing employed in the fabrication of silicon integrated circuits were briefly discussed. These theories and their continued

development are vital for the technological progress of integrated circuit fabrication. Accurate computer simulation of dopant diffusion and implantation depends upon them. However, they can very quickly become extremely complicated when they try to predict diffusion behavior when many factors contribute to it. The project at hand is a case in point. Several steps involve diffusion of N-type and P-type dopants at high concentration in the silicon. The P⁺ buried layer, in order to form the collector of the vertical PNP transistor, must diffuse into heavily N-type antimony doped silicon. All of the diffusion drive-in steps oxidize the surface to thicknesses between 3000 Å and 8000 Å. The isolation process uses a spin on boro-silicate solution which forms a boron doped glass during the diffusion. Research in the literature uncovered several studies that discussed the effect of these conditions on dopant diffusions^{(2-5),(7)}. For example, it has been known for some time that during the oxidation of the silicon surface, silicon self-interstitials are injected into the silicon crystal^{(12),(13),(14)}. This drastically affects the diffusion of all of the primary impurities used to dope silicon in integrated circuit processing. In addition, as the oxidation proceeds, doped silicon is consumed. It is well known that the solubilities of the various dopants are different in silicon dioxide than those in silicon^{(2),(6)}. This results in the depletion or accumulation of dopant in the silicon at the oxide/silicon interface, depending upon the relative solubilities in oxide versus crystalline silicon. Annealing of the radiation damage is also affected by the oxidation of silicon. Stacking faults and other crystalline defects grow during oxidation processes. Therefore, it is vital to insure that any radiation damage is fully annealed before any oxidation begins. The research papers

which were reviewed and are presented in the upcoming sections discuss with the diffusion of dopants under similar conditions.

The effect of silicon lattice site vacancy and silicon self-interstitial point defects upon the substitutional impurity diffusion in silicon was studied by D. A. Antoniadis and I. Moskowitz of the Massachusetts Institute of Technology ⁽¹⁵⁾. In this study the diffusivities of arsenic, antimony, phosphorus and boron during the oxidation of the silicon surface were measured and compared to those under non-oxidizing conditions. They found that the diffusivities for arsenic, phosphorus, and boron were enhanced. The enhancement for these three elements was high at short oxidation time and fell to a steady state value for longer oxidation times. The diffusivity for antimony was enhanced for short oxidation times, but showed retardation as the oxidation time increased. Using the knowledge that silicon self interstitials are injected into the crystal during oxidation, and that the excess interstitials recombine with vacancies, the authors surmised that the diffusion of these impurities is controlled by a dual interstitial/vacancy mechanism. The initial enhancement of the diffusivity for all four elements indicates that the enhanced interstitial concentration increased their rates of diffusion. However, with time the injected interstitials recombined with vacancy point defects and reduced their concentration, also reducing the diffusivity with increasing time. They conclude that arsenic, phosphorus, and boron diffusion have a large dependency on interaction with silicon self interstitials. They also infer that the enhanced diffusion initially observed falls off, due to the reduction in vacancy concentration caused by the recombination with the injected interstitial silicon atoms.

Thus, arsenic, phosphorus, and boron diffusion is dominated by interaction with silicon interstitials, but their interaction with lattice vacancies also plays a role in controlling diffusion. Likewise, the initial enhancement of the antimony diffusivity can be attributed to the increased interstitial concentration. However, they concluded that antimony diffusion is primarily controlled by interactions with silicon lattice vacancies. This conclusion is supported by the fact that the rate of diffusion of antimony decreases with increasing time. It eventually becomes less than the diffusion rate in the absence of silicon oxidation. They attribute this to the reduction of silicon lattice vacancies by recombination with silicon self-interstitials. They also concluded that the recombination of vacancy and interstitial point defects is a slow process, with an activation energy of approximately 1.4 eV.

Similar results have also been reported by S. M. Hu from IBM ⁽¹⁶⁾. This work focused on the enhanced diffusivity due to interstitial injection at low temperature and short time. These processing conditions are the continuing trend in silicon wafer fabrication techniques. This makes the understanding of interstitial injection and its effect on impurity diffusivity under them important. Hu reports that the interstitial supersaturation is dependent upon the oxidation kinetics. At short time and low temperature the kinetics of interstitial supersaturation are linear. This is true up to a time, t_0 , which is determined by the onset of the parabolic oxidation region as described by the oxidation theory of Deal and Grove ⁽¹¹⁾. The characteristic time, t_0 , was shown to increase with decreasing temperature. The purpose of this work by Hu was to enable

prediction of the enhanced diffusion kinetics during low temperature oxidation processing.

Further support to the role of vacancies and interstitials in influencing the diffusion of impurities in silicon is given by P. Fahey *et al.* of Stanford University ⁽¹⁷⁾. Their work studies the diffusion of arsenic, antimony, and phosphorus in silicon during thermal nitridation with ammonia, NH_3 . The specimens under investigation were silicon wafers with a thin layer of thermal oxide covering some regions and in other regions only bare silicon. Direct nitridation of the bare silicon surface injects excess vacancies into the crystal. The nitridation of a silicon surface with a thin layer of oxide injects excess interstitials, similar to thermal oxidation. The diffusion of the impurities during nitridation under each region were studied and compared. Their findings showed that under the influence of interstitial injection, the diffusion of phosphorus under the regions with a thin oxide layer was substantially enhanced, that of arsenic was enhanced to a lesser degree, and that of antimony was retarded. This is consistent with the work reported previously by Antoniadis and Moskowitz ⁽¹⁵⁾ and also that of Hu ⁽¹⁶⁾. Under the influence of vacancy injection, the diffusion of antimony and arsenic under the bare silicon surface were substantially enhanced. The diffusion of phosphorus in these regions was substantially retarded. From these results they conclude that phosphorus diffusion is almost entirely controlled by its interaction with silicon interstitials, while antimony and arsenic diffusion are largely controlled by their interaction with vacancies. Their conclusion that antimony diffusion is controlled by vacancy interaction is consistent with the other researchers previously mentioned ^(12 - 16). However, conflicting with others is the conclusion that

arsenic diffusion is controlled primarily by interaction with vacancies.

2.5.1 High Concentration Phosphorus Diffusion

In reviewing the available literature it was evident that such inconsistencies and disagreements were common. The theories of impurity diffusion in silicon are very complicated and in many instances poorly understood. The case mentioned above is one example. Another is the theories and models presented in two papers which discuss the diffusion of phosphorus in silicon. The diffusion of phosphorus shows some well known characteristics which cannot be modeled by the simple diffusion theories. Diffusion of phosphorus in high concentrations, primarily at the silicon surface, is known to exhibit a flat region which extends into the crystal a distance not predicted using the usual models. At the edge of this flat region, abruptly, the concentration profile becomes very steep. This steep profile continues for a short distance and then the concentration profile again abruptly changes at lower concentrations to a broad tail with a much shallower slope. These observations have been explained both by phosphorus interactions with silicon self interstitials and by phosphorus interactions with silicon lattice vacancies. Both theories also explain the observed emitter push effect resulting when phosphorus diffusing in boron doped silicon causes enhanced diffusion of the boron. The effect is that the boron appears to have been pushed ahead of the diffusing phosphorus. Reviewing the literature it became apparent that adherents of one school of thought seem to very strongly disagree with those of the other.

The first paper was written by S. M. Hu *et al.* of Stanford University ⁽¹⁸⁾. Work by

Hu has been discussed previously in this report ⁽¹⁶⁾. Their conjecture is that on the surface, in the flat concentration region, the phosphorus is entering the silicon lattice in supersaturation as both interstitial ions and substitutional ions. They cite evidence that phosphorus-rich phases are precipitating into the crystal to help support the assumption of supersaturation. The diffusion of the phosphorus under the condition of supersaturation would account for the constant concentration of substitutional phosphorus and the flat concentration profile. They theorize that the phosphorus is diffusing using both a vacancy and interstitialcy interaction mechanism. An interstitialcy, as opposed to a silicon self interstitial, is described as a phosphorus ion and silicon atom pair sharing a lattice site. It can be considered one form of interaction of the diffusing phosphorus ion and a silicon interstitial. The dissociation of the phosphorus ion/silicon atom interstitialcy creates a substitutional phosphorus impurity and a silicon self interstitial. This dissociation creates an excess concentration of silicon self interstitials which then further interact with the phosphorus and other impurities in the silicon. This enhances their movement through the crystal lattice. The authors believe this interaction of excess interstitials to be the cause of the sudden steepening of the concentration profile and subsequent broadened tail region observed in phosphorus diffusion. They also believe that the excess silicon self interstitials created upon the dissociation of the phosphorus silicon pair enhances the diffusion of boron, creating the emitter push effect, when it is present below the diffusing phosphorus. This theory is consistent with Hu's previous work ⁽¹⁶⁾ regarding the oxidation enhanced diffusion of boron and phosphorus due to injection of silicon self interstitials during

oxidation.

Another theory presented to explain the anomalous diffusion of phosphorus is the widely accepted model of R. B. Fair and J. C. C. Tsai of Bell Laboratories ⁽¹⁹⁾. Their theory of phosphorus in silicon assumes that it is totally controlled by interactions with vacancies in the lattice. They propose that at high phosphorus concentrations, the phosphorus and lattice vacancy form pairs in which the phosphorus ion has a single positive charge, and the vacancy is double negatively charged. The concentration of these pairs remains constant until the electron concentration in the crystal drops and the pair loses an electron. They further theorize that the binding energy of the singly positive phosphorus and now singly negative vacancy pair is less. It is therefore more likely to dissociate. The increased dissociation rate creates substitutional phosphorus and unpaired silicon lattice vacancies. The increase in unpaired lattice vacancy concentration increases the diffusion rate of phosphorus and other impurities due to the increased likelihood of their interaction. They also propose that the increase in the vacancy concentration is also responsible for the enhanced boron diffusion in the emitter push effect.

As the development of the theory of diffusion in silicon continues, controversy and disagreements among researchers is likely to continue. As time progresses these theories and models will hopefully become more consistent and provide improved insight into the complicated phenomena that control impurity diffusion in silicon. The review of the published research regarding the development of diffusion models in silicon has provided bountiful information applicable to the development effort proposed.

There are two other phenomenon which warrant mention in the discussion of deviations from modeled diffusion behavior. They are surface impurity redistribution during the oxidation of silicon and outgassing and autodoping during epitaxial growth.

2.6 Surface Impurity Redistribution During Silicon Oxidation

During the oxidation of the silicon surface, impurities in the silicon at the surface are redistributed ^(2,6). Their redistribution depends upon the rate of oxidation of the silicon, their relative solubilities in the silicon and silicon dioxide, and their rates of diffusion in silicon and silicon dioxide. This causes a surface depletion or enhancement which is not accounted for in simple diffusion theories.

It is known that of the four major dopants used in integrated circuit production, boron is most soluble in the growing oxide layer and segregates into it. The result is a depletion of the boron in the silicon surface. J. W. Colby and L. E. Katz ⁽²⁰⁾ report that this effect is more pronounced for $\langle 111 \rangle$ silicon than for $\langle 100 \rangle$ silicon. They also report that it decreases with increasing temperature in the range of 1000 °C to 1200 °C.

The N-type dopants, arsenic, antimony, and phosphorus exhibit the opposite effect. They are more soluble in the silicon and therefore segregate into it during oxidation. The result for these dopants is a build up of dopant in the silicon surface.

A parameter called the segregation coefficient, m , is defined as the ratio of the equilibrium concentration of the impurity in the silicon versus the concentration in the silicon dioxide.

$$m = \frac{[\text{Impurity Concentration in the Silicon}]}{[\text{Impurity Concentration in the Silicon dioxide}]} \quad (13)$$

Experimentally measured values for the segregation coefficient for boron estimate it at 0.3. Values for the segregation coefficient for arsenic, antimony, and phosphorus have been experimentally measured at approximately 10.

The relative diffusion rates of the impurities also significantly affect the concentration profiles at the silicon surface and at the interface. Impurities with rapid diffusion in silicon dioxide move away from the interface quickly. This keeps the concentration below saturation and more impurity is removed from the silicon to establish equilibrium in the oxide.

The oxidation rate also affects the redistribution of impurities at the silicon surface. The silicon dioxide volume is twice that of the silicon. Thus, the faster the growth rate, the more impurity which must be depleted from the silicon in order to maintain equilibrium concentration in the oxide.

2.7 Autodoping During Epitaxial Growth

At the high temperatures usually encountered during silicon processing, impurities already incorporated in the silicon diffuse out of the crystal and into the gaseous processing ambient. They are then free to move via free or forced convective mechanisms. They can redeposit elsewhere on the silicon surface and reincorporate into the crystal. This phenomenon, called auto-doping, can be a major problem at the epitaxial growth step. Here, the silicon contains heavily doped N type and/or P type regions.

During epitaxy, the impurities in these regions diffuse out of the surface rapidly and can redistribute into previously undoped regions. This can drastically affect the threshold voltage and other electrical parameters.

A paper by M. W. M. Graef *et al.* ⁽²¹⁾ describes this phenomenon. They also provide information regarding the effect of processing conditions such as temperature, predeposition bake time, pressure, and chloride ion concentration on the level of lateral autodoping. For example, they demonstrate that reduced pressure can reduce the amount of autodoping when arsenic or antimony are the dopants in the substrate. However, the rate of lateral autodoping when boron is the dopant is increased at lowered pressure.

In this development work, the replacement of arsenic with antimony as the buried N⁺ dopant was done to reduce the lateral autodoping effect. The data presented in the work of Graef *et al.* comparing the peak lateral autodoping shows a reduction of at least an order of magnitude using antimony rather than arsenic. This supports the decision to move to antimony doped N⁺ buried layers.

2.8 Computer Simulation of Doping Processes

The preceding sections describe the types of models which have been proposed and used in computer simulation of semiconductor doping processes. The parameters associated with these models have been determined through extensive experimentation by the various researchers. In the case of thermally controlled diffusion process, the models utilize equations similar to Equation 8 with the various diffusivity terms modeled as a function of temperature using the Arrhenius relationship given in Equation 5. Important

for accurate simulation using such models is the accurate determination of the dominant types of point defect interaction for each of the substitutional impurities. Equally important is the determination of the frequency factors, D_0 , and the activation energies, E_a , which model the temperature dependence of the diffusivities, D^* , D^+ , and D^- from Equation 8 for the different impurities. Experimentally determined values for these parameters are contained in the simulation software used in this thesis.

During a simulation run, the overall diffusivity, as a function of temperature and impurity concentration in the silicon, for each impurity must be calculated to determine the concentration profiles which are expected for the simulated process. Both the temperature and concentration can change with time. This makes the calculation process an iterative one. Many parameters must be calculated over and over for numerous points in a simulation grid which represents various points within the silicon.

Parameters describing the ion implantation process such as R_p and ΔR_p and the effect of channeling in the crystal lattice were also determined via experimentation as were parameters for oxidation and epitaxial growth. They are also available in the software.

Good agreement between experimental data and simulated data determine whether or not the model is acceptable for predicting the physical behavior during processing conditions. However, the models which have been developed for process simulation do not always provide an adequate representation for all processing conditions. Most often the simulation model must be tailored to each individual situation. Experimentation and extraction of new model parameters cannot be done due to the excessive cost and

considerable time involved. In such cases parameters must be modified and the simulated results compared against measured process data. Extensive modification of the diffusion and other parameters were required for the simulation work done for this thesis. The modifications and the work done to verify them are discussed in detail in the next chapter.

2.9 Summary

Success in this development effort depended upon understanding and controlling impurity diffusion during high temperature processing. Simple models for impurity diffusion in silicon are well known, but do not predict diffusion behavior except under the most idealized conditions. Silicon oxidation, impurity outgassing, crystalline defects, and overall impurity concentration all affect the impurity diffusion and, hence, final impurity concentration profiles.

Ion implantation doping processes were also developed to replace some thermal deposition processes. The impurity concentration profiles resulting from ion implantation are very different from those obtained with diffusion processes. In addition, the implanted ions disrupt the crystalline structure of the silicon. Proper implantation and annealing conditions minimize the damage to the crystalline silicon. Understanding of these issues and the subsequent diffusion of the implanted ions was also key to the success of the development effort.

A review of the abundant supply of research reports, technical articles, and textbooks has provided an insight into the complicated processes of impurity diffusion in silicon and ion implantation into silicon. The published research presented in this report is

only a tiny percentage of what is available. There are many more research reports and published literature. The papers presented in this report give one a general overview of the basic theories involved in diffusion and ion implantation in silicon. They also exemplify the complicated and varied mechanisms which come into play in describing these phenomena.

Computer simulations of the new processes were a major portion of the process development. The models used in the simulations come directly from the research described in most of the papers reviewed in this report. Modification of the model parameters was required to obtain meaningful simulation results. Correct interpretation of the simulation results and final experimental results depended upon understanding the research that has been conducted on impurity diffusion and ion implantation in silicon.

Chapter 3. Simulation Software and Parameter Modification

3.1 Introduction

The advantages of using simulation software for process development are obvious. Processing wafers is expensive and time consuming, especially if several trials are necessary to get the desired result. Using simulation software one is able to obtain results for many trials in an extremely short time without the expense of processing wafers. The accuracy of the results depends directly upon the ability of the simulation to model the chemistry and physical behavior occurring under process conditions. To assure that the simulations used for this thesis were accurate, the data they generated were verified using measured process data.

Our experience has shown us that initial attempts at simulating process conditions often do not succeed. Modifications to the model parameters are required to get the accuracy necessary to obtain meaningful simulation data. Fortunately, sufficient measured data from wafers processed under the same conditions as those being simulated were available for model modification and verification. This was the most time consuming step of the simulation process and was primarily a process of trial and error. Once the simulation modification was complete, and the output adequately verified against the available data, running the simulations to characterize the proposed processes took relatively little time.

The simulation software used for this project was the ATHENA package from Silvaco Corporation. The SSUPREM4 module in ATHENA was of primary importance.

It was used to simulate the diffusion, epitaxy, oxidation, and implantation processes described in the previous chapters. Spreading resistance probe (SRP) data of existing, well-documented processes were used as a base line and provided information to validate and modify the models used for the simulations. Once a good match between the available spreading resistance probe data and the simulation output was obtained, numerous simulations were run to characterize the proposed changes in processing sequence, dopants, times and temperatures.

3.2 Spreading Resistance Probe

The spreading resistance probe data shows the activated net impurity concentration and type as a function of depth into the silicon. This data is obtained by cleaving a portion of the silicon wafer through a region that contains the impurity diffusion being characterized. The cleave is then beveled at a shallow angle. The shallower the diffusion, the shallower the angle required to get good resolution of the data versus depth. The silicon is probed in steps through the bevel and the resistivity is measured as a function of depth. The impurity concentration can be calculated from the resistivity versus depth data. Figure 8 illustrates this procedure. Figure 9 shows an example of the data.

Figure 8. Spreading Resistance Probe Technique.

Figure 9. Spreading Resistance Probe Data

The simulation of diffusion and implantation processes shows, for the case of one dimensional simulations, the dopant concentration as a function of depth. Matching the one dimensional simulation results to the spreading resistance probe data was a matter of changing the dopant diffusion coefficients or other variables in SSUPREM4.

3.3 ATHENA Simulation Software

The ATHENA software consists of several program modules which are capable of simulating every aspect of semiconductor wafer fabrication. SSUPREM4, the primary module used for this project, provides models for diffusion, oxidation, epitaxy, and implantation processes. Oxidation rate constants for silicon, diffusion parameters, and implant parameters of numerous impurity dopants in silicon have been characterized and are available within the software. Also available in ATHENA are program modules for simulating CVD deposition, photolithography, photoresist development, wet etch, and plasma etch.

Preparing a simulation deck entails composing a set of text statements which describe the processing conditions. The default parameters associated with the various dopants can be changed by inserting the proper statements where appropriate. Statements defining output files for plotting can also be inserted where desired.

The simulations can be done in one or two dimensions. The simulation of diffusion and implantation processes shows, for the case of one dimensional simulations, the dopant concentration as a function of depth in the silicon. An example of a one dimensional simulation plot is shown in Figure 10.

Figure 10. One Dimensional Simulation

Two dimensional simulations show concentration contours as a function of distance in both X (lateral diffusion) and Y (vertical diffusion). An example of a two dimensional simulation plot is given in Figure 11.

Figure 11. Two Dimensional Simulation

3.3.1 The Simulation Deck

The text statements which detail the processing conditions and sequence are collectively referred to as the simulation deck. It describes the dimensions, materials, and processes used in the model. The first statements in the deck define the simulation grid. The grid defines the dimensions and resolution of the simulation. The next statements define the substrate material and resistivity. The individual processing steps follow in the sequence that they normally occur. The text for each step defines the conditions used in the process. For example, simulation text of ion implantation defines the species, dose, and energy. Diffusion simulation text defines the species, temperature, time, pressure, and ambient. Simulation parameters can be changed by defining the new values where desired. Statements creating output files with the simulation data can be inserted where desired. The data from these files can be plotted and viewed after running the simulation. A complete simulation deck for the new process is included in the Appendix.

3.3.2 Text Statements

The text statements describing the process sequence are straightforward and self explanatory. They can be written directly in ATHENA, or using any ASCII text editor and copied into ATHENA. Changes to the processing conditions can be made by editing the text and running the simulation again. The following example demonstrates how the text statements are written and how they are interpreted.

```
init silicon boron resistivity=14 orientation=1 1 1
```

```
implant arsenic dose=2e15 energy=80 pearson tilt=0 rotation=0
```

impurity i.arsenic dix.0=5.0

diffus time=60 temp=800 t.final=1100 f.n2=5.0 f.o2=3.0 press=1.00

diffus time=90 1100 weto2 press=1.00

diffus time=60 temp=1100 t.final=800 f.n2=5.0 f.o2=3.0 press=1.00

etch oxide all

The statements above define the following process. The substrate is defined as silicon doped with boron. The substrate resistivity is 14 ohm-cm and its orientation is $\langle 111 \rangle$. Arsenic is implanted with a dose of 2×10^{15} ions/cm² at 80 keV. The tilt and rotation of the wafer relative to the ion beam are 0°. The frequency factor of the diffusion coefficient for arsenic diffusing with neutral point defects is changed from the default to 5.0 cm²/s. The wafer is then processed through a diffusion/oxidation process. The first step is 60 minutes. The temperature is ramped from 800 °C to 1100 °C with a N₂ flow of 5.0 slpm and an O₂ flow of 3.0 slpm. The pressure is 1 atm. The next step is a 90 minute cycle at 1100 ° in oxygen saturated with water vapor. The final diffusion step ramps the temperature from 1100 °C to 800 °C with the N₂ and O₂ flow at 5.0 slpm and 3.0 slpm. The last statement removes all the oxide from the simulated silicon surface.

3.3.3 Simulation Grid

Development of the simulation model begins with the definition of a grid on which the simulation calculations are performed. The grid defines the resolution accuracy of the calculations. The finer the grid, the greater the number of calculated data points are generated for a given area. In critical areas requiring greater resolution for accurate

simulation, the grid can be made finer. However, finer grids require greater computing time. The execution time for the simulations can become quite long, especially for two dimensional simulations.

Because the dopant profiles in the processes that were simulated are relatively deep, the grid chosen was large and coarse. Initially, a 10 μm by 10 μm grid with 0.5 μm spacing both in X and Y was chosen. This provided adequate resolution at the outset. Problems arose with this choice when Sb and B implant simulations were attempted. Discussion of this point will follow in forthcoming sections.

Initially, all of the simulations were done in one dimension. In one dimension, the X (lateral) grid is not included in the calculations. Two dimensional simulations were subsequently done to determine the amount of lateral diffusion of the isolation for both the old 12 volt process and the proposed new process.

3.4 SSUPREM4 Model

The SSUPREM4 models for impurity diffusion in silicon, ion implantation in silicon, silicon oxidation, and epitaxial growth on silicon were the models employed in this work. Of primary concern was the model for impurity diffusion. For the 12 volt process, dopant introduction into the silicon is achieved, in most cases, by thermally controlled diffusion processes. When the dopants are implanted into the silicon, the subsequent drive-in processing diffuses the dopants to a depth exceeding 1.0 μm . Most junction depths are several microns deep. The implantation energies used result in junction depths of at most 0.2 μm . Thus, even when the dopants are introduced via implantation, the

assumption has been made that the as implanted dopant distributions are not crucial. The subsequent thermal processing controls the final impurity distribution. Attention has also been given to the model for segregation of dopants at the oxide/silicon interface. The proper simulation of this phenomenon is crucial to properly simulate the expected dopant concentration at the oxide/silicon interface.

3.4.1 Epitaxial Growth Model

Epitaxial growth of silicon is modeled as a conformal deposition of single crystal silicon on the surface of the substrate. The thickness of the epitaxial layer is uniform over the entire simulation surface. If topology is present on the surface it is covered with a uniform thickness with uniform step coverage. The impurity concentration is uniform throughout the thickness of the layer. The dopant, concentration, process temperature, growth rate and process time are specified in the epitaxy statement. During the epitaxy process, the diffusion of all dopants in the silicon are simulated using the diffusion models in SSUPREM4 at the temperature specified in the epitaxy statement.

3.4.2 Oxidation Model

For this work, the unmodified linear-parabolic model described in Chapter 2 was used. It adequately modeled the oxidation of silicon for the processes under consideration.

3.4.3 Ion Implantation Model

The Pearson distribution model is available within the ATHENA simulation software. It was the model employed for the implant simulations in this project and was

assumed to be of sufficient accuracy without modification. As mentioned previously, the ion energies typically used for semiconductor implantation processes result in the projected range being less than 0.2 μm deep. In the newly developed process, the final junction depths are considerably deeper than this and are primarily controlled by the diffusion processes following the ion implantation. This enabled us to use the Pearson model unmodified. Discrepancies between the simulation data and measured data were accounted for by modifying the diffusion parameters.

3.4.4 Diffusion Model

Modeling of the diffusion processes was of most importance for this project. These processes have the greatest influence on impurity concentration profiles and therefore on the electrical parameters of interest. Care was taken to adjust the diffusion parameters of the various impurities such that the software would accurately simulate the expected impurity concentration profile versus depth in the silicon for the conditions of the experiments.

The thermally controlled diffusion of impurities in silicon are modeled in the ATHENA software by Equation 14.

$$\frac{\delta C_T}{\delta t} = \nabla(D_v C_A) \frac{C_v}{C_{v*}} \nabla \log \left[C_A \frac{C_v}{C_{v*}} \frac{c}{n_i} \right] + \nabla(D_i C_A) \frac{C_i}{C_{i*}} \nabla \log \left[C_A \frac{C_i}{C_{i*}} \frac{c}{n_i} \right] \quad (14)$$

where: C_T = total impurity concentration

t = time

D_v = intrinsic diffusivity due to vacancies

D_i = intrinsic diffusivity due to interstitials

C_A = active dopant concentration

C_v = vacancy concentration

C_i = interstitial concentration

C_v^* = equilibrium vacancy concentration

C_i^* = equilibrium interstitial concentration

n_i = intrinsic electron concentration at T

c = n or p (electron or hole concentration)

Equation 14 accounts for the effect of temperature and impurity concentration on D_v and D_i as well as the electric field E.

The fractional interstitialcy factor, F_i , is a measure of how much the impurity diffusion is controlled by interactions with interstitials. It is one of the parameters determined experimentally and is used to calculate D_v and D_i . It is given by Equation 15.

$$F_i = \frac{D_i}{D_v + D_i} \quad (15)$$

where: D_i = intrinsic diffusion coefficient associated with interstitials

D_v = intrinsic diffusion coefficient associated with vacancies

Default values of F_i are given for each dopant in SSUPREM4. The F_i for antimony is 0.05. Thus, antimony diffusion is primarily controlled by vacancies. The F_i for boron is 0.94. Its diffusion is dominated by interstitials. The F_i for arsenic is 0.20. The F_i for

phosphorus has not been determined due to the poor understanding of how it diffuses in silicon.

The intrinsic diffusion coefficients of the impurities due to interstitials, D_i , and vacancies, D_v , are determined using F_i , the intrinsic diffusivity of the dopant atom, D_i^{in} , and the electron concentration, n . They are given by the following Equations 16 and 17.

$$D_i = F_i D_i^{\text{in}} \quad (16)$$

$$D_v = (1-F_i)D_i^{\text{in}} \quad (17)$$

where: F_i = fraction interstitialcy factor

D_i^{in} = intrinsic diffusion coefficient of the i^{th} impurity

The intrinsic diffusion coefficient, D_i^{in} , is modeled as a function of the interaction of the dopant with point defects of various charge states and the electron concentration. This is shown in Equation 18.

$$D_i^{\text{in}} = D_i^{\times} + D_i^{-} \left(\frac{n}{n_i} \right) + D_i^{=} \left(\frac{n}{n_i} \right) + D_i^{+} \left(\frac{n_i}{n} \right) \quad (18)$$

$D_i^{\times}$ = diffusivity of i^{th} impurity associated with neutral defects

D_i^{-} = diffusivity of i^{th} impurity associated with single negative defects

$D_i^{=}$ = diffusivity of i^{th} impurity associated with double negative defects

D_i^{+} = diffusivity of i^{th} impurity associated with single positive defects

These coefficients are modeled in SSUPREM4 using an Arrhenius activation model as a function of the process temperature, Equation 5. Equation 18 is the same as Equation 6

when only neutral, single negative, double negative, and single positive point defects are considered.

The model for diffusion used in the simulations assumes that it occurs under equilibrium conditions. This means that the electron concentration, vacancy concentration, and interstitial concentration are all at equilibrium levels, and are a function of the Fermi level and temperature only. Based upon the literature review, this is likely a poor assumption. However, any non-equilibrium effects, such as interstitial injection during oxidation, have been successfully absorbed into the modified diffusion parameters. Modeling of non-equilibrium effects would require extensive experimentation and evaluation. We had neither the time nor the equipment to accomplish the characterization which would have been required.

3.4.5 Dopant Segregation Model

During oxidation of the silicon, impurities in proximity to the oxide/silicon interface will segregate either into the growing oxide layer or into the silicon. The N-type dopants As and Sb are known to accumulate in the surface silicon, causing an enhanced surface concentration of these dopants. The P-type dopant boron is known to preferentially segregate into the oxide layer. This causes a depleted concentration in the surface silicon. The segregation at an interface is modeled by Equation 19.

$$F_s = h \left[\frac{C_1}{m} - C_2 \right] \quad (19)$$

where: F_s = dopant flux across the boundary from material 1 to material 2

h = transport coefficient

m = segregation coefficient, from Equation 13

Both the transport coefficient, h , and the segregation coefficient, m , are modeled as a function of temperature by an Arrhenius activation model similar to Equation 5.

3.4.6 Adjustments to the Simulation Model

All of the parameters defined in Equations 13 through 18 can be adjusted by the user. In this work, many of the diffusion parameters for the various impurities were adjusted. Because the available process data was usually limited to a single temperature, changing the activation energy, E_A , was not appropriate, and only the pre-exponential constant term D_0 , in Equation 5 was changed. This was done using a trial and error method. D_0 was increased or decreased until an acceptable match of the simulation results to processing data was obtained. In general, D_0 is an experimentally fit parameter and the physics determining its magnitude are not well understood. On the other hand, the activation energy is not expected to vary much and its magnitude for different dopants is fairly well accepted.

Similarly, the segregation coefficients used in Equation 18 were modified to properly model the oxide/silicon interface dopant concentrations. This parameter is also modeled using an Arrhenius model. When modifications were required, only the temperature independent pre-exponential constant term was changed.

The methods used by SSUPREM4 to simulate the diffusion process often were

inadequate representations of the actual processing. An example is the simultaneous oxidation and diffusion occurring during the thermal doping steps. Another example is the doped spin-on glass used as the impurity source at the As buried layer and B isolation steps. To overcome these inadequacies, modifications were sometimes made to the process ambient in the simulation. These changes were rationalized based on the inadequacies of the simulation model and the process conditions. This approach, in combination with changing the diffusion parameters, was successful. Specifics of the methods used to get accurate simulations will be described in the following sections which detail each process step.

3.5 Model Verification and Modification

The development of the simulations was completed by matching, as closely as possible, the dopant concentration profiles measured by spreading resistance probe to those calculated by the simulation program. The spreading resistance data were obtained from three different processes in production at Philips. The existing 12-volt process provided data for the epitaxial layer, isolation diffusion, NPN collector plug diffusion, and NPN base diffusion. A similar bipolar analog process provided data for verification of the isolation diffusion parameters at 1150 °C. An existing 25 volt analog bipolar process provided the data for the parameter modification of the implanted antimony N+ buried layer and the boron P+ buried layer.

A goal during the modification step was to determine a set of parameters for each dopant that would adequately model their diffusion throughout the entire process. This

was especially a concern for the simulation of boron diffusion since boron is used as the dopant for the buried P+ layer, the isolation, and the NPN base.

Three criteria were used to determine when an adequate match was obtained. The first was the depth of the junction, or the depth of the diffusing species if no p/n junction was formed. The second was the peak concentration of the diffused species and its location within the silicon. The third criteria was the impurity concentration at the silicon/oxide interface. An exact match for these criteria was not achieved in every case. When a good match was obtained, often the shape of the profiles differed. However, even without an exact match of the dopant profiles, enough information was obtained from the simulation experiments to draw useful conclusions. The simulation deck for the new 12 volt process is given in the Appendix. Modifications to each diffusion step are described in the next sections.

3.5.1 Initial Oxidation

Oxidation is the first high temperature step. No dopants have been introduced into the silicon at this point except the background substrate dopant. It is not a critical step in the simulation. During this step 14,000 Å of oxide is grown on the silicon surface. The simulation text was taken directly from the process specification.

3.5.2 Arsenic Buried N+ Layer

Following the first masking step, the N+ buried layer is diffused into the silicon. Simulation of arsenic diffusion was done to gain familiarity with the software and how well it simulated the actual physical process. Implanted antimony is being used for this

step in the new 12 volt process.

This diffusion is done in a two step operation. First, an As doped glass is spun on the wafer and serves as the dopant source. The arsenic deposition is done at 1070 °C in an N₂ and O₂ ambient. This step dopes the silicon with the proper amount of arsenic. Next, the oxide in the diffused regions is dipped off in 1:10 HF. The arsenic drive-in process is done at 1250 °C. The simulation text follows.

```
#BN arsenic Deposition
method fermi compress
diffus time=60 temp=800 t.final=1070 f.n2=4.0 press=1.00 c.arsenic=1.0e20
diffus time=30 temp=1070 f.n2=4.0 press=1.00 c.arsenic=1.0e20
diffus time=30 temp=1070 press=1.00 c.arsenic=1.0e20
diffus time=60 temp=1070 t.final=800 press=1.00 c.arsenic=1.0e20
```

```
#Clean 16 Dip off oxide in BN cuts
etch oxide all
```

```
#BN arsenic diffusion
method fermi compress
diffus time=60 temp=800 t.final=1250 f.n2=4.0 f.o2=0.8 press=1.00
diffus time=310 temp=1250 f.n2=4.0 f.o2=0.8 press=1.00
diffus time=75 temp=1250 t.final=800 f.n2=4.0 f.o2=0.8 press=1.00
```

In the simulation no oxygen flows during the arsenic deposition. However, the process specification calls for a flow of 4.0 slpm. The oxygen was eliminated in the simulation because it was unable to accurately simulate the simultaneous oxidation and As diffusion into the silicon surface. The text “c.arsenic=1.0e20” in the simulation deck dictates that the As concentration in the gaseous ambient is at a concentration of 1.0e20 atoms/cm³. The simulation models the diffusion by calculating the diffusion from the ambient onto the silicon surface, and then into the silicon. This is not an accurate model

for this process. The actual process uses a 2000 Å thick layer of As doped spin-on glass for the arsenic source. This layer inhibits the oxidation of the silicon by the ambient oxygen and enhances the rate of arsenic diffusion into the silicon. Elimination of the oxygen flow during the arsenic deposition step helped to provide an accurate simulation of the arsenic diffusion during this step.

3.5.3 Antimony Buried N+ Layer

The antimony N+ buried layer employs ion implantation to introduce the dopant into the silicon. The first simulations of this process step resulted in the antimony concentration much lower than expected, approximately 7 orders of magnitude too low! Initially, the dose was adjusted in the simulation to bring the concentration up. However, this required an 8-fold increase over the actual dose. This was unacceptable. Eventually, it was determined that to accurately simulate the implantation process the grid needed to be much finer in the surface silicon region where the ions were implanted. Modification of the grid spacing to 0.05 µm in the first 0.5 µm of the surface solved this problem. All subsequent simulations were done with this spacing at the surface. Below 0.5 µm from the surface the grid spacing was changed to 0.2 µm. Modification of the antimony diffusion coefficients was not required once the grid modifications were made.

3.5.4 Boron Buried P+ Layer

The boron dopant is also introduced into the silicon via ion implantation at this step. In the initial simulations, the boron concentration in the silicon was much too low. After redefining the grid at the surface, a much closer match to the measured profile was

obtained.

The buried boron step was the last diffusion step simulated. The boron diffusion coefficients had already been modified and defined for the isolation and NPN base process. Using them gave a simulated profile that did not match the measured data for the P+ buried layer. In particular, the peak doping inside the silicon was too high. However, the simulated depth of the diffusion and the up-diffusion into the epitaxy was acceptable. It was decided not to further modify the boron diffusion parameters. This would have entailed considerable work at isolation and NPN base to match the profiles again with new diffusion parameters.

3.5.5 Epitaxial Growth and Oxidation

Simulation of the epitaxial layer growth involves simply specifying the thickness, growth time, temperature, dopant species, and dopant concentration in the silicon. The subsequent oxidation of the epitaxial silicon surface changes the oxide/silicon interface As concentration. Arsenic's propensity to segregate into the silicon from the oxide layer increases it. The spreading resistance probe data show the As concentration increase, but it is barely detectable. The default value for the arsenic segregation coefficient in oxide/silicon defined by SSUPREM4 is 30.0. It was reduced to 1.0 to accurately model the As oxide/silicon interface concentration from the spreading resistance probe data. A segregation coefficient of 1.0 sets the solubility of the arsenic in oxide equal to its solubility in silicon.

3.5.6 Isolation Diffusion and Oxidation

Following a masking and etch step, the wafers are processed through a high concentration boron diffusion step. The dopant source is a spin-on glass layer approximately 6000 Å thick. Following the diffusion, all of the oxide is stripped and the surface is reoxidized. As with the arsenic N+ buried layer, the simultaneous oxidation of and diffusion in the silicon was not modeled well by the simulation. Because the model cannot simulate the doped glass process, reduction of the ambient oxygen flow during the diffusion step, similar to that done in the As buried layer simulation, was required to overcome this problem. Modification of the pre-exponential coefficients for the boron diffusivity equations were also required to adequately simulate this diffusion step.

SSUPREM4 simulates boron diffusion by calculating the diffusion coefficients based on the interaction of the boron impurity with neutral point defects and single negative point defects. Diffusion coefficients are calculated for each interaction in the simulation model. The term `dix.0` represents the constant term for neutral defect interaction with boron. It was changed from 0.037 to 0.1. The term `dip.0` represents this term for interaction with single positive defects. It was changed from 0.72 to 1.2.

Development of the isolation model was done using the 1220 °C process. The reduced diffusion depth for isolation with the new 12 volt process required that the process temperature be lowered to 1150 °C. The parameter modification and ambient oxygen modification developed at 1220 °C were verified at 1150 °C by using spreading resistance probe data for an isolation process run at this temperature. No modifications to the diffusion parameters or process ambient were required when simulating the 1150 °C

process.

3.5.7 Plug Deposition and Diffusion

Masking and etch again define the regions for the plug diffusion. The phosphorus source is phosphine gas in an oxygen and nitrogen ambient. SSUPREM4 is unable to simulate the flow of phosphine in the ambient. Rather we specify the concentration of elemental phosphorus at the surface of the silicon. As previously encountered, the simultaneous oxidation of and phosphorus diffusion in silicon presented problems. This was circumvented by changing the pre-exponential coefficients of the phosphorus in both silicon and oxide.

The change of the phosphorus in oxide diffusion parameter was required to increase the phosphorus surface concentration and the total amount of phosphorus entering the silicon during the plug deposition process. The parameter `dix.0` for phosphorus in oxide was changed from $7.6\text{E-}03$ to $7.6\text{E-}02$. After the plug deposition process is complete, it is changed back to the default value, $7.6\text{E-}03$.

Changing the phosphorus pre-exponential coefficients in the silicon was necessary to simulate the proper junction depth as measured on the spreading resistance probe. Phosphorus diffusion in silicon is not well understood. The model in SSUPREM4 uses phosphorus interaction with neutral and single negative defects as well as double negative interstitials. The terms `dix.0`, `dim.0` and `dimm.0` represent the constant term in the Arrhenius model for these interactions. They were changed from 3.85 to 10.0, from 4.44 to 10.0, and from 44.2 to 50.0, respectively.

3.5.8 NPN Base Process

The boron deposition and diffusion at the NPN base step are two separate operations. The deposition uses solid BN ceramic disks as the boron source. The surface of these disks is oxidized to form a thin layer of B_2O_3 . The wafers are placed in proximity to these disks with the regions to be doped facing them. Introduction of a small amount of H_2 into the ambient causes the formation of boric acid, H_2BO_3 . The boric acid is volatile and diffuses via convection to the surface of the wafer and dopes the exposed silicon regions. The floating vertical PNP emitters are fabricated at this step.

The same types of simulation problems were encountered here. Initial attempts at simulating the measured boron concentration profile were not very accurate and modifications to the diffusion parameters were required.

The base step is a boron diffusion like the isolation step. The same pre-exponential coefficients already modified at isolation diffusion are used to simulate the diffusion. Considerable work had already been done to match the simulated isolation profile to the measured data. Thus, if possible, it was desirable to use these modified coefficients for the NPN base diffusion simulation. After a number of trials, this was accomplished. However, modification of the pre-exponential constant for boron diffusion in oxide was required during the base process simulation.

The modification of the pre-exponential term for diffusion of boron in silicon oxide was necessary to increase the amount of boron diffusing through the growing oxide layer and to properly model the final interface boron concentration at the silicon/oxide interface.

This parameter for boron diffusion in oxide, $d_{ix,0}$, was changed from $3.16E-04$ to $1.5E-02$.

3.5.9 NPN Emitter Diffusion and Oxidation

This step is not crucial to the fabrication of the components under development. The dopant at this step is phosphorus and it forms the emitters of the NPN transistors and ohmic contacts for the NPN collectors. The diffusion of the phosphorus in this step was not simulated. However, the time and temperature processing will affect the diffusion of dopants already in the silicon. Therefore, the NPN emitter step, with no phosphorus introduced into the silicon, was included in the simulation. It is the last high temperature step that was required in the simulation deck.

3.6 Summary of Results

The final simulation profiles and corresponding spreading resistance plots are shown in Figure 12 through Figure 18. Considerable effort was put forth to achieve the results. The simulation profiles are a very close match to the measured data, as can be seen from the comparison of the junction depths, peak concentrations and depths, and surface concentrations shown in Table 4. An identical match of the simulated profile to the measured profile was virtually impossible to achieve. This can be attributed to the limitations in the simulation software. Another problem is the amount of spreading resistance probe data available. Each profile only represents one sample wafer taken from many thousands processed each year. With such limited data, statistical variation cannot be accounted for and it is significant. However, the final results have proven to be

adequate for the purpose of determination of the wafer experiments.

A description of the simulation experiments and the experiments performed on wafers follows in the next chapter. The simulation results provided significant information for the prudent design of the actual experiments.

Process Step	As Buried N+ Diffusion		Sb Buried N+ Diffusion	
Plot	SRP	Simulation	SRP	Simulation
Junction Depth (μm)	15.00	14.00	17.40	17.70
Peak Conc. (cm^{-3})	7.0E+18	8.0E+18	6.0E+18	5.0E+19
Peak Depth (μm)	7.00	6.50	10.00	11.00
Buried N+/Epi Xj. (μm)	3.50	3.50	8.00	8.00

Process Step	Buried P+ Diffusion	
Plot	SRP	Simulation
Junction Depth (μm)	16.00	17.20
Peak Conc. (cm^{-3})	1.0E+17	2.0E+17
Peak Depth (μm)	10.00	10.50
Buried P+/Epi Xj. (μm)	5.00	5.50

Process Step	Epitaxial Layer	
Plot	SRP	Simulation
Junction Depth (μm)	6.30	6.50
Peak Conc. (cm^{-3})	4.0E+15	4.0E+15
Peak Depth (μm)	N. A.	N. A.
Surface Conc. (cm^{-3})	4.0E+15	4.0E+15

Process Step	1220 °C Iso Diffusion		1150 °C Iso Diffusion	
Plot	SRP	Simulation	SRP	Simulation
Junction Depth (μm)	8.80	8.70	7.00	6.50
Peak Conc. (cm^{-3})	3.0E+19	5.0E+19	1.7E+19	1.0E+19
Peak Depth (μm)	1.00	0.50	1.00	0.50
Surface Conc. (cm^{-3})	1.5E+19	1.0E+19	4.0E+18	4.0E+18

Process Step	Plug Diffusion		NPN Base Diffusion	
Plot	SRP	Simulation	SRP	Simulation
Junction Depth (μm)	6.00	6.30	1.20	1.30
Peak Conc. (cm^{-3})	4.0E+19	4.0E+19	4.0E+18	4.0E+18
Peak Depth (μm)	0.50	0.00	0.30	0.40
Surface Conc. (cm^{-3})	3.0E+19	4.0E+19	1.0E+18	2.0E+18

Table 4. Spreading Resistance Probe versus Simulation Results

Figure 12a. Antimony Buried Layer Simulation

Figure 12b. Antimony Buried Layer Spreading Resistance Probe

Figure 13a. Boron Buried P+ Simulation

Figure 13b. Boron Buried P+ Spreading Resistance Probe

Figure 14a. Epitaxial Layer Simulation

Figure 14b. Epitaxial Layer Spreading Resistance Probe

Figure 15a. 1220 °C Isolation Diffusion Simulation

Figure 15b. 1220 °C Isolation Diffusion Spreading Resistance Probe

Figure 16a. 1150 °C Isolation Diffusion Simulation

Figure 16b. 1150 °C Isolation Diffusion Spreading Resistance Probe

Figure 17a. Collector Plug Diffusion Simulation

Figure 17b. Collector Plug Diffusion Spreading Resistance Probe

Figure 18a. NPN Base Diffusion Simulation

Figure 18b. NPN Base Diffusion Spreading Resistance Probe

Chapter 4. Simulation Results and Design of the Experiments

4.1 Introduction

The processing steps involved in the development work have been discussed in the preceding chapters. Refer to Table 2, Figure 1, Figure 3, and Figure 4 for processing details and flow diagrams. Several of these steps have significant impact on the fabrication of device components and the electrical parameters that must be controlled. These steps are the buried P+ diffusion, epitaxial layer, and P+ isolation. The simulation and experimental design focused on these critical steps.

Other, less critical, steps are the N+ buried layer and N+ collector plug. The specific processing parameters for them were chosen based upon experience with other processes in production at Philips.

Prior to running wafer experiments, experimental simulations were performed using SSUPREM4 software. The wafer experiments were designed using the simulation results as a baseline.

4.2 Simulation Experiments

Initially, the existing 12 volt process was simulated and the results compared to spreading resistance probe data. This provided us with a measure of the accuracy of the simulation software. This procedure was outlined in detail in Chapter 3. Once this was complete, the simulation deck was written and simulated experiments were run. The specific goals of the simulation experiments were the following.

- 1) Determine the diffusion times for the isolation and collector plug diffusions for different epitaxial thickness.
- 2) Verify that the chosen variables and their settings were appropriate.
- 3) Quantify the expected reduction in the lateral diffusion of the boron isolation diffusion.
- 4) Determine the appropriate experiments to process in the fabrication area on wafers.
- 5) Determine if more, or other, parameters should be varied, and at what levels.

The results of the simulations were successful in providing answers to the questions listed above.

4.3 Process Simulation

This section describes in detail the changes at each process step. Also, it describes the simulation experiments, their results, and the experimental design which was subsequently run on wafers. The simulation experiments were first performed using an epitaxial layer thickness of 6.5 μm . Using this thickness, a series of simulations were run to determine the collector plug junction depth, lateral diffusion and vertical junction depth of the isolation, and the buried P+ up-diffusion into the epitaxy versus total diffusion time. From these results determination of the various diffusion times for subsequent simulations using a thinner epitaxial layer were made.

4.3.1 Sb Buried N+ Layer

This step plays a less significant role in controlling the parameters of interest in the

development. It primarily controls the current carrying capability of the NPN transistors. Other products using the up-down isolation scheme are successfully using an implanted antimony N+ buried layer. Therefore the same processes and specifications they employ were used. The implant dose was $3.5 \times 10^{15} \text{ cm}^{-2}$ at an energy of 80 keV. This was followed by the drive-in diffusion at 1250 °C for 5.25 hours. An oxide of 2200 Å was grown and the in-line resistivity is $3.2 \pm 0.3 \text{ ohms}$. These process conditions were not varied in the simulation work nor in the wafer experiments.

4.3.2 Buried P+ Layer

The buried boron P+ process is important for the proper control of the device parameters under development. Controlling how far the buried boron diffuses up into the epitaxial layer determines how far the top isolation must be diffused down to electrically isolate the active regions. Also, the gain of the floating vertical PNP transistor is greatly affected by the up-diffusion. The resistivity of the vertical PNP collector, which is fabricated from the buried P+ layer, controls the current carrying capability of this transistor.

The up-diffusion of the boron into the epitaxial layer is affected by the amount, or the dose, of boron implanted into the substrate. Also affected by the implant dose is the resistivity of the vertical PNP collector. Therefore, the simulated ion implant dose was varied to determine the effect of boron concentration on the isolation and vertical PNP transistor. Other products fabricated with an implanted buried P+ layer employ a boron dose of $2.0 \times 10^{14} \text{ cm}^{-2}$ at 100 keV. This dose and energy were used as the center point.

Variations around this center point were evaluated. The energy of the implanted ions was not changed. The boron diffusion after implantation was copied from other production processes.

The up-diffusion of the buried boron into the epitaxial layer, as a function of the total time at 1150 °C during the isolation and collector plug diffusions, was determined by measuring the thickness of the remaining N-type epitaxy above the buried P+ diffusion. This was measured from the oxide/silicon interface to the epitaxy/buried P+ junction. These data are plotted in Figure 19. The junction depth is plotted versus the square root of time resulting in a linear relationship.

Figure 19. Buried P+ up-diffusion versus (time)^{1/2} at 1150 °C.

As shown in Figure 19, the remaining N-type epitaxy is less than 3.0 μm thick for all combinations of plug and isolation diffusion times. Thus, for a 6.5 μm epitaxial layer, requiring a 50 minute plug diffusion, even the lowest isolation diffusion time used in the

simulations, 10 minutes, provided adequate isolation of the active regions.

Several buried P+ simulations in which the implant dose of the boron was varied by ± 15 percent were also run. These results show that the change in the concentration profile of the buried boron was almost imperceptible. Because of this result, changes in the buried boron dose were not pursued further.

The base of the floating vertical PNP transistor is formed from the N-type epitaxial layer between the NPN base diffusion and buried boron P+ region. The thickness of this N-type layer controls the current gain of this transistor. The data in Figure 19 show that the isolation diffusion time has a significant impact on the final thickness of this layer and should also have significant impact upon the gain of the vertical PNP transistor.

Similar simulations were repeated for epitaxial layers of 4.0 μm and 5.0 μm . The results and conclusions for these simulations are discussed in forthcoming sections.

4.3.4 Isolation Diffusion

The isolation diffusion step was also significant to the development effort. Employing an up-down isolation scheme to reduce the amount of boron lateral diffusion allows us to shrink the size of the circuit layout. The boron must be diffused deep enough to provide isolation, but not so deep as to lose any benefit provided by the new process. Ideally, the buried P+ layer and the top isolation will meet at approximately the center of the epitaxial layer, as measured following the isolation diffusion step. This assures adequate isolation and prevents over diffusion of the boron. The sheet resistivity target for the isolation diffusion is of minimal importance. Typically it is below 10.0 ohms/ $\square$.

The oxide thickness is unimportant because after the isolation diffusion, the wafers are processed through an oxide strip and then reoxidized.

The existing isolation process is done at 1220 °C. Because the required diffusion depth was significantly reduced, the temperature used for isolation diffusion was reduced to 1150 °C. The isolation diffusion time depends upon the epitaxial layer thickness and the up diffusion of the buried boron P+ layer. In addition, the subsequent collector plug processing must be taken into account. Products using the collector plug normally have the isolation time reduced because the boron diffusion to isolate the active regions is completed during the collector plug diffusion. Therefore, simulations were run in which the time of both the isolation and collector plug diffusions were varied. The same times used to simulate the buried P+ up-diffusion were used. The simulated boron isolation junction depth and lateral diffusion were measured and plotted in Figure 20 and Figure 21 as a function of the total diffusion time.

The vertical junction depth of the isolation must be deep enough to meet the up-diffusion of the buried P+ diffusion. The up-diffusion of the P+ boron was shown to leave about 3.0 μm of N-type epitaxy. With the collector plug diffusion set at 50 minutes for a 6.5 μm epitaxial layer, the shortest isolation diffusion time evaluated, 10 minutes, resulted in a junction depth of about 4.0 μm . This was more than adequate for isolation of the active regions.

Figure 20. Isolation vertical diffusion versus $(\text{time})^{1/2}$ at 1150 °C.

Figure 21. Isolation lateral diffusion versus $(\text{time})^{1/2}$ at 1150 °C.

Another goal of this work was to reduce the amount of boron lateral diffusion by 50 percent. Two dimensional simulation of the existing isolation process at 1220 °C for 30 minutes shows that the lateral diffusion, measured from the edge of the isolation

pattern, is approximately 6.0 μm . The edge of the isolation pattern was set at 2.0 μm from the right hand edge of the simulation plot. This is shown in Figure 22.

Figure 23 shows a two dimensional simulation of the isolation diffusion with a collector plug diffusion time of 20 minutes and a 20 minute 1150 °C isolation diffusion time. The lateral boron diffusion shown here is approximately 3.0 μm .

This result indicated our goal was attainable. However, as the simulation work continued it became obvious that a 50 percent reduction would not be possible. The reasons for this are given in the coming sections.

4.3.5 Collector Plug Diffusion

The collector plug diffusion time is also dependent upon the epitaxial layer thickness. Adequate time must be allowed during the diffusion to insure that the phosphorus dopant diffuses deep enough to contact the antimony N+ buried layer. This was done by varying the diffusion time in the simulation and measuring the resulting junction depth. The standard time is 50 minutes for 6.5 μm epitaxial layers. In these simulations, the diffusion time was varied around this point. The resulting data are shown in Figure 24.

As with the isolation step, the sheet resistivity of the collector plug is of minimal importance, provided that it is low enough. Typically 2.0 ohms or below is adequate. However, care was taken to insure that the oxide thickness was not changed. This was necessary to maintain the field inversion threshold voltage. The temperature of the collector plug diffusion process was maintained at 1150 °C.

Figure 22. 2D Simulation Plot of Isolation Diffusion at 1220 °C.

Figure 23. 2D Simulation Plot of Isolation Diffusion at 1150 °C.

Figure 24. Phosphorus Collector Plug Depth versus (time)^{1/2}

4.3.6 Epitaxial Layer

The epitaxial layer has the most significant effect upon component fabrication. Many component parameters are determined by the resistivity of the epitaxial layer, which is controlled by the incorporation of dopants into the layer during growth. The resistivity also influences the components under development, but in their case the thickness of the epitaxial layer is of primary concern. For this reason the resistivity of the epitaxial layer was maintained at the current target of 0.9 Ω-cm. Only the thickness was varied in the experiments. The processing temperature remained at 1080 °C and the silicon source remained dichlorosilane, SiH₂Cl₂.

The target epitaxial layer thickness is 6.5 μm for the existing 12 volt process. Achieving our goal to reduce the component spacing could be helped by employing a thinner epitaxial layer. Therefore, thicknesses of 4.0 μm and 5.0 μm were also

investigated using the simulations. The thickness of the epitaxy significantly affects the required depth and, hence, the amount of lateral diffusion of the boron at top isolation. The gain of the vertical PNP transistor is also significantly affected by the epitaxial layer thickness. Determination of the thinnest possible epitaxial layer, while maintaining an acceptable gain on the vertical PNP transistor, was the information desired from the simulations. The thicknesses employed for the wafer experiments were determined from the simulation results.

The simulation experiments described in the preceding sections were repeated for the thinner epitaxial layers. The collector plug diffusion time was set at 10 minutes for 4.0 μm epitaxy, or 20 minutes for 5.0 μm epitaxy. The isolation time was varied in the simulations. Measurement of the remaining epitaxial layer from these simulations showed, for all cases, that there was not a sufficient N-type layer to form the base of the floating vertical PNP transistor. This is shown in Figure 25 for a 4.0 μm epitaxial layer

Similar problems were encountered with 5.0 μm an epitaxial layer. This was verified by including the NPN base diffusion and shown in Figure 26.

Figure 26 shows that the NPN base and buried P+ diffusion are shorted. Thus, based upon these results, the 4.0 μm and 5.0 μm epitaxial layer thicknesses were eliminated from further consideration.

Using a 6.5 μm epitaxial layer and including the NPN base diffusion it was determined that an adequate N-type region for the base of the floating vertical PNP transistor was formed. With a plug diffusion time of 50 minutes and an isolation time of

Figure 25. Insufficient N type Layer, 4.0 μm Epitaxial Layer

30 minutes, an N-type layer of approximately $1.0\text{ }\mu\text{m}$ remained. This appeared to be sufficient and the investigation using a $6.5\text{ }\mu\text{m}$ thick epitaxial layer continued. It was also decided to include a thicker epitaxial layer, $7.5\text{ }\mu\text{m}$ in the wafer experiments.

4.3.7 Subsequent Process Steps

Changes to the processing steps after collector were not required. They were assumed to be adequate to successfully fabricate working components. This assumption was supported by the simulation results.

4.3.8 Conclusions

Using diffusion process simulations, appropriate diffusion times for the phosphorus collector plug and boron isolation as a function of epitaxial thickness were determined. The simulations showed that the combined collector plug and isolation diffusion times had a large effect upon the up-diffusion of the buried boron P⁺ and, thus, the thickness of the N-type region which forms the base of the floating vertical PNP transistor. The simulations also showed that using epitaxial layer thicknesses less than $6.5\text{ }\mu\text{m}$ was not feasible and thicker layers should be evaluated.

This information was used to design and run an experiment using real wafers. The next section discusses this experiment.

4.4 Wafer Experiments

The simulation work provided us with significant information which aided in the

Figure 26. NPN base and Buried P Short, 5.0 μm Epitaxial Layer

design of the wafer run experiments. The most important result from this work was the discovery that thinning the epitaxial layer was not feasible. Also, it was determined that minor changes in the buried P+ dose did not significantly change the amount of up diffusion of the buried boron. The buried P+ up-diffusion was, however, significantly affected by the total diffusion time of the isolation and collector plug. Therefore, the isolation diffusion time was included as a variable in the experimental design.

The final experimental designs for processing the wafers through the fabrication area are shown in Table 5.

Epitaxial Thickness	Isolation Diffusion Time (1150 °C)		
	10 minutes	25 minutes	40 minutes
6.5 μM	10 minutes	25 minutes	40 minutes
7.5 μM	10 minutes	25 minutes	40 minutes

Table 5. Wafer Experimental Design

Detailed discussion of the results of the wafer experiments follows in Chapter 5.

Chapter 5. Experimental Results

This chapter discusses in depth the results of the wafer experiments. These experiments were successful in fabricating functional components. However, the BV_{ceo} of the floating vertical PNP transistor did not meet the minimum requirement of 12 volts. In addition, the gain of the floating vertical PNP transistor was higher than desired. This is likely caused by inadequate epitaxial layer thickness. Additional work required to attain the desired values for these parameters is discussed in Chapter 6.

5.1 Wafer Experimental Design and Results

5.1.1 Experimental Design

The success of the simulation work greatly simplified the wafer experiments that were processed in the production area. The simulation results were used to determine diffusion times, eliminate variables from the experiment, and retarget the thickness of the epitaxial layer. The wafer experiment was shown in Table 5 in Chapter 4. It is shown again in Table 6.

Epitaxial Thickness	Isolation Diffusion Time (1150 °C)		
	10 minutes	25 minutes	40 minutes
6.5 μM	10 minutes	25 minutes	40 minutes
7.5 μM	10 minutes	25 minutes	40 minutes

Table 6. Wafer Experimental Design

Although the simulation deck had been verified against historical process data, its results were never used to draw conclusions regarding actual processing. Therefore, a 7.5 μm epitaxial layer thickness was included to insure, should the results from the wafer

experiments be inadequate, that they would provide information for further experimentation.

Also, the isolation diffusion time was included as an experimental variable. The simulated boron buried P+ up-diffusion was greatly affected by the total diffusion time. It was expected that the gain and the collector to emitter breakdown voltage, PBV_{ceo} , of the floating vertical transistor would show strong dependence on the isolation diffusion time.

The experiment was run on two groups of wafers using different mask sets. The first group was processed using the 5126 mask set. It contains the vertical PNP transistor in the Process Control Module (PCM), but is not a 12 volt product. The second group was processed using the 5922 mask set. This set does not contain the vertical PNP transistor, but is a 12 volt product. Two experiments were run using the two mask sets. Data from the vertical PNP were obtained from the 5126 set and data regarding the 12 volt parametrics were obtained from the 5922 mask set. The products normally fabricated using these two mask sets have different design rule spacings, which affected the measured parameters. However, valid conclusions regarding the new process were drawn from the results on both mask sets.

5.1.2 Wafer Experimental Results

The electrical parameters of primary interest were discussed in Chapter 2. They are the isolation-epitaxy breakdown voltage, BV_{iso} ; the NPN collector (epitaxy)-NPN base breakdown voltage, BV_{cbo} ; the NPN emitter-NPN collector breakdown voltage,

BV_{ceo}; the MOS field threshold voltage, MOSV_t; the PNP emitter-PNP collector breakdown voltage, PBV_{ceo}; and the PNP transistor gain. The averages of these parameters from the wafer experiments are tabulated below in Table 7 for the 5922 mask set and in Table 8 for the 5126 mask set.

Epitaxial Thickness	6.5 μm			7.5 μm		
Isolation Diffusion Time	10 min	25 min	40 min	10 min	25 min	40 min
NPN BV _{iso} (V)	63.5	63.6	64.0	58.2	58.6	59.9
NPN BV _{cbo} (V)	43.8	44.0	42.9	41.0	41.0	41.4
NPN BV _{ceo} (V)	19.9	19.8	19.3	17.1	16.7	17.4
MOSV _t (V)	18.4	18.4	18.4	19.4	19.7	20.1

Table 7. Average Parametric Results for 5922 Mask Set

All parameters except those associated with the floating vertical PNP transistors are adequate for fabrication of the 12 volt products. The data in Table 8 shows that the vertical PNP parameters are very strongly affected by the epitaxial layer thickness. An epitaxial layer of 6.5 μm was found to be inadequate to fabricate this transistor. The BV_{ceo} of the floating vertical PNP transistor on these wafers was less than 1 volt, indicating insufficient spacing between the PNP emitter and collector. An epitaxial layer of 7.5 μm increased the BV_{ceo} to about 10 volts, but is still not sufficient to sustain the breakdown voltage above 12 volts.

Figure 27 and Figure 28 show the current-voltage characteristics of the floating vertical transistor fabricated with 6.5 μm and 7.5 μm epitaxial layers.

Epitaxial Thickness	6.5 μm			7.5 μm		
Isolation Diffusion Time	10 min	25 min	40 min	10 min	25 min	40 min
NPN BV _{iso} (V)	35.6	44.8	26.0	48.2	45.6	47.1
NPN BV _{cbo} (V)	45.2	44.3	30.6	45.4	43.0	43.8
NPN BV _{ceo} (V)	17.9	18.4	19.4	19.2	17.9	17.8
MOSV _t (V)	16.2	17.3	14.6	16.9	17.0	16.6
PNP BV _{ceo} (V)	0.8	0.7	0.0	9.6	10.2	12.6
PNP Gain	--	--	--	140	150	145

Table 8. Average Parametric Results for 5126 Mask Set

Figure 27. Floating PNP Characteristics with 6.5 μm Epitaxy.

Further experimentation with thicker epitaxial layers is required to obtain the desired floating vertical PNP transistor characteristics. The final epitaxial thickness will also determine the isolation diffusion time required and the resulting lateral diffusion. This will determine if and by how much we can shrink the component spacings on the 12 volt

products.

Figure 28. Floating PNP Characteristics with 7.5 μm Epitaxy.

The isolation diffusion time did not significantly affect the floating vertical PNP transistor. This is shown in Figure 29. Increasing the isolation diffusion time increases the amount of buried boron up-diffusion. Therefore, the expectation was that the floating vertical PNP transistor gain would increase and the collector to emitter breakdown voltage, PBV_{ceo} , would decrease. Neither of these parameters show the expected effects due to the changes in the isolation diffusion time.

Variation of the NPN parameters and $MOSV_t$ between groups can be attributed to differences in the epitaxial layer resistivity. The change from arsenic to antimony buried layer made the resistivity targeting more difficult. Epitaxial layer resistivity has a strong impact on the breakdown voltages and field threshold. In addition, the design spacings on the two mask sets are different. This also affected these parameters significantly.

Figure 29. VPNP Transistor PBV_{ceo} versus Isolation diffusion time, 7.5 μ m Epitaxy.

5.2 Summary

The simulation and development work of this thesis has shown the feasibility of using the up-down isolation process for the 12 volt product line manufactured at Philips Semiconductors in Sunnyvale. Except for the floating vertical PNP transistor, all of the important parametrics were sufficient to support the expected operating voltages of these devices. Chapter 6 discusses the work necessary to continue the development of the new 12 volt process.

Chapter 6. Conclusions and Future Work

This chapter further discusses the conclusions of this thesis and proposes future work to bring the up-down isolation process into production and replace the existing 12 volt process. It was shown that the up-down isolation scheme is an alternative to the existing process for the 12 volt product line. However, fabrication of the floating vertical PNP transistor was unsuccessful. It requires an epitaxial layer greater than 7.5 μm thick. Reduction in the lateral diffusion of the isolation boron is possible, but is less than the originally hoped for 50 %; it depends upon the final epitaxial layer thickness.

6.1 Floating Vertical PNP Transistor

The failure of the vertical PNP transistor to sustain the required voltage has been attributed to an insufficient epitaxial layer thickness. The epitaxial layer must be greater than 7.5 μm to enable the vertical PNP transistor to function under the expected conditions. The anticipated final epitaxial layer thickness is in the range of 8.0 μm to 9.0 μm . The simulation deck developed during the course of the thesis work will be used to do preliminary evaluation of thicker epitaxy and determine the required collector plug and isolation diffusion times.

Reduction of the buried boron up-diffusion may also be beneficial to targeting the floating vertical PNP transistor gain and collector to emitter breakdown voltage. This can be achieved by reducing the amount of boron beneath the epitaxial layer. During the initial stages of the simulation work the boron implant dose at this step was varied by $\pm 15\%$. We observed practically no change in the measured up-diffusion as a function of

these changes. Further simulation work with greater reduction in the implant dose, possibly up to an order of magnitude, will help in determining how feasible this approach is. Reduction of the implant dose will increase the resistivity of the floating vertical PNP collector. This reduces the current carrying capability of the transistor and may not be an acceptable approach.

6.2 Isolation Boron Lateral Diffusion

Significant reduction of the lateral diffusion of the isolation is also attainable with the up-down isolation process. The requirement of a thicker epitaxial layer to fabricate an adequate vertical PNP transistor make the potential reduction somewhat less than 50% that was initially stated as the goal. Likely, this reduction will be in the 30% to 40% range. It is dependent upon the final epitaxial layer thickness based upon the vertical PNP transistor requirements. It is also dependent upon the isolation diffusion time, and the collector plug diffusion time. These times can be readily determined for the thicker epitaxial layer using the simulation deck that was developed for this thesis work. The reduction in the design rule spacings is dependent upon how much the isolation lateral diffusion is reduced.

6.3 Summary

The successful development of the up-down isolation process depends upon further simulation and development to determine the proper epitaxial layer thickness. This is necessary to insure that the BV_{ceo} of the vertical PNP is higher than approximately 15 volts. Determination of sufficient diffusion time to isolate the active regions will

determine the amount of lateral boron isolation diffusion. The reduction in component spacing depends upon the amount of lateral diffusion. The results of this future work will determine whether the development of the new 12 volt process continues into production. The simulation deck developed for this thesis will be of great benefit in completing this work. The final results of the up-down isolation development, the cost of retooling old masks for 1.0 μm alignment tolerances, and the cost of adding the oxide/nitride capacitor must all be considered.

Appendix. SSUPREM4 Simulation Deck

Initialization

#Grid Definition

line x loc=0.00 spac=0.50
line x loc=10.00 spac=0.50

line y loc=0.00 spac=0.05
line y loc=0.50 spac=0.05
line y loc=10.00 spac=0.20

#Substrate Definition

init silicon boron resistivity=12 orientation=111

Initial Oxidation

#Initial Oxidation

diffus time=50 temp=800 t.final=1150 dryo2 press=1 hcl%=0
diffus time=186 temp=1150 weto2 press=1 hcl%=0
diffus time=60 temp=1150 t.final=800 dryo2 press=1 hcl%=0

Buried Sb N+ Layer

#BN Implant - Buried Antimony

implant antimony dose=4.0e15 energy=80 pearson tilt=0 rotation=0

#BN Sb Diffusion

method fermi compress
diffus time=60 temp=800 t.final=1070 nitro press=1.00
diffus time=35 temp=1070 t.final=1250 dryo2 press=0.25 hcl%=0
diffus time=190 temp=1250 dryo2 press=0.25 hcl%=0
diffus time=76 temp=1250 t.final=800 dryo2 press=0.25 hcl%=0

Buried P+ Implant and Diffusion

#BP Implant - Buried Boron

implant boron dose=2.0e14 energy=100 pearson tilt=0 rotation=0

#BP Boron Diffusion

method fermi compress
diffus time=12 temp=800 t.final=900 f.hcl=0.03 f.n2=7.0 f.o2=4.5 press=1.0
diffus time=10 temp=900 f.hcl=0.03 f.n2=7.0 f.o2=4.5 press=1.0
diffus time=50 temp=900 f.n2=7.0 f.o2=4.5 press=1.0
diffus time=5 temp=900 f.n2=7.0 press=1.0
diffus time=28 temp=900 t.final=1135 f.n2=7.0 press=1.0
diffus time=22 temp=1135 f.n2=7.0 f.o2=2.2 press=1.0
diffus time=10 temp=1135 f.h2=7.1 f.hcl=0.03 f.n2=0.6 f.o2=3.8 press=1.0
diffus time=60 temp=1135 t.final=800 f.n2=7.0 press=1.0

Epitaxial Growth

#Epitaxial Growth

epitaxy time=6.5 temp=1080 thickness=6.5 divisions=100 press=1.00 \ c.arsenic=4.0e15

Reoxidation

#Change As segregation coefficient from 30.0 to 1.0

impurity i.arsenic silicon /oxide seg.0=1.0

#Epitaxial Oxidation

method fermi compress

diffus time=50 temp=800 t.final=1150 f.n2=3.0 f.o2=0.3 press=1.00

diffus time=5 temp=1150 f.hcl=0.02 f.n2=4.0 f.o2=1.6 press=1.00

diffus time=5 temp=1150 f.n2=4.5 f.o2=3.8 press=1.00

diffus time=59 temp=1150 f.h2=7.1 f.o2=3.8 press=1.00

diffus time=60 temp=1150 t.final=800 f.n2=3.0 f.o2=0.3 press=1.00

Isolation Diffusion

#Change boron in silicon diffusion constants from 0.037 to 0.1, from 0.72 to 1.2

impurity i.boron silicon dix.0=0.1 dip.0=1.2

#Iso Diffusion

method fermi compress

diffus time=40 temp=800 t.final=1220 f.n2=4.5 f.o2=0.001 press=1.00 \

c.boron=1.0e23

diffus time=30 temp=1220 f.n2=4.5 f.o2=0.001 press=1.00 c.boron=1.0e23

diffus time=75 temp=1220 t.final=800 f.n2=4.5 f.o2=.001 press=1.00 \

c.boron=1.0e23

Plug Deposition

#Change phos in oxide diffusion coef from 7.6e-3 to 7.6e-2

impurity i.phosphor oxide dix.0=7.6e-2

#Change phos in Si diffusion coefs from 3.85 to 10, from 4.44 to 10, from 44.2 to 50.0

impurity i.phosphor silicon dix.0=10.0 dim.0=10.0 dimm.0=50.0

#Plug deposition

method fermi compress

diffus time=20 temp=800 t.final=930 f.n2=7.0 f.o2=0.2 press=1.00

diffus time=10 temp=930 f.n2=7.0 f.o2=0.2 press=1.00

diffus time=58 temp=930 f.n2=7.0 f.o2=0.4 press=1.00 c.phosphor=1.0e23

diffus time=17 temp=930 f.n2=7.0 f.o2=4.0 press=1.00 c.phosphor=1.0e23

diffus time=20 temp=930 t.final=800 f.n2=7.0 f.o2=0.3 press=1.00 \

c.phosphor=1.0e23

#Clean 13 Remove phos doped oxide

etch oxide all

Plug Diffusion

#Change phos in oxide diffusion coef from 7.6e-2 to 7.6e-3
impurity i.phosphor oxide dix.0=7.6e-3

#Plug diffusion
method fermi compress
diffus time=50 temp=800 t.final=1150 f.hcl=0.3 f.n2=4.5 f.o2=2.0 press=1.00
diffus time=50 temp=1150 f.o2=2.0 press=1.00
diffus time=6 temp=1150 f.h2=3.0 f.o2=2.0 press=1.00
diffus time=60 temp=1150 t.final=800 f.n2=4.5 f.o2=2.0 press=1.00

Base Deposition

#Change boron in silicon diffusion constants from 0.037 to 0.1, from 0.72 to 1.2
impurity i.boron silicon dix.0=0.1 dip.0=1.2

#Change boron in oxide diffusion constant from 3.16e-4 to 1.5e-2
impurity i.boron oxide dix.0=1.5e-2

#Base Deposition
method fermi compress
diffus time=15 temp=800 t.final=935 f.n2=4.0 f.o2=4.0 press=1.00 \
c.boron=1.0e23
diffus time=30 temp=935 f.n2=4.0 f.o2=4.0 press=1.00 c.boron=1.0e23
diffus time=30 temp=935 t.final=800 f.n2=8.0 press=1.00 c.boron=1.0e23

Base Diffusion

Base Diffusion
method fermi compress
diffus time=30 temp=800 t.final=1050 f.n2=4.0 f.o2=4.0 press=1.00
diffus time=54 temp=1050 f.n2=1.8 f.o2=2.2 press=1.00
diffus time=34 temp=1050 f.h2=3.7 f.o2=2.0 press=1.00
diffus time=60 temp=1050 t.final=800 f.n2=4.5 press=1.00

#Emitter Diffusion
method fermi compress
diffus time=20 temp=800 t.final=930 f.n2=7.0 f.o2=0.2 press=1.00
diffus time=10 temp=930 f.n2=7.0 f.o2=0.2 press=1.00
diffus time=30 temp=930 f.n2=5.0 f.o2=2.0 press=1.00
diffus time=40 temp=930 t.final=800 f.n2=7.0 f.o2=0.2 press=1.00

#Emitter Oxidation
diffus time=10 temp=800 t.final=850 f.n2=4.0 press=1.00
diffus time=5 temp=850 f.n2=4.0 press=1.00
diffus time=15 temp=850 f.h2=4.8 f.o2=3.0 press=1.00
diffus time=30 temp=850 f.n2=4.0 press=1.00
diffus time=10 temp=850 t.final=800 f.n2=4.0 press=1.00

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