2001

Design of a 0Hz to 1200Hz Variable frequency drive with space vector control

Jacob Roberts Bemrich
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**DESIGN OF A 0Hz TO 1200Hz VARIABLE FREQUENCY DRIVE
WITH
SPACE VECTOR CONTROL**

A Thesis

Presented to

**The Faculty of the Department of Electrical Engineering
San Jose State University**

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Jacob Roberts Bemrich

August, 2001

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ABSTRACT

DESIGN OF A 0Hz TO 1200Hz VARIABLE FREQUENCY DRIVE

WITH

SPACE VECTOR CONTROL

Jacob Roberts Bemrich

An open loop, 0Hz to 1200Hz, 3-phase, AC Variable Frequency Drive (VFD) has been developed to be used for multi-pole permanent magnet AC motors and AC induction motors used in electric vehicles or aerospace applications. A market review for such a VFD concludes that “off-the-shelf” variable frequency drives that fit this description and operate with a DC input are unavailable. A space vector generated PWM signal controls the switches of a DC-AC inverter to deliver the 3-phase electrical energy to the stator windings of a motor using the constant V/Hz principle to calculate the reference space vector voltage. The space vector generated PWM produces lower harmonics when compared to the direct sinusoidal PWM and provides a 15% increase in the phase-to-phase voltage. This design was proven to generate 3-phase output voltages producing sinusoidal currents from 0Hz to 1200Hz through the windings of a 3-phase motor.

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LIST OF VARIABLES

Variable		Units
ϕ_{ag}	Air gap flux	Wb
ω_r	Rotor speed	Rad/sec
ω_s	Synchronous speed	Rad/sec
ω_{sl}	Angular slip speed	Rad/sec
B_{ag}	Flux density distribution	T
E_{ag}	Air gap voltage produced by air gap flux	V
f	Frequency	Hz
f_{sl}	Slip speed	Hz
I_m	Magnetizing currents	A
I_r	Rotor inductance	H
I_s	Stator current	A
L_{lr}	Rotor leakage resistance	H
L_{ls}	Stator leakage inductance	H
L_m	Magnetizing inductance	H
R_r	Rotor resistance	Ω
R_s	Stator resistance	Ω
T_{em}	Electro-mechanical torque	N-m
U_s	Space vector for state s.	V
$U_{sd} \ U_{sq}$	Components of U_s in the d-q plane	V
$V_a \ V_b \ V_c$	Three phase voltage outputs	V

Variable		Units
V_{an} V_{bn} V_{cn}	Voltage across the 3-phase windings of the stator delivered by the DC-AC inverter with reference to the neutral, n .	V
V_{dc}	DC bus voltage	V
V_s	Generic variable for the voltage across the stator	V

LIST OF ACRONYMS

Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
BLDC	Brushless DC (motor)
CPU	Central Processing Unit
CSI	Current Source Inverter
DAC	Digital-to-Analog Converter
DC	Direct Current
DSP	Digital Signal Processor
EMI	Electro-Magnetic Interference
FOC	Field Oriented Control
HP	Horse Power
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
ISR	Interrupt Service Routine
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

Acronyms

PMAC	Permanent Magnet AC (motor)
PROM	Programmable Read Only Memory
PWM	Pulse-Width Modulation
QEP	Quadrature Encoder Pulse
RAM	Random Access Memory
SCR	Silicon Controlled Rectifier
SVPWM	Space Vector PWM
V/Hz	Constant Volts/Frequency
VFD	Variable Frequency Drive
VSI	Voltage Source Inverter
VVI	Variable Voltage Input

CHAPTER 1: INTRODUCTION

Variable frequency drives (VFD) are widely used to adjust the speed of AC induction motors as well as AC synchronous motors. They are used in motor applications such as heating, ventilation, and air conditioning, as well as in more complicated applications such as pump control and robotics. A survey of variable frequency drives concludes there are no “off-the-shelf”, 3-phase variable drives that generate an output from 0Hz to 1200Hz with a DC voltage input. Table 1-1 contains a brief list of variable frequency drives that are available. The column labeled “Control” refers to two types of control methods. The V/Hz control type maintains a constant air gap flux in the motor by maintaining the ratio of the stator voltage to frequency constant. The vector control type is much more complicated and requires a model for the specific motor under control. For more information, see Table A-3 in Appendix A that contains a list of websites for commercial variable frequency drives.

Table 1-1: VFD Market Survey.

Manufacturer	Output			Input
	Control	HP	Frequency (Hz)	Voltage
AC Technology	V/Hz	3	0 - 99	240 VAC
Acumentrics	Vector	3	0 - 700	300 VDC
Baldor	Vector	3	0 - 120	240 VAC
Danfoss	V/Hz	3	28 - 90	240 VAC
Cleveland Motion	Vector	5	0 - 480	240 VAC
Warner Electric	V/Hz	1	6 - 120	230 VAC
IMD	V/Hz	10	10 - 90	240 VAC

The objective of this research is to design a variable frequency drive that (1) provides 3-phase voltages to generate sinusoidal currents through the windings of an AC

induction or permanent magnet AC motor, (2) adjusts the output frequency from 0Hz to 1200Hz, and (3) maintains a constant current throughout the adjustable output frequency. The operator controls the output frequency. This VFD could be used in electric vehicles or other applications where the motor has a high pole-count. The increased pole-count provides better torque but decreases the speed of the motor. This VFD can operate at a high frequency allowing for an increase in speed.

Figure 1-1 is a simplified diagram of this VFD design. The desired output frequency is set by the operator and read by the digital signal processor (DSP) based controller. The DSP based controller adjusts the sequence of the switches on the DC-AC inverter to transform the DC bus voltage into 3-phase, pulse-width modulated voltages to be delivered to a 3-phase motor for a desired frequency. For this design, the 3-phase motor will be an AC induction or permanent magnet AC motor. There is neither position nor speed feedback from the motor to the DSP controller. This design operates in open-loop mode only.

Figure 1-1: Descriptive Diagram of Variable Frequency Drive

The DC-AC inverter is rated for 600 VDC and 100A. The inverter is an Intelligent Power Module (IPM), [PM100CVA060, Powerex Inc., Youngwood, PA] that uses Insulated Gate Bipolar Transistors (IGBT) and incorporates circuitry to protect the transistors from short-circuit, over-temperature, and under-voltage. The DSP controller interfaces with the IPM through opto-isolators to isolate the high power switching devices from the digital signals. The DSP controller is an evaluation module for the TMS320F240 DSP from Texas Instruments [TMDS3P603070, Texas Instruments, Dallas, TX].

The remainder of this thesis is divided into four chapters. Chapter 2: Design Background, explains the theory and technology used to develop this variable frequency drive. The design background chapter includes (1) AC motor theory, both AC induction motors and permanent magnet AC motors, to explain how the speed can be adjusted using a VFD, (2) variable frequency drive technologies, from inefficient mechanical methods to direct control of the AC motor using solid-state devices, (3) DC-AC inverters, to show how they deliver 3-phase power to the motor, and (4) pulse-width modulation (PWM) techniques used to control the energy delivered to the load by the DC-AC inverter. The space vector generated PWM (SVPWM) will be discussed in detail and is used to create the modulation signal in this design.

Following the theoretical background, Chapter 3: Design Implementation analyzes the hardware and software design used to realize the 0Hz to 1200Hz variable frequency drive.

Chapter 4: Experimental Results proves that the variable frequency drive design produces 3-phase voltages generating sinusoidal currents, which are adjustable from 0Hz to 1200Hz and provides a constant current to the windings of the motor throughout the frequency range.

Finally, Chapter 5: Conclusion summarizes the results, reviews the lessons learned, and suggests ideas for future work.

CHAPTER 2: DESIGN BACKGROUND

This chapter of the thesis provides background into the theory and technology used to implement this design. In order to understand variable frequency drives, a brief overview of AC induction motors and permanent magnet AC motors is given. The constant volts/frequency technique will be presented as a viable method to adjust the speed of an AC motor, maintain a constant current, and achieve electromagnetic torque that is independent of the supply frequency. In addition, a synopsis of VFD technologies is presented, touching on DC-AC inverters and pulse-width modulation techniques, specifically the space vector PWM.

AC INDUCTION MOTOR OVERVIEW

AC induction motors convert electrical energy into rotational mechanical energy. Time varying electrical energy produces a time varying magnetic field through the windings of the stator (stationary part) of the motor. The rotor (rotating part) of the motor is magnetically linked to the stator much as a transformer's secondary windings are linked to the primary windings. The magnetic link induces electrical energy through the rotor producing its own magnetic field.

In a 3-phase induction motor, three stator windings are evenly spaced 120° around the rotor. Three balanced sinusoidal voltages, 120° out of phase with one another, excite the three stator windings that produce sinusoidal currents in the stator, thus creating a rotating magnetic field. This rotating magnetic field in the stator induces a current through the rotor, producing a magnetic field in the rotor as well and causing it to rotate in the same direction as the magnetic field. This interaction produces electromagnetic

torque. The amount of magnetic flux that can be produced in the air gap between the stator and the rotor depends on the amount of electrical current delivered. The design of the motor dictates the amount of electrical current that the motor can withstand.

The following mathematical overview of AC induction motors is summarized by Mohan et al (Mohan, Undeland, and Robbins 1995, 400-413). When balanced three-phase sinusoidal voltages are applied to the stator V_s at frequency f a balanced set of currents is produced. These currents I_m create a flux density distribution B_{ag} in the air gap. The flux density has constant amplitude and rotates with constant speed. This speed is called the synchronous speed ω_s . Applying a frequency f to a p -pole motor, the synchronous speed (Mohan, Undeland, and Robbins 1995, 401) is

$$\omega_s = \frac{2}{p} \times 2\pi f . \quad (2-1)$$

Due to the air gap flux density distribution B_{ag} , the air gap flux ϕ_{ag} rotates the rotor with respect to the stator windings at the synchronous speed. The air gap flux produces E_{ag} , which is the counter-emf (electro-motive force), called the air gap voltage. E_{ag} depends on the frequency f of the voltage delivered to the winding of the stator. Its relationship to the air gap flux is

$$E_{ag} \cong k_1 f \phi_{ag} , \quad (2-2)$$

where k_1 is some constant (Mohan, Undeland, and Robbins 1995, 401). An equivalent circuit of one phase of the 3-phase AC induction motor is shown in Figure 2-1. V_s is the stator voltage, I_s is the current through the stator, R_s is the stator resistance, and L_{ls} is the leakage inductance in the stator. I_r is the current through the rotor, R_r is the rotor

resistance, L_{lr} is the leakage inductance in the rotor, and $R_r (f-f_{sl})/f_{sl}$ is the rotor resistance due to slip speed. I_m and L_m are the magnetizing current and inductance, respectively.

Figure 2-1: Equivalent circuit of a single phase of a 3-phase AC induction motor (Mohan, Undeland, and Robbins 1995, 401).

Other than at low frequencies the stator resistance R_s can be neglected and $\bar{E}_{ag}$ is approximately V_s , which is the per-phase voltage applied to the winding of the stator resulting in

$$V_s \cong f\phi_{ag} . \quad (2-3)$$

The air gap flux and the currents through the rotor produce the torque in an AC induction motor. When the rotor is rotating at the synchronous speed, there is neither induced rotor voltage, rotor current, nor torque. When the rotor is rotating at any other speed in the same direction as the air gap flux rotation at ω_s , the motor is “slipping” relative to the air gap flux. This is called the slip speed, ω_{sl} . Slip speed is $\omega_s - \omega_r$. The electromechanical torque T_{em} is

$$T_{em} \cong \phi_{ag}^2 f_{sl}, \quad f_{sl} = \omega_{sl} / 2\pi , \quad (2-4)$$

where the torque is heavily dependent on the air gap flux (Mohan, Undeland, and Robbins 1995, 403-404). Maintaining a constant air gap flux is important for

maintaining the torque even when supply frequency changes. The constant volts/frequency (V/Hz) principle can be used to maintain a constant air gap flux. It will be discussed later on page 9.

Permanent magnet AC (PMAC) motors offer a more efficient alternative. Since this variable frequency drive design is to be used in an electric vehicle or aerospace application where the supply of power is limited and efficiency is a necessity, PMAC motors must be discussed.

PERMANENT MAGNET AC MOTOR OVERVIEW

Synchronous permanent magnet AC motors are very similar to AC induction motors. Both require the stator to produce a magnetic field and both rotate in the same direction as the rotating magnetic field. PMAC motors use permanent magnets to produce the air gap magnetic field instead of relying on a magnetizing component of stator current like the AC induction motor (Slemon, 1994). Permanent magnet AC motors are more efficient, less complicated in construction, and have fewer losses than the traditional AC induction motor (Slemon, 1994). Figure 2-2 is the equivalent circuit for one leg of the 3-phase PMAC motor.

Figure 2-2: Permanent Magnet AC motor equivalent circuit (Slemon, 1994).

The PMAC motor can generate continuous torque only when the speed of the motor is directly related to the supply frequency (Slemon 1994). Unlike the AC induction motor, the torque produced by the motor is not a function of the slip speed, but rather a function of the angle with which the peak field of the stator leads the rotor (Slemon, 1994). The torque is derived as

$$T_{em} = \frac{3p}{2} L_m I_f I_s \sin \beta , \quad (2-5)$$

where p is the number of motor poles and L_m is the magnetizing inductance. When the rotor rotates at an angular speed ω_r , the effect of the rotor as seen by the stator can be represented by a sinusoidal current source I_f with an angular frequency of $\omega_f = (p/2) \omega_r$ (Slemon, 1994). I_s is the current through the stator, and β is the electrical angle at which the peak of the stator field leads the rotor magnet axis (Slemon, 1994). Notice that according to equation (2-5), if the stator current leads the rotor field by 90° , then the maximum torque is realized. Equation (2-5) also shows that by maintaining a constant current through the stator, the torque can remain constant throughout the adjustable frequency range of the variable frequency drive. Again, the constant V/Hz principle can be used to maintain the magnetic flux created by the stator by maintaining the current through the windings of the stator.

CONSTANT VOLTS/FREQUENCY PRINCIPLE

The constant volts/frequency (V/Hz) principle is used to maintain constant flux in the stator of the motor. By maintaining constant flux in the stator, the torque of the motor becomes independent of the supply frequency, assuming the voltage applied to the stator

is sinusoidal and the voltage drop across the stator resistor is neglected (Yu and Figoli 1998). From equation (2-3), the stator air gap flux can be represented as

$$\phi_{ag} \cong \frac{V_s}{f}, \quad (2-6)$$

showing that to maintain constant flux in the stator, the ratio of stator voltage to stator excitation frequency (i.e., supply frequency) must remain constant. When the constant V/Hz principle is implemented, the ratio of the stator voltage V_s to frequency f depends on the motor ratings. When the frequency is low and likewise the voltage to the motor windings is low, the stator resistor's voltage drop cannot be neglected and must be compensated. At frequencies higher than the rated value, the voltage remains constant to avoid insulation breakdown (Yu and Figoli 1998). Figure 2-3 shows this relationship. The flat part of the curve in Figure 2-3 represents a voltage “boost” that must be used to overcome the stator resistance at low frequencies.

Figure 2-3: Voltage versus frequency using V/Hz principle with a minimum voltage “boost” at low frequencies to overcome the voltage drop across the stator resistance (Yu and Figoli 1998).

VARIABLE FREQUENCY DRIVES

The objective of this section is to provide an overview of different types of variable frequency drives with emphasis on the pulse-width modulated AC variable frequency drive.

TYPES OF VARIABLE FREQUENCY DRIVES

Varying the speed and torque of a motor drive is nothing new to industry. Since the late 1800s, the AC induction motor has been used to perform many tasks in industry. Many techniques have been developed to adjust for varying torque and speed requirements. The techniques used to perform this task have moved from mechanical interventions to the use of semiconductors to directly change the speed of the AC induction motor.

Mechanical interventions such as the low efficiency “Reeves” drive keep the motor at a constant speed while the output shaft contributes to the change in the drive speed. This drive uses a variable pitch V-belt that attaches to adjustable flanges on the drive shaft. As the flanges move, the belt appears to be rotating on different pulley diameters. The speed range is only about 4 to 1 (Phipps 1994).

A hydraulic drive system, which includes a motor-driven pump, a hydraulic motor, reservoir, and control valves, can apply large amounts of torque with a wide speed range. However, hydraulic drives have low efficiencies due to the motor-driven pump running at full speed 100% of the time. They also present maintenance, control, and environmental issues due to the piping and fluids (Phipps 1994).

Another adjustable drive uses eddy-current coupling. This device permits slip from the motor to the drive shaft. The “stiffness” of the coupling depends on the DC excitation level on the coupling’s winding. Again, the motor is running at full speed 100% of the time. This technique should be considered a torque controller because when the load is removed, the speed of the drive increases. Although this drive has good starting characteristics and absorbs shock loads well, the efficiency is low and many of these drives require some type of liquid cooling (Phipps 1994).

The rotating DC drive is a prevalent and more efficient variable speed drive. It uses regeneration when it encounters an over-hauling load. This means the energy recycles back into the power system, a form of energy conservation. However, they require significant amounts of floor space and since DC machines have brushes, they can create sparks and must therefore be isolated from explosive environments (Phipps 1994).

The transistors, silicon controlled rectifiers (SCR), and operational amplifiers that were developed in the early 1960s elevated variable frequency drives to an entirely new level. The solid-state VFD was born. The solid state VFD had many advantages. The friction and winding losses from the generator were eliminated. The efficiency of the VFD was increased significantly due to reduced heat loss through the solid-state device, compared to that produced by other generation equipment. In addition, the control circuitry operated with less power (Phipps 1994).

The advantages of the solid-state VFD are as follows: zero speed starting, direct drive from the motor, and increased efficiency. This new technology was used to control the speed and torque of DC motors in the 1960s. With the advancement of power

semiconductors and fast microprocessors, the 1980s became the era of AC induction motor control (Phipps 1994). An overview of the AC variable frequency drives follows.

AC VARIABLE FREQUENCY DRIVE

The traditional AC variable frequency drive converts AC to DC and then inverts DC to AC, using a variety of switching methods, (See Figure 2-4). The AC output then has a controllable frequency and voltage. An AC variable frequency drive is often called an inverter. The three most common inverter designs are current source inverter, variable voltage inverter, and pulse-width modulated inverter (Phipps 1994). A comparison of the three types will develop an understanding of the reasons for choosing the PWM inverter for this design.

Figure 2-4: Typical VFD diagram. AC is converted into DC through a converter then the DC is inverted into a variable frequency and voltage AC output.

Current Source Inverter (CSI)

The CSI system converts the AC into a variable DC bus voltage, traditionally, using silicon-controlled rectifiers. The bus voltage is controlled to maintain the proper volts to frequency ratio (V/Hz), which ensures the motor air gap flux is constant throughout the frequency range. As with the converter side, silicon-controlled rectifiers are also used in the inverter section to control the output frequency (Phipps 1994).

The CSI system is inherently regenerative to the power line without any additional hardware. There are a few drawbacks to this system. This system must be tested with a load, motors must be matched to the system, and at low frequencies, the currents are delivered in pulses. This is called “cogging” and it is demanding on mechanical hardware. The CSI system has a power factor that varies with frequency, and can be as low as 70% at 30Hz (Phipps 1994). In addition, the SCRs create troublesome harmonics. These harmonics are currents or voltages with frequencies that are integer multiples of the fundamental output power frequency and can interfere with computers and other sensitive equipment. SCRs have been found to have predominant 5th, 7th, and 11th harmonics. If the output frequency of the CSI system is 10Hz, the 5th, 7th, and 11th harmonics are at 50Hz, 70Hz, and 110Hz, respectively (Phipps 1994).

Variable Voltage Input (VVI)

Much like the CSI system, the VVI system has a variable DC bus. Instead of regulating the current, the VVI system regulates the voltage to the motor. The VVI system does not have to be matched to any one motor as long as the motor is within the current rating of the inverter and it operates at higher frequencies up to 200Hz. Despite these advantages, the VVI system does share the same harmonic, power factor, and cogging problems as the CSI system (Phipps 1994).

Pulse-Width Modulation Inverter

Pulse-width modulation is a series of pulses that have a fixed frequency and magnitude, but a variable pulse width. The pulse-width modulation system is different from the CSI and the VVI systems because it uses diodes to convert the AC to DC and

produces a constant DC bus voltage. Large capacitors are used to maintain the bus voltage, contributing to the 3 to 5Hz ride-through capability (Phipps 1994). Ride-through capabilities allow the input power to be reduced or removed for a short time with little or no effect on the performance.

There are many other advantages to PWM systems. The power factor is constant at all speeds and can be higher than 95% depending on the design (Phipps 1994). The PWM system is a soft start system, meaning there is no wear on the components due to cogging when the motor is started. The diodes in the AC to DC converter section prevent some of the harmonics from getting back onto the main AC line, meaning the PWM system has little harmonic interference, relative to the CSI and VVI systems (Phipps 1994).

Table 2-1 shows a comparison of the different types of variable frequency drives. A “+” indicates a good rating for a specific parameter and “+ +” indicates an excellent rating. Likewise, a “-“ indicates a poor rating and “- -“ indicates a very poor rating.

Table 2-1: Comparison of Variable Frequency Drives (Mohan, Undeland, and Robbins 1995, 428). Note, the reference refers to the VVI type drive as the Square Wave VSI.

Parameter	PWM	VVI	CSI
Input power factor	+	-	--
Torque pulsations	++	-	-
Multi-motor capabilities	+	+	-
Regeneration	-	-	++
Short-circuit protection	-	-	++
Open-circuit protection	+	+	-
Ability to handle undersized motor	+	+	-
Ability to handle oversized motor	-	-	-
Efficiency at low speeds	-	+	+
Size and weight	+	+	--
Ride-through capability	+	-	-

DC-AC INVERTERS

It is understandable that the DC-AC inverter could be considered the muscle and force behind the PWM variable frequency drive. It can be made of different types of transistors; the most popular are the MOSFET (Metal Oxide Semiconductor Field Effect Transistors), and the IGBT (Insulated-Gate Bipolar-junction Transistors).

This section will provide background on three power semiconductors. The bipolar, MOSFET, and IGBT power devices will be presented. In addition, an IGBT DC-AC inverter will be used to demonstrate the delivery of electrical energy to the motor.

POWER SEMICONDUCTORS FOR DC-AC INVERTERS

Power semiconductor devices have had the greatest impact on the performance of AC variable frequency drives. Device performance determines the size, weight, and cost of the system. The device must withstand very large voltages when the device is off, tolerate very large currents with a low voltage drop across the device when it is on, and switch between the on and off states very rapidly. None of the following devices exhibit the ideal switching characteristics. There are always tradeoffs between switching speed and power capabilities.

Bipolar Power Devices

The first power bipolar transistors and thyristors were commercially available in the 1950s. With such a high demand for these devices, their ratings have steadily improved, due to advances in the manufacturing process. Consequently, a single thyristor is capable of blocking 6500V and 1000A (Baliga 1994).

Although these devices have been used extensively in power electronic applications, they require large currents to control them. This means the control circuitry needed would be large and bulky, adding to the overall system size and weight. This problem has propelled the development of power semiconductors that require less current and can be driven from integrated circuits (Baliga 1994). Hence, the power MOSFET was developed.

Power MOSFET

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is based on the technology used to create CMOS logic circuits. It exhibits much faster switching characteristics and requires a voltage to turn it on, rather than a current (Baliga 1994). Only during the transition from on to off does a small amount of current flow (Mohan, Undeland, and Robbins 1995, 25). The blocking voltage can become quite large. The drawback to the power MOSFET is the high voltage drop across the transistor (Baliga 1994). The voltage drop is proportionate to the bus voltage per the device rating. This is not acceptable for high-voltage variable frequency drives.

IGBT

The Insulated Gate Bipolar Transistor (IGBT) incorporates the low voltage control characteristics of the MOSFET and the superior on-state attributes of the bipolar. Developed in the 1980's, the IGBT incorporates a MOS-gate region to control the current in a wide-base high-voltage bipolar transistor. This is how the IGBT obtained the control properties of the MOSFET with the on-state features of the bipolar (Baliga 1994).

IGBT DC-AC INVERTER

The IGBT DC-AC inverter was used for this VFD design because of its power capabilities and switching frequencies. This section will explain how the IGBT inverter produces the 3-phase voltages, using switching patterns.

A simplified schematic of an IGBT DC-AC inverter is shown in Figure 2-5. This design incorporates a split DC bus voltage. The junction of the split bus n' can be used as a neutral when the motor design allows access to the neutral of the motor. The 3-phase outputs (V_a , V_b , V_c) are applied to the stator windings of the 3-phase motor, producing the currents (I_{sa} , I_{sb} , I_{sc}) through the stator. By turning on these transistors in a certain sequence, a sinusoidal waveform is generated. At no time should transistor a and a' be on at the same time. This applies to the b and b' switches as well as the c and c' switches. When complementary switches are on at the same time, the bus voltage is shorted. This is called shoot-through. To prevent shoot-through, dead-band is incorporated. Dead-band is the time between one switch turning off and the complementary switch turning on. Dead-band ensures that no complementary switches are on simultaneously.

Knowing that only three switches can be on at the same time, there are 2^3 switching states. The eight switching states create a switch variable vector, $[a \ b \ c]^T$. Two of the eight states occur when all the upper switches are off, $[a \ b \ c]^T = [0 \ 0 \ 0]^T$ and when all the upper switches are on, $[a \ b \ c]^T = [1 \ 1 \ 1]^T$. These two switch state vectors are called the “zero vectors” 0_{000} or 0_{111} , respectively. Table 2-2 shows the other six non-

zero switch vectors for the coinciding state. Knowing the complementary switch is the opposite, 1 indicates the switch is on and 0 indicates the switch is off.

Figure 2-5: Three-phase power converter diagram (Yu and Figoli 1998). The junction of the split DC bus voltage n' can be used as a neutral if the motor allows access to its neutral n .

Table 2-2: Inverter non-zero switch states.

state	a	b	c
1	1	0	0
2	1	1	0
3	0	1	0
4	0	1	1
5	0	0	1
6	1	0	1

Figure 2-6 is an example of the switch states during state 2, when switch a , b , and c' are on (i.e. $[a \ b \ c]^T = [1 \ 1 \ 0]^T$). A simplified circuit in Figure 2-7 provides some insight into what the voltages are across the individual stator windings. During state 2,

the voltage across stator winding a , and b , V_{an} and V_{bn} , respectively is $1/3 V_{dc}$. It can also be shown that the voltage across stator winding c , V_{cn} , is $-2/3 V_{dc}$.

Figure 2-6: Representation of a DC-AC inverter during state 2. Similar representations can be made of each state.

Figure 2-7: Example of a DC-AC inverter equivalent circuit to explain the voltages across the stator windings during state 2. Similar equivalent circuits can be made for each state.

Table 2-3 shows the results of the per-phase voltages during each state. A matrix was developed to provide a simple method to calculate the appropriate voltages during the associated state (Yu and Figoli 1998). Each state's switch vector can be easily inserted into equation (2-7) and the per-phase voltage will be the result.

Table 2-3: Inverter per phase voltages normalized to V_{dc} .

state	V_{an}	V_{bn}	V_{cn}
1	2/3	-1/3	-1/3
2	1/3	1/3	-2/3
3	-1/3	2/3	-1/3
4	-2/3	1/3	1/3
5	-1/3	-1/3	2/3
6	1/3	-2/3	1/3

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}. \quad (2-7)$$

As an example, substituting the switch vector for state 2 the per-phase voltages are

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix} = V_{dc} \begin{bmatrix} 1/3 \\ 1/3 \\ -2/3 \end{bmatrix}. \quad (2-8)$$

Figure 2-8 shows that proceeding through the switch states sequentially generates three quasi-sinusoidal waveforms that are two states out of phase from one another. These phase differences equate to 120° .

The voltage waveforms in Figure 2-8 are delivered directly to the stator windings of the motor. In order to vary the voltages and frequency, a pulse-width modulation technique must be incorporated to generate the modulation signal.

Figure 2-8: Phase-to-neutral waveforms with respect to the state voltages (Holtz 1997, 145). Notice the waveforms resemble sinusoids with a phase shift of 2 states, which equates to 120° .

PULSE-WIDTH MODULATION (PWM)

Pulse-width modulation (PWM) is a technique used to easily control the energy delivered from a power converter, such as a DC-AC inverter, to a load, such as a motor. The PWM is a series of pulses that have a fixed frequency and magnitude, but a variable pulse width. A modulation signal is used to vary the width of the pulses from period to period to create the fundamental frequency delivered to the motor. The pulses toggle the power transistors on and off, according to the same modulation signal. The energy to be delivered to the load depends on the modulating signal; hence, the switching frequency must be much higher than the modulating frequency (Yu and Figoli 1998).

MODULATION TECHNIQUES

There are many different ways to generate the modulation frequency. Three common methods are the suboscillation method, direct sinusoidal method and the space

vector method. The suboscillation method requires individual modulators for the three phases of the motor. This technique is used for fast analog applications (Holtz 1997). The direct sinusoidal, often called the sampled sinusoidal method, uses either analog circuits or digital signal processors and requires a reference sinusoidal input to generate the PWM signal. The design presented in this thesis uses the space vector generated PWM because it does not require a reference sinusoidal input, it produces fewer harmonics, and it generates phase-to-phase RMS voltages that are 15% higher than the direct sinusoidal method (Yu and Figoli 1998).

SPACE VECTOR PWM

When discussing the space vector PWM technique, it is necessary to mention the transformation from a 3-phase system to a 2-phase system. The transformation allows computations to be performed in a 2-dimensional coordinate system rather than the more complex 3-dimensional coordinate system. Figure 2-9 (a) shows the 3-phase plane and Figure 2-9 (b) shows the 2-phase plane.

Figure 2-9: (a) 3-phase plane and (b) 2-phase plane

Three-Phase to Two-Phase Transformation

To transform the 3-phase variables into 2-phase variables, equation (2-9) is used. The variable X represents 3-phase variables and 2-phase variables, in this case it represents voltages or currents specifically.

$$C (X_a + X_b e^{j2\pi/3} + X_c e^{j4\pi/3}) = X_d + jX_q \quad (2-9)$$

Using some trigonometry, equation (2-9) is made into the matrix in (2-10) (Yu and Figoli 1998). Multiplying the 3-phase variables, such as voltages or currents, by the matrix in (2-10) transforms them into the 2-phase variables. The coefficient, C , is used to

$$T_{abc-dq} = C \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (2-10)$$

maintain power between the transformation from the 3-phase coordinate system to the 2-phase coordinate system.

Solving for the Constant, C

To find the constant C , the total power in the 3-phase plane must be equal to the total power in the 2-phase plane,

$$P_{3\phi} = P_{2\phi}, \quad (2-11)$$

thus making

$$V_{an}i_a + V_{bn}i_b + V_{cn}i_c = V_{d1}i_d + V_{q1}i_q. \quad (2-12)$$

For balanced 3-phase systems with sinusoidal currents and voltages,

$$i_a + i_b + i_c = 0, \quad (2-13)$$

$$V_{an} + V_{bn} + V_{cn} = 0, \quad (2-14)$$

and using the matrix in (2-10), the voltages and currents in the 3-phase plane can be substituted for the voltages and currents in the 2-phase plane producing,

$$C \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = C \begin{bmatrix} V_d \\ V_q \end{bmatrix} = C \begin{bmatrix} -3/2 V_{bn} - 3/2 V_{cn} \\ \sqrt{3}/2 V_{bn} - \sqrt{3}/2 V_{cn} \end{bmatrix} \text{ and} \quad (2-15)$$

$$C \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = C \begin{bmatrix} i_d \\ i_q \end{bmatrix} = C \begin{bmatrix} -3/2 i_b - 3/2 i_c \\ \sqrt{3}/2 i_b - \sqrt{3}/2 i_c \end{bmatrix}. \quad (2-16)$$

Substituting the voltages and currents on the right side of equation (2-12) with the voltages and currents transformed by equations (2-15) and (2-16) and using equations (2-13) and (2-14) to solve for i_a and V_{an} on the left side of equation (2-12) produces

$$(-V_{in} - V_{cn})(-i_b - i_c) + V_{bn}i_b + V_{cn}i_c = C^2 \left[\left(-3/2 i_b - 3/2 i_c \right) \left(-3/2 V_{bn} - 3/2 V_{cn} \right) + \left(\sqrt{3}/2 i_b - \sqrt{3}/2 i_c \right) \left(\sqrt{3}/2 V_{bn} - \sqrt{3}/2 V_{cn} \right) \right]. \quad (2-17)$$

Collecting common terms produces

$$2V_{bn}i_b + 2V_{cn}i_c + V_{bn}i_c + V_{cn}i_b = C^2 \left(3V_{bn}i_b + 3V_{cn}i_c + 3/2 V_{bn}i_c + 3/2 V_{cn}i_b \right). \quad (2-18)$$

Finally, solving for C , the constant is found to be

$$C = \sqrt{2/3}. \quad (2-19)$$

Generating the Basic Space Vectors

The per-phase voltages established in Table 2-3 are transformed into 2-dimensional RMS space vector voltages using equation (2-9) to create

$$\bar{U}_s = \left(\sqrt{2/3} \right) (V_{an} + V_{bn} e^{j2\pi/3} + V_{cn} e^{j4\pi/3}) = U_{sd} + jU_{sq}, \quad (2-20)$$

where $\bar{U}_s$ is the voltage space vector for state s . U_{sd} and U_{sq} are the components that make up $\bar{U}_s$ in the 2-dimensional d-q plane (Aller et al. 2000). Substituting the per-

phase voltages into equation (2-20) for the associated state s the voltage vector for that state is generated.

Substituting the per-phase voltages generated by state 2, as shown in Table 2-3, into equation (2-20), the space vector for state 2 is

$$\bar{U}_2 = V_{dc} \left(\sqrt{2/3} \right) \left(\frac{1}{3} + \frac{1}{3} e^{j2\pi/3} + -\frac{2}{3} e^{j4\pi/3} \right). \quad (2-21)$$

The resultant space vector is shown in Figure 2-10.

Figure 2-10: Space Vector, $\bar{U}_2$, generated from the space vector equation using the 3-phase voltages generated during state 2. Similar vectors can be generated using the other states.

The space vector for state 2 can be composed of two scalars in the d-q plane, U_{sd} and U_{sq} . Referring to Figure 2-10, the components are calculated using

$$U_{sd} = V_{dc} \left(\sqrt{2/3} \right) \left[V_{an} * \cos(0^\circ) + V_{bn} * \cos(120^\circ) + V_{cn} * \cos(240^\circ) \right], \text{ and} \quad (2-22)$$

$$U_{sq} = V_{dc} \left(\sqrt{2/3} \right) \left[0 + V_{bn} * \sin(120^\circ) + V_{cn} * \sin(240^\circ) \right]. \quad (2-23)$$

Substituting the values of V_{an} , V_{bn} , and V_{cn} calculated in equation (2-8) for state 2, the scalar components of $\bar{U}_2$ are $[U_{2d} \ U_{2q}] = [1/\sqrt{6} \ 1/\sqrt{2}] V_{dc}$.

The other space vectors can be calculated as shown above by multiplying the T_{abc-dq} transform matrix by the per-phase voltage vectors for each state. For example,

multiplying the per-phase voltages generated by state 3 (see Table 2-3) by the transform matrix T_{abc-dq} , the result in (2-24) is the space vector for state 3. Figure 2-11 shows the six non-zero space vectors and their switch patterns.

$$\bar{U}_3 = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} = \frac{-1}{3} \\ V_{bn} = \frac{2}{3} \\ V_{cn} = \frac{-1}{3} \end{bmatrix} V_{dc} = V_{dc} \begin{bmatrix} \frac{-1}{\sqrt{6}} \\ \frac{1}{\sqrt{2}} \end{bmatrix} \quad (2-24)$$

Figure 2-11: Basic space vectors in the d-q plane with associated switch patterns (Yu and Figoli 1998).

Generating Space Vector PWM

The space vector PWM generation is based on an approximation of the reference voltage vector U_{out} , using the switching patterns for the eight basic space vectors. This can be accomplished by making the average voltage output of the inverter equal to the average of U_{out} within the same period T . Referring to Figure 2-11, the reference voltage

vector U_{out} , can be derived from V_1 and V_2 . V_1 and V_2 are $U_1 \cdot T_1$ and $U_2 \cdot T_2$, respectively. T_1 and T_2 are much smaller than T . The duration of T_1 and T_2 are such that $T \geq T_1 + T_2$. Therefore another time T_0 is inserted to make $T = T_1 + T_2 + T_0$. T_0 is the time when no power is delivered to the load from the inverter. It is made up of a “zero vector”, either 0_{000} or 0_{111} (Yu and Figoli 1998). Equation (2-25) shows how U_{out} can be generated using this technique.

$$T * \overline{U_{out}} = T_1 \overline{U_1} + T_2 \overline{U_2} + T_0 (0_{000} \text{ or } 0_{111}) \quad (2-25)$$

T is equal to the PWM period. How T_1 , T_2 , and T_0 are actually calculated is explained in Chapter 3.

Mapping the desired 3-phase voltage to the d-q plane using the T_{abc-dq} transform matrix shown in (2-10) computes U_{out} . Since the 3-phases are 120° apart, U_{out} rotates around the d-q plane at the same frequency as the desired 3-phase output. This design will operate only in the under-modulation region where the maximum magnitude of U_{out} must fit inside the envelope created by the space vector hexagon shown in Figure 2-11. This provides a maximum magnitude of $V_{dc}/\sqrt{2}$ for U_{out} (Yu and Figoli 1998). Figure 2-12 and the equations in (2-26) prove the maximum reference space vector magnitude is $V_{dc}/\sqrt{2}$.

The phase-to-phase and the per-phase RMS values are $V_{dc}/\sqrt{2}$ and $V_{dc}/\sqrt{6}$, respectively. The phase-to-phase and per-phase RMS values for the direct sinusoidal PWM generation technique, mentioned previously are $V_{dc}\sqrt{3}/(2\sqrt{2})$ and $V_{dc}/(2\sqrt{2})$, respectively (Mohan, Undeland, and Robbins 1995, 226-228). Thus, the space vector

PWM generated output is $2/\sqrt{3}$ or 1.15 times greater than the direct sinusoidal PWM method can generate (Yu and Figoli 1998).

Figure 2-12: Sector I of the space vector hexagon.

The magnitude of $U_{out(MAX)}$ is $V_{dc}/\sqrt{2}$.

$$\sin(60^\circ) = \frac{|U_{out(MAX)}|}{|U_1|}$$

$$|U_1| = \frac{\sqrt{2}}{\sqrt{3}} * V_{dc} \quad \therefore \quad (2-26)$$

$$|U_{out(MAX)}| = \frac{\sqrt{3}}{2} * \frac{\sqrt{2}}{\sqrt{3}} * V_{dc} = \frac{V_{dc}}{\sqrt{2}}$$

The space vector PWM is generated entirely in the DSP based controller of the variable frequency drive. The implementation is discussed in Chapter 3.

CHAPTER 3: DESIGN IMPLEMENTATION

There are two major sections to the design of this variable frequency drive. The first is the hardware design, which consists of the controller, the controller-to-DC-AC inverter interface, and finally, the DC-AC inverter. The second section is the software used by the DSP to collect the desired output frequency and generate the space vector PWM. Figure 3-1 is a block diagram of the variable frequency drive. The DSP performs all the calculations to generate the space vector PWM per the desired frequency input. The inverter delivers the energy to the load at the commanded frequency.

Figure 3-1: An open loop, 3-Phase, Variable Frequency Drive Block Diagram. A 10-turn potentiometer is used to adjust the 3-phase frequency and a DSP controller is used to create the space vector generated PWM signals to the inverter. The inverter delivers the power to the load (Yu and Figoli 1998).

HARDWARE

There are three major parts to the hardware design: the DSP controller, the DSP controller-to-DC-AC inverter interface board, and the DC-AC inverter/IPM. Figure 3-2 is the hardware layout diagram.

Figure 3-2: Hardware Layout Diagram

DSP CONTROLLER

An extensive market search was performed to locate a manufacturer that made an evaluation board for their Digital Signal Processor (DSP) that could be used as the controller for this variable frequency drive. The results from the search can be found in Appendix B. The controller chosen is an evaluation module for the TMS320F240 (DSP) from Texas Instruments [TMDS3P603070, Texas Instruments, Dallas, TX]. This DSP is

optimized specifically for motor control and power conversion applications. Some of the keys features of the TMS320F240 DSP are:

- Three 16-bit, 6-mode, general-purpose timers
- 12 PWM channels
- A quadrature encoder pulse interface (QEP)
- Four capture units
- Dual 10-bit, 8-channel ADCs
- Synchronous and asynchronous communications peripherals
- A programmable phase-locked-loop clock module
- 544 words of dual access RAM
- 16K words of on-chip Flash memory

The evaluation module board has some added features:

- 4-channel 12-bit DAC
- 128K words of external memory
- RS-232 compatible, DB-9 serial port
- Four 34-pin connectors to access relevant signals on the evaluation board

The emulation port, which is compatible with the IEEE1149.1 standard, allows the evaluation board to be the target board for the emulator (Texas Instruments 1997).

See Appendix C for an image of the evaluation module. The controller performs all the calculations necessary to generate the space vector PWM signals that are delivered to the DC-AC inverter.

DC-AC INVERTER / IPM

The DC-AC inverter could have been implemented in one of two ways. The first method would be to design the DC-AC inverter using discrete components. This method would require not only designing circuitry to deliver the power required to the load but also designing the control circuitry to ensure the inverter would be protected from short-circuits, over-temperature and under-voltage. The second method, which is the method chosen for this design, is to purchase an Intelligent Power Module (IPM). An IPM incorporates the control circuitry to protect the power transistors from short-circuits, over-temperature, and under-voltage. It also provides an interface to connect the switching signals from a controller.

A search was conducted to determine which IPM would be used in this design. Some of the parameters that were considered were availability, cost, power capabilities, and performance. Refer to Table A-2 in Appendix A for a list of manufacturers. The DC-AC inverter used in this design was made by Powerex. The PM100CVA060 IPM is rated for 600 volts and 100 amperes. It can operate at a switching frequency up to 20kHz, which is the PWM switching frequency used in this design. Refer to the data sheet in Appendix D for more information.

DSP CONTROLLER TO DC-AC INVERTER INTERFACE

An interface board using opto-isolators was designed to isolate the high power switching signals of the IPM from the sensitive digital signals on the controller. Switching high voltages can generate electrical noise that may interfere with the digital signals. To prevent the unwanted noise from affecting the integrity of the digital signals,

opto-isolators were used to separate the digitally generated PWM signals from the control voltages of the IPM. To isolate the switching power supplies from the control voltages of the IPM, an isolated DC-DC supply was used. A schematic of the interface board design is in Appendix E. The interface from the DSP to the IPM was borrowed from application notes for the IPM from Powerex.

The interface board was designed to mount directly onto the IPM. This reduces the length of the conductors, eliminates the need for cables, and increases electrical noise immunity.

Opto-Isolators

Opto-isolators optically isolate two signals. The first signal generates light, which when detected generates the second signal, thereby sharing neither grounds nor power. The two types of opto-isolators used were recommended by Powerex. The more critical of the two types is the HCPL-4504 from Agilent Technologies. The specification sheet is in Appendix F. The HCPL-4504 was designed specifically for IPM interfacing. These opto-isolators interface the sensitive PWM signals to the control voltages of the IPM.

The second opto-isolator is the Sharp PC817. This opto-isolator is used to interface the fault lines generated by the IPM to the DSP. For this design, the fault lines are not monitored by the DSP. The opto-isolators were installed so that the design could easily be modified to monitor the faults generated by the IPM. The design currently has the opto-isolated fault outputs connected to LEDs for visually detecting a fault. The specification sheet for the PC817 is in Appendix F.

The control voltages of the IPM that are opto-isolated from the DSP were generated by an isolated DC-DC voltage supply.

Isolated DC-DC Supply

The isolated DC-DC supply that is used to isolate the switching DC supply from the control signals on the IPM is made by Powerex, M57140-01. The specification sheet is in Appendix G. Isolated DC-DC converters are more expensive than non-isolated converters (Born 2000). This design was a prototype; therefore, price was not as important as isolating the control voltages from the rest of the switching DC power. The input of the isolated DC-DC supply has a narrow range of 18 to 22VDC. The output is 15VDC. In this design, the input is from a 24VDC switching power supply that has been adjusted to 21.5VDC; narrowly meeting the supply input specification.

Opto-isolators and isolated DC-DC converters are good design practices to reduce interference. However, other techniques to reduce the indirect coupling of high-powered signals must also be used to ensure signal integrity.

EMI Reduction

With the high voltages used and the high current ratings supported by the IPM, the design would be at risk from electro-magnetic interference (EMI). To prevent EMI, the top of the interface board has a ground plane weaved between the holes of the board. This layer is connected to earth ground as a shield. Another preventative measure taken was the implementation of a shielded cable between the DSP controller and the interface board. The shield of the cable is connected to the ground plane on the interface board. Connecting the shield to only one end of the cable prevents ground loops. One last

design practice that was implemented was the sheet metal box with welded corners to prevent interference from external sources such as motors or other EMI generating equipment.

All this hardware is controlled by software that is downloaded to the DSP controller from a computer. The next section presents a detailed description of what the software must do to generate the space vector PWM signals.

SOFTWARE

The program that controls this design was borrowed from a program written by 'Texas Instruments' application engineer Zhenyu Yu (Yu and Figoii 1998). The program was written to operate an inverter from Spectrum Digital [Stafford, TX.] and control the speed of a motor with a rated frequency of 60Hz from 0Hz to 120Hz. The speed of the motor was adjusted using push buttons. The program was carefully altered to accommodate the requirements for this design, which is to generate a 3-phase output from 0Hz to 1200Hz. The frequency is adjusted by sampling the voltage across a potentiometer. The modified program is in Appendix H.

OVERVIEW

This program has two distinct sections. The first section is the sampling loop, where the desired 3-phase output frequency and the magnitude of the associated reference space vector U_{out} is generated. During the sampling loop, the program obtains the desired frequency by sampling the voltage on the speed control potentiometer that interfaces to the analog-to-digital converter (ADC) on the DSP. The ADC value is then converted into an angular frequency, and the angular frequency is converted to the magnitude of the

reference space vector U_{out} based on the V/Hz criteria. Once the conversions are complete, the processor waits for an interrupt. See Figure 3-3 for the program flow chart. Refer to (Texas Instruments, CPU Instructions 1999 and Peripherals 1999) for more specific information about the TMS320F240 digital signal processor. The other section is the interrupt service routine.

First, an explanation of an interrupt and interrupt service routine is necessary. An *interrupt* is a signal to the processor that interrupts the program to immediately attend to a critical process. The program generates an interrupt every 50 μ s. An interrupt service routine (ISR) is generally a small program that attends to the critical process for which the interrupt is generated. Once the ISR is complete, the program resumes where it was interrupted. This program has one interrupt service routine, during which the DSP performs the calculations necessary to generate the PWM signals, applying the space vector technique, based on the frequency and magnitude of the reference space vector collected in the sampling loop.

Many of the conversions in this program are generated by the use of look-up tables. A look-up table is mathematical data stored in memory and indexed in a unique way to be used during the execution of a program instead of performing complex calculations for each conversion. As an example, this program stores the sine values (i.e. $\sin(x)$) of 360 angles from 0° to 90° rather than calculating them during the execution of the program. The data is accessed by converting an angle to an index number to retrieve the associated sine value. This will be discussed in more detail later.

Figure 3-3: Program Flow Chart (Yu and Figoli 1998)

Some background information is necessary to discern how the fixed point DSP maintains its accuracy and generates the PWM signals. The accuracy is maintained using the D-scaling technique.

D-Scaling Notation

D-scaling notation is used in the original program written by Zhenyu Yu and maintained in the modified version. This explanation of the D-scaling technique was borrowed directly from the explanation in the application notes (Yu and Figoli 1998) containing the program.

To achieve the most accurate results, the software incorporates D-scaling notation. It is very similar to the popular Q-scaling notation.

$$D_x = Q(15 - x) \quad (3-1)$$

The scaling factor provides the highest resolution possible, but it must be tracked to ensure no mathematical errors. A variable with scale D_x can represent numbers from $-2^x + \Delta$ to $2^x - \Delta$, where Δ is an infinitely small number.

Consider equation (3-2)

$$X = a * Y + b * Z, \quad (3-2)$$

where $a = 0.124$, $b=0.4$. Y and Z are in separate ranges, 0-7.999 and 0-0.999, respectively. The scale of a can be assigned to D_{-3} (or Q_{18}) which represents the numbers from 0.12499 to 0.124999. In D_{-3} notation, 0.124 becomes $0.124 * 2^{18}$ or 32506. The other numbers, b , Y , and Z , would use the scales of D_{-1} , D_3 and D_0 , respectively. When two numbers are multiplied together, the scales are handled per equation (3-3).

$$D_x * D_y = D_{(x + y)} \quad (3-3)$$

The multiplication of a and Y create a D_0 scaled number and the multiplication of b and Z create a D_{-1} scaled number. Two numbers added together must have the same D notation. Therefore, $b*Z$ has to shift to the right by one bit so the addition to $a*Y$ is accurate. When programming, the programmer must pay attention to additions and subtractions to make sure there is no overflow.

Generating the PWM

One of the great features of the TMS320F240 DSP is the ability to generate PWM signals. This DSP can generate 12 discrete PWM signals. In this design, only six are used.

There are two types of PWM signals, symmetric and asymmetric. The asymmetric PWM has the edge aligned to the end of the PWM period. The symmetric PWM has the pulse aligned to the center of the period. Figure 3-4 shows the difference between the symmetric and asymmetric PWM. Symmetric PWM signals generate fewer harmonics in the voltage and current outputs (Yu and Figoli 1998). The symmetric PWM signal generation starts with the general-purpose timers that are also built into the DSP.

For clarity, Table 3-1 links the PWM signal number to the associated switch in the DC-AC inverter. The PWM signal numbers (i.e. 1, 2, 3...) will be used throughout the rest of the thesis.

General-purpose timer 1, GPTimer1, is a programmable timer. It can be programmed to be an up counter, down counter, or up-down counter by writing to its configuration register, T1CON. Symmetrical PWM signals require the timer to be in the

Figure 3-4: Symmetric and Asymmetric PWM signals (Yu and Figoli 1998).

Table 3-1: PWM signal to associated inverter switch.

PWM Signal	Inverter Switch
PWM1	a
PWM2	a'
PWM3	b
PWM4	b'
PWM5	c
PWM6	c'

up-down counting mode. A register, TPER1, is loaded with a value that divides the system clock, $TPER1 = T_{PWM}/2$. In this design, the desired PWM frequency is 20kHz, which would correspond to TPER1 obtaining a value of 500 with a system clock of 20MHz. Compare registers named CMPR1, CMPR2, and CMPR3 are loaded with the compare values that are used to turn on and off PWM1, PWM3 and PWM5, respectively. PWM2, PWM4, and PWM6 are controlled based on PWM1, PWM3, and PWM5, respectively; therefore, only three compare registers are required.

The PWM can easily be programmed to be active low or active high. The hardware interface design dictates this decision. In this design, the hardware is such that

the DSP is sinking current to turn on the LED in the opto-isolator; therefore PWM1, PWM3, and PWM5 must be active low. Refer to Appendix E for a schematic of the opto-isolator implementation. Since PWM2, PWM4, and PWM6 are the opposite, they must be active high. This can be accomplished simply by setting the appropriate bits in register ACTR.

Dead-band is easy to incorporate with this DSP to prevent shoot-through. The register, DBTCON, can be loaded with the number of clock cycles required for the dead-band. In this design, $2.5\mu\text{s}$ is the required dead-band for the IPM. The IPM data sheet from Powerex provided this requirement. Each clock cycle is 50ns; therefore, the required number of cycles is 50 or 32h. This value is loaded into the upper portion of the DBTCON register.

Another general-purpose timer, GPTimer2 is synchronized with GPTimer1 and is used for the sampling frequency. In this design, the sampling frequency has been set to 20kHz. 20,000 times per second, an interrupt is generated by GPTimer2. Again, setting up the appropriate registers is all that is required. By not masking the GPTimer2 interrupt bit in the interrupt masking register IMRB an interrupt is generated every $50\mu\text{s}$.

Figure 3-5 represents the sequence of the timers, PWM signals, and interrupts. Figure 3-5 could not be drawn to scale due to the number of pulses it would require to take a 20MHz clock and divide it into a 20kHz timer. It is merely a representation of what is happening during the timer cycles.

The registers used to generate the symmetric PWM and interrupts were named based on the header file created by Texas Instruments in Appendix I. This header file

Figure 3-5: DSP General Purpose Timers generating the symmetrical PWM signals and sampling interrupts.

sets the associated register address with a descriptive name, making it easier to understand the functionality of the program.

Now that accuracy maintenance and PWM generation have been clarified, the details of the program used to run this variable frequency drive, presented in the following sections, can be better understood.

SAMPLING LOOP

The first major section of the program is the generation of the desired output frequency and reference space vector from the sampled user input. This is all performed between the interrupts.

Converting User Input into Angular Frequency

The user can adjust the frequency of the 3-phase output by turning a 10-turn potentiometer on the front of the box that houses the design. The potentiometer changes the voltage read by the ADC on the DSP. The voltage can vary from 0 to 5 volts. This voltage range corresponds to the frequency range of 0Hz to 1200Hz.

The ADC is read after the interrupt routine is complete. The data is shifted to the right 1 bit. Since the ADC is only 10 bits, the highest value that can be read is 7FE0h, which pertains to the highest frequency, 1200Hz. The ADC reading is in D_1 notation, which scales the voltage reading to a number between 0 and 1. The next step is to convert the ADC reading into angular frequency. A simple ratio is used for the conversion. 1200Hz corresponds to approximately 7540 rad/sec; therefore multiplying the ADC counts by $(7540 \text{ rad/sec} / 7FE0h \text{ counts})$ the proper angular frequency will be achieved. Since 7FE0h with D_1 scaling is approximately equal to 1, the frequency to angular frequency variable F_W is set to 30160 with D_{13} scaling. The next step is to calculate the reference space vector, U_{out} .

Angular Frequency to Reference Space Vector U_{out}

Now that the angular frequency has been calculated, it must be converted to the magnitude of the reference space vector voltage $|U_{out}|$. It was shown in the theory section

that the maximum RMS voltage output using space vector PWM was $V_{dc}/\sqrt{2}$. Using the V/Hz method, $|U_{out}|$ can be found by multiplying the angular frequency by the maximum voltage ratio, $1/\sqrt{2}$, divided by the rated angular speed. In this design, 1000Hz is used as the rated angular speed. The ω to $|U_{out}|$ conversion factor is as follows,

$$\omega \rightarrow |U_{out}| = \frac{1/\sqrt{2}}{[1000 * 2\pi]_{rad/sec}} = 0.0011254. \quad (3-4)$$

The angular frequency to $|U_{out}|$ conversion variable W_U is set to 15105 with D_{12} scaling. A minimum $|U_{out}|$ is necessary to compensate for the stator resistance at low frequencies. In this program, the minimum $|U_{out}|$ is $0.2219 * V_{dc}$. This value was selected during experiments to allow the motor to rotate. Figure 3-6 shows the volts per frequency slope the software uses to calculate the magnitude of the space vector reference voltage U_{out} .

Figure 3-6: V/Hz implementation in the software. The voltage boost at low frequencies was found experimentally for the motor used during the experiments. The U_{out} axis is normalized to the bus voltage, V_{dc} .

Once the angular frequency and the magnitude of U_{out} are determined, the program will wait for an interrupt from general-purpose timer 2.

INTERRUPT SERVICE ROUTINE

The second major section of the program is the interrupt service routine, where the space vector PWM is calculated every 50 μ s sample period. The first calculation required is the 32-bit integration to determine the phase of U_{out} .

Using Integration to Find the Phase Angle of U_{out}

Now that the magnitude of U_{out} is calculated, its phase must be obtained. The phase is used to find the sector and quadrant in which U_{out} resides. This is necessary for decomposition.

The program multiplies the angular frequency, calculated before the interrupt, by the sampling time and adds the result to the phase angle calculated during the previous interrupt to generate the new phase angle. To easily manage the accumulated phase angle of U_{out} , 360° is subtracted from the accumulated phase angle when it is greater than 360°.

Once the angle of U_{out} is determined, the quadrant in which it resides can be determined and its vector components calculated by finding the sine and cosine of the angle.

Determining the Quadrant, and the Sine and Cosine of the Phase of U_{out}

Figure 3-7 can be used as a visual aid for the following explanation. The quadrant in which U_{out} resides is needed to determine the value of the sign of the sine variable (SS) and the value of the sign of the cosine variable (CS) for the given phase angle of U_{out} . This method allows the look-up table to contain only 1/4 of a period of sine values because

Figure 3-7: Value of the sign of the sine (SS) variable and cosine (CS) variable depending on the quadrant that U_{out} is in.

the values repeat themselves with only a change in the sign. Once the quadrant is determined, a signed value can be given to the sine and cosine variables SS and CS, respectively. The quadrant that U_{out} is in is determined systematically by subtracting the quadrant's boundary angles from the phase angle of U_{out} computed earlier, and comparing the result to zero. Depending on the quadrant, the phase is subtracted from the boundary limit or the boundary limit is subtracted from the phase. The result is translated into an index number that is used to look up the sine and cosine values.

As an example, suppose the phase of U_{out} is 150° . The first step would be to subtract 90° from 150° . Since the result would be greater than 0, the condition to fit into quadrant 1 would fail. The next step would be to subtract the angle from 180° . The result would be 30° . The result is greater than 0° and fits the condition to be in quadrant 2. The sign of the sine variable SS is assigned -1 and the sign of the cosine variable CS is assigned $+1$ (Refer to Figure 3-7). The look-up table has 360 D_1 scaled numbers that are the sine values of 360 angles between 0° and 90° . The resultant angle, in this case

30° , is multiplied by the look-up table's angle-to-index translation number, $4 = (360/90^\circ)$.

The result of the multiplication "points" to the number of the table entry. In this example, 30° would point to table entry 120, which is 8192 in D_1 scaling, and would convert to 0.500, which is the sine of 30° . The cosine is simply obtained by counting from the end of the table since the cosine and sine are 90° out of phase. This entry is 14189 and converts to 0.866025, which is the cosine of 30° .

Now that the quadrant is known and the sine and cosine of the phase of U_{out} have been determined, U_{out} can be broken down into its vector components. In addition, from the phase angle of U_{out} , the sector in which U_{out} resides must be found to determine the switching sequence.

Determining the Vector Components and the Sector of U_{out}

The decomposition algorithm requires the components of U_{out} and the sector in which U_{out} resides. The components of U_{out} , called U_d and U_q are the vector components on the d-q axis that make up U_{out} (See Figure 3-8). Knowing the phase angle and the magnitude of U_{out} , U_d and U_q are easily found using a little trigonometry.

Figure 3-8: Components of U_{out} , U_d and U_q .

Decomposition of U_{out} into T_1 , T_2 , and T_0

The final step in this process is decomposing the vector U_{out} into T_1 , T_2 , and T_0 , then loading the compare registers with the proper data and in the proper sequence, using the appropriate basic space vectors. To clarify some notation in this section, U_s refers to a basic space vector and $U_{s\pm1}$ refers to its adjacent basic space vector 60° away. Since this VFD only rotates counter-clockwise relative to the d-q plane, only U_{s+1} will be used in the following discussion.

The decomposition starts with the following equation,

$$T_{PWM} * \overline{U}_{out} = \overline{U}_s * T_1 + \overline{U}_{s+1} * T_2. \quad (3-5)$$

T_{PWM} is the PWM period. U_s and U_{s+1} are the basic space vectors that make up U_{out} . The objective is to solve for T_1 and T_2 so that the average voltage of U_{out} can be generated using the switching sequence of U_s and U_{s+1} . Knowing the value of T_1 and T_2 , T_0 can be calculated by subtracting T_1 and T_2 from T_{PWM} . The compare registers for the timer require half of the total times of T_1 , T_2 , and T_0 because the PWM signals are symmetric, $T_p = T_{PWM}/2$. The reference space vector can be represented as $U_{out} = [U_d \ U_q]^T$. Therefore the decomposition equation is

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} * M(s) = \frac{1}{2} \begin{bmatrix} T_1/T_p & T_2/T_p \end{bmatrix}, \quad (3-6)$$

where $M(s)$ is the decomposition matrix for a specific sector s . It is made of the inverse of the matrix created by the basic space vectors U_s and U_{s+1} (i.e. $[\overline{U}_s \ \overline{U}_{s+1}]^T$).

Equation (3-7) shows how to generate the $M(s)$ matrix for any sector s . $M(s)$ is stored in

$$M(s) = \frac{\begin{bmatrix} U_{(s+1)2} & -U_{(s+1)1} \\ -U_{(s)2} & U_{(s)1} \end{bmatrix}}{U_{s1} * U_{(s+1)2} - U_{(s+1)1} * U_{s2}} \quad (3-7)$$

a look-up table that is indexed by the sector. As an example, suppose U_{out} is in sector 1, therefore

$$M(1)^{-1} = [\bar{U}_1 \quad \bar{U}_2] = \begin{bmatrix} \sqrt{2}/\sqrt{3} & 1/\sqrt{6} \\ 0 & 1/\sqrt{2} \end{bmatrix}. \quad (3-8)$$

Refer to Figure 2-11 for the basic space vectors that make up sector 1. Since $M(s)$ is

$[\bar{U}_1 \quad \bar{U}_2]^{-1}$, the $M(1)$, D_1 scaled values in the look-up table are

$$M(1) = \begin{bmatrix} \sqrt{3}/\sqrt{2} & -1/\sqrt{2} \\ 0 & \sqrt{2} \end{bmatrix}. \quad (3-9)$$

In the program, the members of the decomposition matrix are multiplied by $[U_d \ U_q]^T$, found in the previous section, to find $0.5(T_1/T_p)$ and $0.5(T_2/T_p)$. The result is multiplied by T_p , leaving $0.5*T_1$ and $0.5*T_2$. Once T_1 and T_2 are calculated, the sector will determine which switch will toggle first. Then the compare registers will be loaded accordingly. The values are loaded into the compare registers, varying the width of the PWM.

Constants and Variables

Tables 3-2 and 3-3 contain information about some of the constants and variables used in the assembly program. The constants and variables are described conceptually

Table 3-2: Select software constants and explanations

Constant	Constant Description	D _i	Constant Equation	Constant Value in Hex	X by	Converted	Units
F_W	Hertz to angular frequency conversion	D ₁₃	$\frac{1200 * 2\pi}{7FE0h}$	75D0h	2 ⁻²	7540	Rad/s/Hz
W_U	Angular frequency to reference space vector U _{out} conversion	D ₁₂	$\frac{1/\sqrt{2}}{2\pi * 1000}$	3B01h	2 ⁻²⁷	112.5x10 ⁻⁶	V/rad/s
min_U	Minimum value for space vector U _{out} , i.e. "boost"	D ₁	NA	0E34h	2 ⁻¹³	.2219	Ratio of V _{dc}

Table 3-3: Select software variables and explanations

Variable	Variable Description	D _i	Affected by	Variable Range in Hex	X by	Converted Range	Units
set_F	Desired frequency in Hz	D ₀	ADC15 value from speed adjustment potentiometer	0 - 7FE0h	2 ⁻¹⁵	0 - 1	Ratio of max motor speed
S_W	Desired angular frequency	D ₁₃	set_F * F_W	0 - 75D0	2 ⁻²	0 - 7540	Rad/s
S_U	Desired space vector U _{out}	D ₁	S_W * W_U	0 - 2D41h	2 ⁻¹³	0 - 0.7071	Ratio of V _{dc}
theta_r	U _{out} phase angle	D ₃	$\frac{20kHz}{S_W/2\pi} \sum_{n=0}^{2\pi} S_W \cdot 50\mu n$	0 - 6488h	2 ⁻¹²	0 - 2π	Radians
theta_m	theta_r truncated to a value from 0 to π/2	D ₃	NA	0 - 1922	2 ⁻¹²	0 - π/2	Radians
U _d	Horizontal component of U _{out} vector	D ₃	S_U * Cos(theta_m)	0 - 0B50h	2 ⁻¹²	0 - 0.7071	Ratio of V _{dc}
U _q	Vertical component of U _{out} vector	D ₃	S_U * Sin(theta_m)	0 - 0B50h	2 ⁻¹²	0 - 0.7071	Ratio of V _{dc}

and mathematically providing insight as to how the numbers are generated and affected by other constants and/or variables. Note, only the variables that directly represent the operation of the VFD are presented.

When this program is operating, the design produces voltage waveforms that generate sinusoidal currents through an inductive load at a specified frequency. The empirical results are shown in the Chapter 4.

CHAPTER 4: EXPERIMENTAL RESULTS

The following data, shown in Figures 4-1 to 4-22, were collected from the 3-phase variable frequency drive. Two power supplies were used to increase the bus voltage, V_{dc} , to over 100V. This chapter describes the test equipment used to collect the results in Table 4-1, demonstrates the 3-phase constant current waveforms at multiple frequencies up to 1200Hz, displays the average phase-to-neutral and average phase-to-phase voltage waveforms used to generate the sinusoidal currents, and shows the symmetric PWM signals used to create the voltage waveforms.

TEST EQUIPMENT

Table 4-1: Test equipment used to collect the experimental data

Equipment	Manufacturer	Model	Specifications
Oscilloscope	Tektronix	540C	4 channels
Current Probe Amplifier	Tektronix	AM503	NA
Current Probes	Tektronix	A6302	NA
Oscilloscope Voltage Probes	Tektronix	P6139A	NA
Digital Multimeter	Tektronix	TEK DMM247	NA
Variable DC Power Supply	Hewlett Packard	6032A	0-60VDC, 1000W
Fixed DC Power Supply	Astec	LPS255	48V, 10A
3-phase AC Induction Motor	Vickers-Welco	Not known	1.1HP, 3700RPM, 400Hz, 208VAC

THREE-PHASE SINUSOIDAL CURRENTS

The 3-phase sinusoidal currents were measured using three Tektronix [Beaverton, OR] current probes. A current probe amplifier was used to boost the signal to the oscilloscope. The oscilloscope was set to 10mV/division and the amplifier was adjusted to output a voltage that corresponds to a current per 10mV. As an example, Figure 4-1 shows the current probe amplifier set to 5A/10mV. The amplitude of the signal is 12.0mV. The corresponding current at 60Hz is simply 5A/10mV times the measured 12.0mV peak-to-peak voltages, resulting in 6A peak-to-peak. Figure 4-2 and 4-3 show the sinusoidal currents through the motor windings at 600Hz and 1200Hz, respectively.

Figure 4-1: Three-phase sinusoidal currents at 60Hz. The phases are 120° apart. The current probe amplifier was set to 5A/10mV, [5A/div] measuring 6A peak-to-peak current. The bus voltage measured 102.5VDC and the bus current measured 0.43A

Figure 4-2: Three-Phase Sinusoidal Currents at 600Hz. Notice the phases are 120° apart. The current probe amplifier was set to 5A/10mV, [5A/div] measuring 6.8A peak-to-peak current. The bus voltage measured 102.5VDC and the bus current measured 0.68A

Figure 4-3: Three-Phase Sinusoidal Currents at 1200Hz. Notice the phases are 120° apart. The current probe amplifier was set to 5A/10mV, [5A/div] measuring 6.8A peak-to-peak current. The bus voltage measured 102.5VDC and the bus current measured 0.8A

The amplitude of the 3-phase sinusoidal currents varied very little from 60Hz to 1200Hz, providing constant current to the motor as the frequency was increased.

Figure 4-4 shows half the period of one of the phase currents at 500Hz. It is hard to see but looking closely, the residue of the 20kHz switching frequency can be seen.

Figure 4-4: Switching frequency on the current waveform. Notice the 20kHz PWM switching residue. The larger the inductance, the smaller the switching ripple. The fundamental frequency is 500Hz.

IDEAL SPACE VECTOR VOLTAGE WAVEFORM

This section presents the ideal voltage waveform that is generated when using the space vector modulation technique. Figure 4-5 is an illustration of the ideal phase-to-neutral average voltage waveform (Pinto et al, 2000). This waveform produces sinusoidal average phase-to-phase voltages. The amplitude and frequency of the waveform in Figure 4-5 varies due to the V/Hz criteria. As the frequency increases, the amplitude increases. The amplitude is a function of the bus voltage V_{dc} .

Figure 4-5: The ideal space vector phase-to-neutral average voltage waveform. It produces sinusoidal phase-to-phase average voltages. This illustration of this waveform was created from a similar waveform seen in (Pinto et al 2000).

MEASURED SPACE VECTOR VOLTAGE WAVEFORMS

The empirical data in this section was collected directly at the output of the PWM signals from the DSP controller. Four sets of data were collected at 60Hz, 600Hz, and 1200Hz. These frequencies were chosen to demonstrate the voltage waveforms throughout the frequency spectrum of the variable frequency drive. The four sets of data include the phase-to-neutral switching voltage waveform, the phase-to-phase switching voltage waveform, the phase-to-neutral average voltage waveform, and the phase-to-phase average voltage waveform.

It should be noted that the word “filtered” and “average” are interchangeable in this section, because the average voltage waveforms were produced by a filter. It should

also be noted that since the voltage waveforms were collected from the digital PWM signals of the DSP, the “neutral” reference was digital ground.

The phase-to-neutral average voltage waveforms were collected by filtering the phase-to-neutral switching voltage waveforms through a resistor-capacitor network with a time constant τ of 100 μ s. A 1000 Ω resistor and a 0.1 μ F capacitor were used to realize the low-pass filter. The phase-to-phase waveforms were produced by using the math functions on the oscilloscope. To demonstrate the phase-to-phase voltages, phase 2 was subtracted from phase 1, phase 3 was subtracted from phase 2, and phase 1 was subtracted from phase 3. It is hard to extract meaningful data from the switching waveforms. They are presented to provide the non-filtered voltage waveforms to compare to the filtered voltage waveforms for completeness. The average or filtered voltage waveforms are more descriptive because they show the average voltages that produce the sinusoidal currents through the stator of the motor that are shown in Figures 4-1 to 4-3.

THREE PHASE VOLTAGE WAVEFORMS AT 60HZ

Figure 4-6 and Figure 4-7 show the phase-to-neutral switching voltage waveforms and the phase-to-neutral average voltage waveforms, respectively. Note the average voltage waveforms in Figure 4-7 resemble the ideal space vector average voltage waveform in Figure 4-5.

Figure 4-6: Phase-to-neutral switching voltage waveforms at 60Hz. Phase 1 (top), phase 2 (middle), and phase 3 (bottom) were measured with the oscilloscope set to 5V/div at a 4ms/div time scale. Notice there is little meaningful data to extract but it is presented as a comparison to the filtered data in Figure 4-7.

Figure 4-7: Phase-to-neutral average voltage waveforms at 60Hz. The waveforms were generated by filtering Figure 4-6 through a low-pass filter with a time constant of 100 μ s. Phase 1 (top), phase 2 (middle), and phase 3 (bottom) have a fundamental frequency of 60Hz and are 120° apart. The oscilloscope is set to 1V/div at a 10ms/div time scale.

Figure 4-8 and Figure 4-9 present the phase-to-phase switching voltage waveforms and the phase-to-phase average voltage waveforms, respectively. Note the average voltage waveforms in Figure 4-9 are sinusoidal with a fundamental frequency of 60Hz and 120° apart. These sinusoidal voltages produce the sinusoidal current waveforms in Figure 4-1.

There is a noticeable “dead-time” in the phase-to-phase switching voltage waveforms in Figure 4-8. “Dead-time” is the time where the phase-to-phase switching voltage is zero. This is due to the pulses having such a short pulse width that the oscilloscope did not capture them. If this “dead-time” truly existed then it would be noticeable in the phase-to-phase average voltage waveforms in Figure 4-9 and the current waveforms in Figure 4-1.

Figure 4-8: Phase-to-phase switching voltage waveforms at 60Hz. Phase 1-2 (top), phase 2-3 (middle), and phase 3-1 (bottom) were measured with the oscilloscope set to 10V/div at a 4ms/div time scale. Notice there is some “dead-time” where the phase-to-phase switching voltage is zero for an extended period of time. This is due to the pulses having such a short pulse width that they could not be captured by the oscilloscope.

Figure 4-9: Phase-to-phase average voltage waveforms at 60Hz. The waveforms were generated by filtering Figure 4-8 through a low-pass filter with a time constant of 100 μ s. Phase 1-2 (top), phase 2-3 (middle), and phase 3-1 (bottom) have a fundamental frequency of 60Hz and are 120° apart. The oscilloscope is set to 1V/div at a 10ms/div time scale.

THREE PHASE VOLTAGE WAVEFORMS AT 600HZ

Figure 4-10 and Figure 4-11 show the phase-to-neutral switching voltage waveforms and the phase-to-neutral average voltage waveforms, respectively. Note the average voltage waveforms in Figure 4-11 do not closely resemble the ideal space vector average voltage waveform in Figure 4-5. Since the PWM frequency is 20kHz and the fundamental frequency is 600Hz, one period of the average phase-to-neutral voltage waveform is constructed using only 33 PWM cycles, hence unable to closely produce the ideal space vector average voltage.

Figure 4-10: Phase-to-neutral switching voltage waveforms at 600Hz. Phase 1 (top), phase 2 (middle), and phase 3 (bottom) were measured with the oscilloscope set to 5V/div at a 400μs/div time scale. Notice there is little meaningful data to extract but it is presented as a comparison to the filtered data in Figure 4-11.

Figure 4-11: Phase-to-neutral average voltage waveforms at 600Hz. The waveforms were generated by filtering Figure 4-10 through a low-pass filter with a time constant of 100μs. Phase 1 (top), phase 2 (middle), and phase 3 (bottom) have a fundamental frequency of 600Hz and are 120° apart. The oscilloscope is set to 2V/div at a 400μs/div time scale.

Figure 4-12 and Figure 4-13 exhibit the phase-to-phase switching voltage waveforms and the phase-to-phase average voltage waveforms, respectively.

Figure 4-12: Phase-to-phase switching voltage waveforms at 600Hz. Phase 1-2 (top), phase 2-3 (middle), and phase 3-1 (bottom) were measured with the oscilloscope set to 10V/div at a 400μs/div time scale.

Figure 4-13: Phase-to-phase average voltage waveforms at 600Hz. The waveforms were generated by filtering Figure 4-12 through a low-pass filter with a time constant of 100μs. Phase 1-2 (top), phase 2-3 (middle), and phase 3-1 (bottom) have a fundamental frequency of 60Hz and are 120° apart. The oscilloscope is set to 5V/div at a 400μs/div time scale.

Note the average voltage waveforms in Figure 4-13 are sinusoidal with a fundamental frequency of 600Hz and 120° apart. These sinusoidal voltages produce the sinusoidal current waveforms in Figure 4-2.

THREE PHASE VOLTAGE WAVEFORMS AT 1200HZ

Figure 4-14 and Figure 4-15 demonstrate the phase-to-neutral switching voltage waveforms and the phase-to-neutral average voltage waveforms, respectively. Like Figure 4-11, the average voltage waveforms in Figure 4-15 do not resemble the ideal

Figure 4-14: Phase-to-neutral switching voltage waveforms at 1200Hz. Phase 1 (top), phase 2 (middle), and phase 3 (bottom) were measured with the oscilloscope set to 5V/div at a 200µs/div time scale. Notice there is little meaningful data to extract but it is presented as a comparison to the filtered data in Figure 4-15.

space vector average voltage waveform in Figure 4-5. Since the PWM frequency is 20kHz and the fundamental frequency is 1200Hz, one period of the average phase-to-neutral voltage waveform is constructed using only 16 PWM cycles, again unable to

produce the ideal space vector average voltage. Figure 4-15 is also affected by the filter's time constant ($\tau = 100\mu\text{s}$).

Figure 4-15: Phase-to-neutral average voltage waveforms at 1200Hz. The waveforms were generated by filtering Figure 4-14 through a low-pass filter with a time constant of $100\mu\text{s}$. Phase 1 (top), phase 2 (middle), and phase 3 (bottom) have a fundamental frequency of 1200Hz and are 120° apart. The oscilloscope is set to 2V/div at a $200\mu\text{s}/\text{div}$ time scale.

Figure 4-16 and Figure 4-17 show the phase-to-phase switching voltage waveforms and the phase-to-phase average voltage waveforms, respectively. Note the average voltage waveforms in Figure 4-17 are sinusoidal with a fundamental frequency of 1200Hz and 120° apart. These sinusoidal voltages produce the sinusoidal current waveforms in Figure 4-3.

Figure 4-16: Phase-to-phase switching voltage waveforms at 1200Hz. Phase 1-2 (top), phase 2-3 (middle), and phase 3-1 (bottom) were measured with the oscilloscope set to 10V/div at a 200μs/div time scale.

Figure 4-17: Phase-to-phase average voltage waveforms at 1200Hz. The waveforms were generated by filtering Figure 4-16 through a low-pass filter with a time constant of 100μs. Phase 1-2 (top), phase 2-3 (middle), and phase 3-1 (bottom) have a fundamental frequency of 60Hz and are 120° apart. The oscilloscope is set to 5V/div at a 200μs/div time scale.

DC BUS VOLTAGE AND DC BUS CURRENT STABILITY

In order for the VFD design to work properly, a stable DC bus is necessary.

Figure 4-18 shows that the DC bus voltage and current were stable while the VFD was operating at 1200Hz.

Figure 4-18: One-half the DC bus voltage (top) and DC bus currents (bottom) at 1200Hz. One side of the two-sided DC bus voltage was measured to be 56VDC, [20V/div]. The current ripple is approximately 3mA peak-to-peak, [1A/div].

V/HZ DATA

The V/Hz plot is presented in Figure 4-19. Notice the plot is not linear in the range of 200Hz to 300Hz. Due to voltage supply limitations, the motor could not run at frequencies above 200Hz. As the back EMF decreased, the phase-to-phase voltage decreased, resulting in the observed voltage drop. At a speed much below the synchronous speed, the motor reached steady state. At this steady state speed, the voltage became linear. The plot supports the claim that the V/Hz method is properly implemented.

Figure 4-19: V/Hz data collected.

PWM SIGNALS

Figure 4-20 shows the symmetric PWM signals generated by the DSP, using the space vector technique. Figure 4-21 presents the PWM signals at the output of the DC-AC inverter. Figure 4-22 demonstrates the dead-band used to prevent shoot-through.

Figure 4-20: Symmetric 20kHz PWM generation. This PWM signal was measured at the output of the controller. PWM1 (top), PWM3 (middle), and PWM5 (bottom) were measured with the oscilloscope set to 5V/div on a 10μs/div time scale.

Figure 4-21: PWM signals were collected at the output of the DC-AC inverter. PWM1 (top), PWM3 (middle), and PWM5 (bottom) are Van', Vbn', and Vcn', respectively, where n' is the joint of the split supply. Refer to Figure 2-5. The oscilloscope was set to 50V/div on a 50μs/div time scale

Figure 4-22: Dead-band. For this design, the opto-isolators are integrated such that the PWM signal is active low. The dead-band time is implemented so that the complementary PWM signals are never low at the same time. Per the IPM data sheet, the dead-band time is set to 2.5μs. PWM1 (top) and PWM2 (bottom) were measured with the oscilloscope set to 2V/div on a 5μs/div time scale.

CHAPTER 5: CONCLUSION

SUMMARY

This variable frequency drive design, using the constant V/Hz principle and symmetric, space vector generated PWM signals, varied a 3-phase output from 0Hz to 1200Hz, while maintaining constant current. The 3-phase voltage outputs produce sinusoidal currents through the windings of an AC induction motor. Due to budgetary constraints, a permanent magnet AC motor could not be procured for testing.

A DSP controller and Intelligent Power Module incorporated much of the hardware necessary to generate the variable frequencies without any additional hardware design. Many design characteristics, including V/Hz, space vector PWM, and symmetric PWM are implemented in the program for the DSP.

The experimental data presented in the previous section shows that the realized design was operational and performed well. Figures 4-1 to 4-3 present the current waveforms, at the output of the DC-AC inverter, for three AC line frequencies: 60Hz, 600Hz, and 1200Hz. The inverter supplies power to a 208VAC motor. The current remains constant across the line frequency spectrum. This indicates the V/Hz method is properly implemented in the DSP controller. In addition, notice the current waveforms are sinusoidal and spaced 120° apart. This indicates the PWM methodology is properly implemented.

Figure 4-4 presents one-half current cycle of one leg of the inverter. The AC line frequency is 500Hz. Although it is not very clear, the switching waveform can be seen

on the fundamental AC waveform. Due to the large stator inductance of the motor, it is difficult to see clearly.

The average phase-to-phase voltage waveforms for three AC line frequencies: 60Hz, 600Hz, and 1200Hz are presented in Figure 4-9, Figure 4-13, and Figure 4-17, respectively. Notice the average phase-to-phase voltage waveforms are sinusoidal and spaced 120° apart. These voltage waveforms produce the sinusoidal waveforms of Figures 4-1 to 4-3.

DC bus stability was a challenge to meet with this VFD design. To achieve a stable DC bus, 2,301 μF was required for each rail of the power supply. The bus stability is presented in Figure 4-18. Notice the current ripple is only 3mA peak-to-peak.

The V/Hz plot is presented in Figure 4-19. Notice the plot is not linear in the range of 200 - 300Hz. Due to voltage supply limitations, the motor could not run at frequencies above 200Hz. As the back EMF decreased, the phase-to-phase voltage decreased resulting in the observed voltage drop. Once the motor reached a steady state, the voltage became linear. The plot supports the claim that the V/Hz method is properly implemented.

LESSONS LEARNED

Use shielded cables for all I/O and communication. The VFD initial design did not consistently contain shielded cables. Therefore, some time was lost diagnosing random faults. The faults were traced back to noise coupling into the communication lines.

VFD DC voltage bus should have provisions for the installation of a number of energy storage capacitors. The initial VFD design contained space for approximately two 100 μ F capacitors. To get reasonable DC bus stability, considerable additional capacitance was required. The design inadequacies made it very difficult to add the additional storage capacitors.

When making voltage and/or current measurements using an oscilloscope, be sure to place the probe grounds carefully for proper measurements. In addition, to prevent scope measurement ground faults, be sure to "float" the oscilloscope by plugging the oscilloscope into a 2-prong adapter that prevents the oscilloscope's ground from being connected to earth ground.

SUGGESTIONS FOR FUTURE WORK

The variable frequency speed drive designed in this thesis could be improved as suggested below.

IMPLEMENTING MOTOR FEEDBACK

This design operates the VFD in an open loop mode. Properly closing the loop with position feedback from an encoder or monitoring the sinusoidal current in Field Oriented Control (FOC) would ensure a more precisely controlled speed.

Encoder

Using encoder feedback would extend the VFD design to brushless DC (BLDC) motors. The interrupt service routine requires only 250ns to complete. Therefore, there is plenty of overhead time to implement the feedback. Texas Instruments has many

application documents on this subject. Their website at www.ti.com is a good source for information for implementing encoder feedback on the TMS320F240 DSP.

Field Oriented Control

Texas Instruments also has application documents for field oriented control (FOC). This method monitors two of the three phases and controls the power to the motor based on this measurement. A good source for implementing FOC is also at Texas Instruments' website at www.ti.com.

RELIABILITY STUDY

The design outlined in this thesis focused on research and development applications. The intended users of the design are engineers that understand the principles and limitations of the design. The design could be improved upon by uncovering the design weaknesses and making it more robust through further testing.

Some of the design weaknesses are as follows:

1. Connectors are under-rated
2. DC input and AC output wire is slightly under rated
3. DC voltage bus does not properly support the addition of storage capacitors
4. The IPM fault outputs are not monitored by the DSP controller
5. The IPM could be replaced by a model with increased power capabilities

Safety features could be implemented for the user and future engineers that modify or build upon this design. Simple changes might include measurement breakouts

so users do not have to put their hands or face in a high voltage area to take measurements.

SOFTWARE USER INTERFACE

Currently the interface to operate this design requires the user to understand how the design works. A user interface program could be developed to make it easier to control the frequency of the 3-phase output. The evaluation module that is used as the controller has a serial port that could communicate to another computer.

STAND-ALONE UNIT WITH PROM

The VFD currently loses the program in the DSP every time the power is cycled to the processor. A PROM (Programmable Read Only Memory) interface could be designed, which would allow engineers developing new power conversion techniques to cycle the power to the DSP without downloading the program.

OUTPUT FILTER TOPOLOGIES

Higher PWM frequencies are becoming more common as power electronics are improved. As the switching frequency is increased, control improves. The higher switching frequencies have a negative effect on the motor side. “High frequency inverters have been shown to contribute to premature winding failures and bearing currents. High dv/dt applied to the motor windings excite the parasitic coupling capacitances that produce bearing currents and contribute to electromagnetic compatibility concerns.” (Sozer et al. 2000) Filter topologies could be researched and characterized using the VFD presented in this thesis.

PERFORMING ANALYSIS OF CODE TO REAL VALUES

An analysis could be performed that would extract the values of the variables and transform them into real values that are understood and relate directly to the parameters of the motor, such as air gap flux, stator voltage, and excitation frequency. A special utility to extract the data would need to be created. The data could then be used to analyze the performance of the variable frequency drive. This would be most beneficial for a closed loop implementation where the control parameters could be “tuned” to enhance the performance of the motor.

REFERENCES

- Aller, José M., Alexander Bueno, Tomás Pagá, José A. Restrepo, Victor M. Guzmán, and Maria I. Giménez. 2000. Space Vector Applications in Power Systems. *Proceedings of the 2000 Third IEEE International Caracas Conference on Devices, Circuits and Systems*, 2000, P78/1 -P78/6.
- Baliga, B. Jayant. 1994. Power Semiconductor Devices for Variable-Frequency Drives. *Proceedings of the IEEE*, August 1994, Vol. 82: No 8: 1112-1122.
- Bonnet, A., T Alukaiday, P. C. K. Luk. 1997. A High Performance Space Vector Motor Controller. *DSP Chips in Real Time Measurement and Control*, September 25, 1997, 4/1-4/4.
- Born, Peter. 2000, Pros and Cons of Isolated and Non-Isolated DC-DC Converters. *PCIM*, October 2000, 92-93
- Holtz, J. 1997. *Electric Machines for Drives*. Edited by Bimal K. Bose. *Pulse Width Modulation for Electronic Power Conversion*. New York: IEEE Press.
- Mohan, Ned, Tore M. Undeland, and William P. Robbins. 1995. *Power Electronics Converters, Applications, and Design*. New York: John Wiley & Sons, Inc.
- Phipps, Clarence A. 1994. *Variable Speed Drive Fundamentals*. Lilburn, GA: The Fairmont Press, Inc.
- Pinto, Joao O., Bimal K. Bose, Luiz Eduardo Borges da Silva, and Marian P. Kazmierkowski. 2000. A Neural-Network-Based Space-Vector PWM Controller for Voltage-Fed Inverter Induction Motor Drive. *IEEE Transactions on Industry Applications*, November/December 2000, Vol. 36: No. 6: 1628-1636.
- Sleman, Gordon R. 1994. Electrical Machines for Variable-Frequency Drives. *Proceedings of the IEEE*, August 1994, Vol. 82: No 8: 1123-1139.
- Sozer, Yilmaz, David A. Torrey, and Suhan Reva. 2000. New Inverter Output Filter Topology for PWM Motor Drives. *Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2000*, Vol. 2: 911 -917.
- Texas Instruments. 1997. TMS320C24x DSP Controllers Evaluation Module, Texas Instruments. Technical Reference SPRU248A.
- Texas Instruments. 1999. TMS320F/C24x DSP Controllers CPU and Instruction Set. Reference Guide SPRU160C.

Texas Instruments. 1999. TMS320F/C24x DSP Controllers Peripheral Library and Specification Devices. Reference Guide SPRU161C.

Yu, Zhenyu and David Figoli. 1998. AC Induction Motor Control Using Constant V/Hz Principle and Space Vector PWM Technique with TMS320C240, Texas Instruments Application Report: SPRA284A.

APPENDICES

APPENDIX A: REFERENCE INTERNET SITES

VARIABLE FREQUENCY DRIVE MICRO-CONTROLLERS

Table A-1 provides a list of DSP controller suppliers who offer development systems as part of their product line. Development systems provide a complete system for prototyping and characterization efforts. In addition, these sites provide technical papers addressing code development.

Table A-1: DSP Controller Suppliers Providing Development Systems

Item	Supplier & P/N	Processor Description	Website
1	Analog Devices ADMC300	25-MHz, Fixed-point DSP 16-bit data 24-bit instruction	www.analog.com
2	Hitachi SH7040	28.7-MHz, 32-bit RISC core Hardware MAC	www.hitachi.com
3	Motorola MC68HC708MP16	8-MHz 8-bit CPU08 core	www.mot.com
4	SGS Thomson ST10F166	20-MHz 16-bit ST10 core	www.st.com
5	Texas Instruments TMS320C240	20-MHz Fixed-point DSP	www.ti.com

INTELLIGENT POWER MODULES

Table A-2 presents the manufacturers of Intelligent Power Modules. Powerex no longer make their own IPMs, but rather markets Mitsubishi's IPM products in the United States. Mitsubishi still markets their own IPMs in other countries.

Table A-2: Intelligent Power Module Supplier Reference

Item	Manufacturer	Product Range	Website
1	Fuji	4 - 7 IGBT packages 15 - 300A 450 - 900V	www.collmer.com/fuji_ipm
2	International Rectifier	3 IGBT package 15A 230V	www.irf.com
3	Mitsubishi	1 - 7 IGBT packages 10 - 800A 600 - 1200V	www.mitsubishichips.com
4	Powerex	1 - 7 IGBT packages 10 - 800A 600 - 1200V	www.pwr.com
5	Toshiba	3 - 7 IGBT packages 20 - 300A 600 - 1200V	www.toshiba.com
6	Tyco	1 - 3 IGBT packages 5 - 30 A 600 - 1200V	www.siemens.com

VARIABLE FREQUENCY DRIVE SUPPLIER REFERENCE

Table A-3 presents suppliers offering variable frequency drives. Many of these drives are integrated as part of the motor.

Table A-3: Variable Frequency Drive Supplier Reference

Item	Manufacturer	Product Description	Website
1	AC Technology	V/Hz Control Frequency range: 0 - 99 Max voltage input: 240 VAC	www.actechdrives.com
2	Acumentrics	Vector Control Frequency range: 0 - 700 Max voltage input: 300 VDC	www.acumentrics.com
3	Baldor	Vector Control Frequency range: 0 - 120 Max voltage input: 240 VAC	www.baldor.com
4	Danfoss	V/Hz Control Frequency range: 28 - 90 Max voltage input: 240 VAC	www.danfoss.com
5	Cleveland Motion	Vector Control Frequency range: 0 - 480 Max voltage input: 240 VAC	www.cmcccontrols.com
6	Warner Electric	V/Hz Control Frequency range: 6 - 120 Max voltage input: 230 VAC	www.warnernet.com
7	IMD	V/Hz Control Frequency range: 10 - 90 Max voltage input: 240 VAC	www.imd.com
8	Trace Technologies	Vector Control Frequency range: 0 - 120 Max voltage input: 240 VAC	www.tracetech.com

APPENDIX B: DSP SURVEY RESULTS

Table B-1: Survey of DSPs

Manufacturer and Part Number	Processor Structure	Features	PWM Capabilities	Other Features	Development Board Price
Analog Devices ADMC300	<ul style="list-style-type: none"> 25-MHz Fixed-point DSP 16-bit data 24-bit instruction 	<ul style="list-style-type: none"> 4-kbyte program RAM 2-kbyte ROM 1-kbyte data RAM 5x16-bit ADCs Incremental encoder interface 12-bit I/O port Event, interval, and watch-dog timers Two SCI UARTs 	<ul style="list-style-type: none"> 3-phase, 12-bit center aligned Programmable dead-time 80-nsec edge detection 3.05-kHz at 12-bit to 48.8-kHz at 8-bit resolution 	<ul style="list-style-type: none"> Debugger in ROM Motor/math functions On-line support Limited application docs 	<ul style="list-style-type: none"> \$395.00 ADMCF 326
Hitachi SH7040	<ul style="list-style-type: none"> 28.7-MHz 32-bit RISC core Hardware MAC 	<ul style="list-style-type: none"> 64-kbyte ROM 4-kbyte RAM 8x10-bit ADC 2 S/H, 2-phase encoder interface 5x16-bit timers 2x16-bit interval timers Two UARTs 	<ul style="list-style-type: none"> 6-phase, 10-bit Automatic dead-time generation 20-kHz carrier frequency, 35-nsec resolution 	<ul style="list-style-type: none"> 32x32-bit multiply Limited support and application docs 	<ul style="list-style-type: none"> N/A
Motorola MC68HC708 MP16	<ul style="list-style-type: none"> 8-MHz 8-bit CPU08 core 	<ul style="list-style-type: none"> 16-kbyte ROM/EPROM 512-byte RAM 10x8-bit ADC Two timer blocks 4-SPI, 2-SCI I/Os, 13-I/O ports 	<ul style="list-style-type: none"> 3-phase, 250-nsec resolution for center, 125-nsec edge-aligned Programmable dead-time, current-sense for dead-time compensation 	<ul style="list-style-type: none"> On-line support Limited application docs 	<ul style="list-style-type: none"> N/A
SGS Thomson ST10F166	<ul style="list-style-type: none"> 20-MHz 16-bit ST10 core 	<ul style="list-style-type: none"> 32-kbyte flash EPROM 1-kbyte RAM 512-byte register file 10x10-bit ADCs 5x16-bit timers, watch-dog timer Two UARTs, 76-I/Os 	<ul style="list-style-type: none"> General-purpose capture/compare unit 16-channels, 400-nsec resolution Two auto-reload registers 	<ul style="list-style-type: none"> Assembler and linker emulation 	<ul style="list-style-type: none"> N/A
Texas Instruments TMS320C240	<ul style="list-style-type: none"> 20-MHz Fixed-point DSP 	<ul style="list-style-type: none"> 16-kbyte ROM/EEPROM 544-word program/data RAM 2x10-bit ADCs Quadrature encoder interface PLL clock generator, watch-dog timer, event-manager module Four SCI / two SPI serial interfaces, 28-I/O 	<ul style="list-style-type: none"> 12 compare/PWM channels Programmable dead-time 16-bit, 50-nsec resolution Programmable PWM waveforms 	<ul style="list-style-type: none"> Debugger in ROM Assembler and linker emulation On-line support Good application docs 	<ul style="list-style-type: none"> \$1,700.00 TMDX3 26P124 X

APPENDIX C: EVALUATION MODULE

Figure C-1: Evaluation module for the TMS320F240 DSP from Texas Instruments. (Texas Instruments 1997)

APPENDIX D: POWEREX IPM DATA SHEET

This data sheet is readily available on the Internet at www.pwrX.com.

POWEREX

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15687-1800 (724) 626-7272

PM100CVA060

Intellimod™ Module
Three Phase
IGBT Inverter Output
100 Amperes/600 Volts

Description:
Powerex Intellimod™ Intelligent Power Modules are isolated base modules designed for power switching applications operating at frequencies to 20kHz. Built-in control circuits provide optimum gate drive and protection for the IGBT and free-wheel diode power devices.

- Features:**
- Complete Output Power Circuit
 - Gate Drive Circuit
 - Protection Logic
 - Short Circuit
 - Over Temperature
 - Under Voltage

- Applications:**
- Inverters
 - UPS
 - Motion/Servo Control
 - Power Supplies

Ordering Information:
Example: Select the complete part number from the table below - i.e. PM100CVA060 is a 600V, 100 Ampere Intellimod™ Intelligent Power Module.

Type	Current Rating Amperes	V _{CE} Volts (x 10)
PM	100	60

Dimensions	Inches	Millimeters
A	4.33	110.0
B	3.50	89.0
C	0.87 ±0.04/-0.02	22.0 ±1.0/-0.5
D	3.74 ±0.010	95.0 ±0.25
E	2.91 ±0.010	74.0 ±0.25
F	0.16	4.0
G	0.87	22.0
H	0.42	10.6
J	0.79	20.0
K	2.09 ±0.02	53.0 ±0.5
L	0.39	10.0
M	0.49	12.5
N	0.67	17.0

Dimensions	Inches	Millimeters
P	0.30	7.5
R	0.65	16.5
S	M5 Metric	M5
T	0.22 Dia.	Dia. 5.5
U	0.56 ±0.010	14.1 ±0.25
V	1.72 ±0.012	43.57 ±0.3
W	0.57 ±0.012	14.6 ±0.3
X	2.90	73.7
Y	0.78	19.7
Z	0.10 ±0.010	2.54 ±0.25
AA	0.137 ±0.010	3.49 ±0.25
BB	0.02 SQ	0.64 SQ
CC	0.12 ±0.04/-0.02	3.0 ±1.0/-0.5

Powerex, Inc., 200 Mills Street, Youngwood, Pennsylvania 15687-1800 (724) 825-7272

PM100CYA060

Intellimod™ Module

Three Phase IGBT Inverter Output

100 Amperes/600 Volts

Absolute Maximum Ratings, $T_J = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	PM100CYA060	Units
Power Device Junction Temperature	T_J	-20 to 150	°C
Storage Temperature	T_{stg}	-40 to 125	°C
Case Operating Temperature	T_C	-20 to 100	°C
Mounting Torque, M5 Mounting Screws (Typical)	—	17	in-lb
Mounting Torque, M5 Main Terminal Screws (Typical)	—	17	in-lb
Module Weight (Typical)	—	560	Grams
Supply Voltage, Surge (Applied between P - N, Surge Value)	$V_{CC(surge)}$	500	Volts
Supply Voltage Protected by SC ($V_D = 13.5 - 16.5\text{V}$, Inverter Part, $T_J = 125^\circ\text{C}$ Start)	$V_{CC(prot.)}$	400	Volts
Isolation Voltage, AC 1 minute, 60Hz Sinusoidal	V_{RMS}	2500	Volts

Control Sector

Supply Voltage Applied between ($V_{UP1}-V_{UPC}$, $V_{VP1}-V_{VPC}$, $V_{WP1}-V_{WPC}$, $V_{N1}-V_{NC}$)	V_D	20	Volts
Input Voltage Applied between (U_P , V_P , W_P , U_N , V_N , W_N)	V_{CIN}	20	Volts
Fault Output Supply Voltage (Applied between F_D , V_{NC} , F_D , V_{PC})	V_{FO}	20	Volts
Fault Output Current (Sink Current at F_D Terminals)	I_{FO}	20	mA

IGBT Inverter

Collector-Emitter Voltage ($V_{CE} = 15\text{V}$, $V_{CIN} = 15\text{V}$)	V_{CES}	600	Volts
Collector Current, $\pm$ ($T_C = 25^\circ\text{C}$)	I_C	100	Amperes
Peak Collector Current, $\pm$ ($T_C = 25^\circ\text{C}$)	I_{CP}	200	Amperes
Collector Dissipation ($T_C = 25^\circ\text{C}$)	P_C	338	Watts

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PM10SCVA060

IntelliMod™ Module

Three Phase IGBT Inverter Output

100 Amperes/600 Volts

Electrical and Mechanical Characteristics, $T_J = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Control Sector						
Short Circuit Trip Level	SC	$-20^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, $V_D = 15\text{V}$	158	—	—	Amperes
Short Circuit Current Delay Time	$t_{d(SC)}$	$V_D = 15\text{V}$	—	10	—	μs
Over Temperature Protection	OT	Trip Level	100	110	120	$^\circ\text{C}$
($V_D = 15\text{V}$)	OT_r	Reset Level	85	95	105	$^\circ\text{C}$
Supply Circuit Under Voltage Protection	UV	Trip Level	11.5	12.0	12.5	Volts
($-20^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$)	UV_r	Reset Level	—	12.5	—	Volts
Circuit Current	I_J	$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$, $V_{N1} = V_{NC}$	—	40	55	mA
		$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$, $V_{XP1} = V_{XPC}$	—	13	18	mA
Input ON Threshold Voltage	$V_{CIN(on)}$	Applied between $U_p - V_{UPC}$, $V_p - V_{VPC}$	1.2	1.5	1.8	Volts
Input OFF Threshold Voltage	$V_{CIN(off)}$	$W_p - V_{WPC}$, U_N , V_N , $W_N - V_{NOC}$	1.7	2.0	2.3	Volts
Fault Output Current	$I_{FO(H)}$	$V_D = 15\text{V}$, $V_{FO} = 15\text{V}$	—	—	0.01	mA
	$I_{FO(L)}$	$V_D = 15\text{V}$, $V_{FO} = 15\text{V}$	—	10	15	mA
Minimum Fault Output Pulse Width	t_{FO}	$V_{FO} = 15\text{V}$	1.0	1.8	—	mS

Powerex, Inc., 200 Mills Street, Youngwood, Pennsylvania 15087-1888 (724) 825-7272

PM100CVA000
Intellimod™ Module
Three Phase IGBT Inverter Output
100 Amperes/600 Volts

Electrical and Mechanical Characteristics, $T_j = 25^\circ\text{C}$ unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
IGBT Inverter Sector						
Collector-Emitter Cutoff Current	I_{CES}	$V_{CE} = V_{CES}, V_D = 15\text{V}, T_j = 25^\circ\text{C}$	—	—	1.0	mA
		$V_{CE} = V_{CES}, V_D = 15\text{V}, T_j = 125^\circ\text{C}$	—	—	10.0	mA
FWD _i Forward Voltage	V_{EC}	$-I_C = 100\text{A}, V_D = 15\text{V}, V_{CIN} = 15\text{V}$	—	2.20	3.30	Volts
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$V_D = 15\text{V}, V_{CIN} = 0\text{V}, I_C = 100\text{A}$	—	2.35	2.80	Volts
		Pulsed, $T_j = 25^\circ\text{C}$	—	2.55	3.05	Volts
		$V_D = 15\text{V}, V_{CIN} = 0\text{V}, I_C = 100\text{A}$	—	2.55	3.05	Volts
Inductive Load Switching Times (Upper/Lower Arm)	t_{PI}	$V_D = 15\text{V}, V_{CIN} = 0\text{V} - 15\text{V}$ $V_{CC} = 300\text{V}, I_C = 100\text{A}$ $T_j = 125^\circ\text{C}$	0.4	0.8	2.1	μS
	t_{rr}		—	0.2	0.3	μS
	$t_{C(on)}$		—	0.3	1.1	μS
	t_{off}		—	1.9	2.9	μS
	$t_{C(off)}$		—	0.6	1.2	μS

Thermal Characteristics

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Units
Junction to Case Thermal Resistance	$R_{\theta(j-c)}$	Each Inverter IGBT	—	—	0.37	C/Watt
	$R_{\theta(j-c)}$	Each Inverter FWD _i	—	—	0.70	C/Watt
Contact Thermal Resistance	$R_{\theta(c-f)}$	Case to Fin Per Module. Thermal Grease Applied	—	—	0.027	C/Watt

Recommended Conditions for Use

Characteristics	Symbol	Condition	Value	Units
Supply Voltage	V_{CC}	Applied across P-N Terminals	≤ 400	Volts
	$V_{CE(surge)}$	Applied across Terminals	≤ 500	Volts
		P-U, P-V, P-W, U-N, V-N, W-N		
	V_{DJ}	Applied between $V_{UP1}-V_{JHC}$, $V_{N1}-V_{NHC}$, $V_{WP1}-V_{WPC}$, $V_{WP1}-V_{WPC}$	± 1.5	Volts
Input ON Voltage	$V_{CIN(on)}$	Applied between $U_p, V_n, W_p, U_n, V_n, W_n$	≤ 0.8	Volts
Input OFF Voltage	$V_{CIN(off)}$		≥ 4.0	Volts
Arm Shoot-Through Blocking Time	t_{DEAD}	For IPW's each input signal	≥ 2.5	μS

POWEREX

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PM100CVA080

Intellimod™ Module

Three Phase IGBT Inverter Output
100 Amperes/800 Volts

POWEREX

Powerex, Inc., 200 Mills Street, Youngwood, Pennsylvania 15897-1800 (724) 925-7272

PM100CVA089

Intellimod™ Module

Three Phase IGBT Inverter Output

100 Amperes/800 Volts

APPENDIX E: DSP TO IPM INTERFACE BOARD SCHEMATIC

OPTO-ISOLATOR INTERFACE TO IPM

APPENDIX F: OPTO-ISOLATOR DATA SHEETS

AGILENT TECHNOLOGIES HCPL-4504

This data sheet is readily available on the Internet at www.agilent.com.

High CMR, High Speed Optocouplers

Technical Data

HCPL-4504
HCPL-J454
HCPL-0454
HCNW4504

Features

- **Short Propagation Delays for TTL and IPM Applications**
- **15 kV/ μ s Minimum Common Mode Transient Immunity at $V_{CM} = 1500$ V for TTL/Load Drive**
- **High CTR at $T_A = 25^\circ\text{C}$**
 $>25\%$ for HCPL-4504/0454
 $>23\%$ for HCNW4504
 $>19\%$ for HCPL-J454
- **Electrical Specifications for Common IPM Applications**
- **TTL Compatible**
- **Guaranteed Performance from 0°C to 70°C**
- **Open Collector Output**
- **Safety Approval UL Recognized**
 - 2500 V rms / 1min. for HCPL-4504/0454
 - 3750 V rms / 1min. for HCPL-J454
 - 5000 V rms / 1min. for HCPL-4504 Option020 and HCNW4504

CSA Approved
BSI Certified (HCNW4504)
VDE884 Approved

- $V_{D-SM} = 560$ Vpeak for HCPL-0454 Option060
- $V_{D-SM} = 630$ Vpeak for HCPL-4504 Option060

- $V_{RDM} = 891$ Vpeak for HCPL-J454
- $V_{RDM} = 1414$ Vpeak for HCNW4504

Applications

- **Inverter Circuits and Intelligent Power Module (IPM) interfacing** - High Common Mode Transient Immunity (> 10 kV/ μ s for an IPM load/drive) and ($t_{PLH} - t_{FRL}$) Specified (See Power Inverter Dead Time section)
- **Line Receivers** - Short Propagation Delays and Low Input-Output Capacitance
- **High Speed Logic Ground Isolation - TTL/TTL, TTL/CMOS, TTL/LSTTL**

- **Replaces Pulse Transformers** - Save Board Space and Weight
- **Analog Signal Ground Isolation** - Integrated Photodetector Provides Improved Linearity over Phototransistors

Description

The HCPL-4504 and HCPL-0454 contain a GaAsP LED while the HCPL-J454 and HCNW4504 contain an AlGaAs LED. The LED is optically coupled to an integrated high gain photo detector.

The HCPL-4504 series has short propagation delays and high CTR. The HCPL-4504 series also has a guaranteed propagation delay difference ($t_{PLH} - t_{FRL}$). These

Functional Diagram

A 0.1 μ F bypass capacitor between pins 5 and 6 is recommended.

TRUTH TABLE	
LED	V_O
ON	LOW
OFF	HIGH

CUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

features make the HCPL-1504 series an excellent solution to IPM inverter dead time and other switching problems. The CTR, propagation delay, and CMR are specified both for TTL and IPM conditions which are provided for ease of application. These single channel, diode-transistor optocouplers are available in 8-Pin DIP, SO-8, and Widebody

package configurations. An insulating layer between a LED and an integrated photodetector provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base collector capacitance.

Selection Guide

Package Type	Standard 8-Pin DIP (300 Mil)	White Mold 8-Pin DIP (300 Mil)	Small Outline SO8	Widebody (400 Mil)
Part Number	HCPL-1504	HCPL-J154	HCPL-0154	HCNW1504
VDE0884 Approval	$V_{DSM} = 630 \text{ Vpeak}$ (Option 060)	$V_{DSM} = 891 \text{ Vpeak}$	$V_{DSM} = 560 \text{ Vpeak}$ (Option 060)	$V_{DSM} = 1411 \text{ Vpeak}$

Ordering Information

Specify Part number followed by Option Number (if desired)

Example

HCPL-1504 #XXX

- 020 = 11,500 Vrms/Minute Option* for HCPL-1504 Only.
- 060 = VDE0884 Option* for HCPL-1504/J154.
- 300 = Gull-Wing Lead Option for HCPL-1504/J154, HCNW1504.
- 500 = Tape and Reel Packaging Option.

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor for information.

* Combination of Option 020 and Option 060 is not available.

Schematic

Package Outline Drawings

HCPL-4504 and HCPL-J454 Outline Drawing

HCPL-4504 and HCPL-J454 Gull Wing Surface Mount Option 300 Outline Drawing

HCPL-0434 Outline Drawing (8-Pin Small Outline Package)

HCNW4504 Outline Drawing (8-Pin Widebody Package)

HCNW4504 Gull Wing Surface Mount Option 300 Outline Drawing

Solder Reflow Temperature Profile (HCPL-0454 and Gull Wing Surface Mount Option Parts)

Note: Use of nonchlorine activated fluxes is highly recommended.

Regulatory Information

The devices contained in this data sheet have been approved by the following agencies:

Agency/Standard	HCPL-4504	HCPL-J454	HCPL-0456	HCNW4504
Underwriters Laboratories (UL) Recognized under UL1577, Component Recognition Program, Category FTQ/2, File E55361	✓	✓	✓	✓
Canadian Standards Association (CSA) Component Acceptance Notice #5 File CA88324	✓	✓	✓	✓
Verband Deutscher Elektrotechniker (VDE) DIN VDE 0884 (June 1992)	✓	✓		✓
Technischer Überwachungs-Verein Rheinland (TUV) Certificate R9650938 DIN VDE 0884 (June 1992)			✓	
British Standards Institute (BSI) Certification according to BS EN60065: 1994(BS415:1994), BS EN60050: 1992(BS7002:1992), and IEC 65(1985).				✓

Insulation and Safety Related Specifications

Parameter	Symbol	Value				Units	Conditions
		HCPL-4504	HCPL-J454	HCPL-0454	HCNW4504		
Minimum External Air Gap (External Clearance)	L(101)	7.1	7.4	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	8.0	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.5	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photomitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 175	≥ 175	≥ 175	≥ 200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Hewlett-Packard data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements.

However, once mounted on a printed circuit board, minimum

creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and

ridges which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

VDE 0884 Insulation Related Characteristics

Description	Symbol	HCPL-0434 OPTION 000	HCPL-0504 OPTION 000	HCPL-J434	HCNW4504	Unit
Installation classification per DIN VDE 0110/1:89, Table 1 for rated mains voltage ≤ 150 V rms for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 450 V rms for rated mains voltage ≤ 600 V rms for rated mains voltage ≤ 1000 V rms		I-IV I-III	I-IV I-IV I-III	I-IV I-IV I-III	I-IV I-IV I-IV I-IV I-III	
Climate Classification		55/100/21	55/100/21	55/100/21	55/85/21	
Pollution Degree (DIN VDE 0110/1:89)		2	2	2	2	
Maximum Working Insulation Voltage	V_{MWS}	500	600	800	1414	V _{rms}
Input to Output Test Voltage, Method b* $V_{\text{MWS}} \times 1.875 = V_{\text{PZ}}$, 100% Production Test with $t_{\text{PZ}} = 1$ sec, Partial Discharge < 5 pC	V_{PZ}	1050	1181	1670	2652	V _{rms}
Input to Output Test Voltage, Method a* $V_{\text{MWS}} \times 1.5 = V_{\text{PZ}}$, Type and Sample Test, $t_{\text{PZ}} = 60$ sec, Partial Discharge < 5 pC	V_{PZ}	840	945	1330	2121	V _{rms}
Highest Allowable Overvoltage* (Transient Overvoltage, $t_{\text{m}} = 10$ sec)	V_{ADM}	1000	6000	6000	8000	V _{rms}
Safety Limiting Values - Maximum Values Allowed in the Event of a Failure, also see Thermal Derating curve Case Temperature Input Current Output Power	T_{S} $I_{\text{A,B,SC}}$ $P_{\text{S,OUT,TRT}}$	150 150 600	175 250 600	175 400 600	150 500 700	°C mA mW
Insulation Resistance at T_{A} , $V_{\text{AD}} = 500$ V	R_{A}	$\geq 10^9$	$\geq 10^9$	$\geq 10^9$	$\geq 10^9$	Ω

*Refer to the opt. coupler section of the Designer's Catalog, under regulatory information (VDE 0884) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

NOTE: Insulation Characteristics are per DIN VDE 0884 (June 1992 revision).

NOTE: Surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	$^{\circ}\text{C}$	
Operating Temperature	T_A	HCPL-4504 HCPL-0454 HCPL-4454 HCNW4504	-55	100	$^{\circ}\text{C}$	
Average Forward Input Current	$I_{F(AVG)}$			25	mA	1
Peak Forward Input Current (50% duty cycle, 1 μs pulse width)	$I_{F(PEAK)}$	HCPL-4504 HCPL-0454 HCPL-4454 HCNW4504		50 40	mA	2
Peak Transient Input Current ($\leq 1 \mu\text{s}$ pulse width, 300 pps)	$I_{F(TRANS)}$	HCPL-4504 HCPL-0454 HCPL-4454 HCNW4504		1 0.1	A	
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4504 HCPL-0454 HCPL-4454 HCNW4504		5 3	V	
Input Power Dissipation	P_{IN}	HCPL-4504 HCPL-0454 HCPL-4454 HCNW4504		45 40	mW	3
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pin 6-5)	V_O		-0.5	20	V	
Output Power Dissipation	P_O			100	mW	4
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds Up to seating plane, 10 seconds	T_{LS}	HCPL-4504 HCPL-0454 HCNW4504		260 260	$^{\circ}\text{C}$	
Reflow Temperature Profile	T_{RP}	HCPL-0454 and Option 300	See Package Outline Drawings section			

Electrical Specifications (DC)Over recommended temperature ($T_A = 0^\circ\text{C}$ to 70°C) unless otherwise specified. See note 12.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL4501	25	32	60	%	$T_A = 25^\circ\text{C}$ $V_{CE} = 0.1\text{ V}$ $I_F = 10\text{ mA}$ $V_{CE} = 4.5\text{ V}$	1, 2, 4	5
		HCPL0454	21	34	60		$V_{CE} = 0.5\text{ V}$		
		HCPLJ451	19	37	60		$T_A = 25^\circ\text{C}$ $V_{CE} = 0.1\text{ V}$		
			13	30			$V_{CE} = 0.5\text{ V}$		
		HCNW4501	23	29	60		$T_A = 25^\circ\text{C}$ $V_{CE} = 0.1\text{ V}$		
			19	31	61		$V_{CE} = 0.5\text{ V}$		
		HCPL4501	26	35	65		$T_A = 25^\circ\text{C}$ $V_{CE} = 0.1\text{ V}$ $I_F = 12\text{ mA}$ $V_{CE} = 4.5\text{ V}$		
		HCPL0454	22	37			$V_{CE} = 0.5\text{ V}$		
	CTR	HCPLJ451	21	43	65	%	$T_A = 25^\circ\text{C}$ $V_{CE} = 0.1\text{ V}$	1, 2, 4	5
			16	35			$V_{CE} = 0.5\text{ V}$		
		HCNW4501	25	31	65		$T_A = 25^\circ\text{C}$ $V_{CE} = 0.1\text{ V}$		
			21	35	69		$V_{CE} = 0.5\text{ V}$		
Logic Low Output Voltage	V_{OL}	HCPL4501		0.2	0.3	V	$T_A = 25^\circ\text{C}$ $I_F = 10\text{ mA}$ $V_{CE} = 4.5\text{ V}$		
		HCPL0454			0.3		$I_F = 12\text{ mA}$		
		HCPLJ451		0.2	0.3		$T_A = 25^\circ\text{C}$ $I_F = 10\text{ mA}$		
					0.3		$I_F = 10\text{ mA}$		
		HCNW4501		0.2	0.3		$T_A = 25^\circ\text{C}$ $I_F = 10\text{ mA}$		
					0.3		$I_F = 10\text{ mA}$		
Logic High Output Current	I_{OH}			0.003	0.5	μA	$T_A = 25^\circ\text{C}$ $V_{CE} = V_{CC} = 5.5\text{ V}$ $I_F = 0\text{ mA}$	5	
				0.01	1		$T_A = 25^\circ\text{C}$ $V_{CE} = V_{CC} = 15\text{ V}$		
Logic Low Supply Current	I_{CC1}	HCPL4501		50	200	μA	$I_F = 10\text{ mA}$ $V_{CE} = \text{Open}$ $V_{CC} = 15\text{ V}$		12
		HCPL0454							
		HCNW4501							
		HCPLJ451		50					
Logic High Supply Current	I_{CC2}			0.02	1	μA	$T_A = 25^\circ\text{C}$ $I_F = 0\text{ mA}$ $V_{CE} = \text{Open}$ $V_{CC} = 15\text{ V}$		12
					2		$V_{CE} = 15\text{ V}$		
Input Forward Voltage	V_F	HCPL4501		1.5	1.7	V	$T_A = 25^\circ\text{C}$ $I_F = 10\text{ mA}$	3	
		HCPL0454			1.8				
		HCPLJ451	1.45	1.59	1.85		$T_A = 25^\circ\text{C}$ $I_F = 10\text{ mA}$		
		HCNW4501	1.45		1.95				
Input Reverse Breakdown Voltage	BV_F	HCPL4501	5			V	$I_R = 10\text{ }\mu\text{A}$		
		HCPL0454							
		HCPLJ451	3				$I_R = 100\text{ }\mu\text{A}$		
		HCNW4501							
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	HCPL4501		± 6		$\text{mV}/^\circ\text{C}$	$I_F = 10\text{ mA}$		
		HCPL0454							
		HCPLJ451		± 4					
		HCNW4501							
Input Capacitance	C_{IN}	HCPL4501		60		pF	$f = 1\text{ MHz}$ $V_F = 0\text{ V}$		
		HCPL0454							
		HCPLJ451		70					

*All typicals at $T_A = 25^\circ\text{C}$

AC Switching Specifications

Over recommended temperature ($T_A = 0^\circ\text{C}$ to 70°C) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PLL}			0.2	0.3	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 20\text{ kHz}$, Duty Cycle = 10%, $I_F = 16\text{ mA}$, $V_{CC} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{FRL} = 1.5\text{ V}$	6, 8, 9	9
					0.5				
	t_{PLL}		0.2	0.5	0.7	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty Cycle = 50%, $I_F = 12\text{ mA}$, $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{FRL} = 1.5\text{ V}$	6, 10-11	10
		HCPL-J454 Others	0.05 0.1		1.0				
Propagation Delay Time to Logic High at Output	t_{PLH}			0.3	0.5	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 20\text{ kHz}$, Duty Cycle = 10%, $I_F = 16\text{ mA}$, $V_{CC} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $V_{FRL} = 1.5\text{ V}$	6, 8, 9	9
					0.7				
	t_{PLH}		0.3	0.8	1.1	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty Cycle = 50%, $I_F = 12\text{ mA}$, $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{FRL} = 2.0\text{ V}$	6, 10-11	10
			0.2		1.4				
Propagation Delay Difference Between Any 2 Parts	$t_{PLH} - t_{PLL}$		-0.4	0.3	0.9	μs	$T_A = 25^\circ\text{C}$ Pulse: $f = 10\text{ kHz}$, Duty Cycle = 50%, $I_F = 12\text{ mA}$, $V_{CC} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $V_{FRL} = 1.5\text{ V}$, $V_{FRLH} = 2.0\text{ V}$	6, 10-11	17
			-0.7		1.3				
Common Mode Transient Immunity at Logic High Level Output	$[CM_I]$		15	30		$\text{kV}/\mu\text{s}$	$T_A = 25^\circ\text{C}$ $V_{CC} = 1500\text{ V}_{DC}$, $V_{CE} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $I_F = 0\text{ mA}$	7	7, 9
	$[CM_I]$		15	30		$\text{kV}/\mu\text{s}$	$V_{CE} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 0\text{ mA}$	7	8, 10
Common Mode Transient Immunity at Logic Low Level Output	$[CM_I]$		15	30		$\text{kV}/\mu\text{s}$	$T_A = 25^\circ\text{C}$ $V_{CC} = 1500\text{ V}_{DC}$, $V_{CE} = 5.0\text{ V}$, $R_L = 1.9\text{ k}\Omega$, $C_L = 15\text{ pF}$, $I_F = 16\text{ mA}$	7	7, 9
	$[CM_I]$	HCPL-J454	15	30		$\text{kV}/\mu\text{s}$	$V_{CE} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 12\text{ mA}$	7	8, 10
	$[CM_I]$	Others	10						
	$[CM_I]$		15	30		$\text{kV}/\mu\text{s}$	$V_{CE} = 15.0\text{ V}$, $R_L = 20\text{ k}\Omega$, $C_L = 100\text{ pF}$, $I_F = 16\text{ mA}$	7	8, 10

*All typ. at $T_A = 25^\circ\text{C}$

Package Characteristics

Over recommended temperature ($T_A = 0^\circ\text{C}$ to 25°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{SO}	HCPL4501	2500			V_{rms}	$RI \leq 50\%$, $t = 1 \text{ min.}$, $T_A = 25^\circ\text{C}$		6, 11, 16
		HCPL0454	3750						6, 14, 16
		HCPL4501	5000						6, 11, 15
		Option 020	5000						6, 15, 16
		HCNW4504	5000						
Input-Output Resistance	R_{IO}	HCPL4501		10^{12}		Ω	$V_{IO} = 500 \text{ Vdc}$		6
		HCPL0454							
		HCPL454							
		HCNW4504	10^{12}	10^{13}			$T_A = 25^\circ\text{C}$ $T_A = 100^\circ\text{C}$		
Capacitance (Input-Output)	C_{IO}	HCPL4501		0.6		pF	$f = 1 \text{ MHz}$		6
		HCPL0454							
		HCPL454		0.8					
		HCNW4504		0.5	0.6				

*All typicals at $T_A = 25^\circ\text{C}$.

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Related Characteristics Table (if applicable), your equipment level safety specifications or IHP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

- Derate linearly above 70°C free-air temperature at a rate of $0.8 \text{ mW}/^\circ\text{C}$ (8-Pin DIP).
- Derate linearly above 80°C free-air temperature at a rate of $0.5 \text{ mW}/^\circ\text{C}$ (SO-8).
- Derate linearly above 70°C free-air temperature at a rate of $1.6 \text{ mW}/^\circ\text{C}$ (8-Pin DIP).
- Derate linearly above 80°C free-air temperature at a rate of $1.0 \text{ mW}/^\circ\text{C}$ (SO-8).
- Derate linearly above 70°C free-air temperature at a rate of $0.9 \text{ mW}/^\circ\text{C}$ (8-Pin DIP).
- Derate linearly above 80°C free-air temperature at a rate of $1.1 \text{ mW}/^\circ\text{C}$ (SO-8).
- Derate linearly above 70°C free-air temperature at a rate of $2.0 \text{ mW}/^\circ\text{C}$ (8-Pin DIP).
- Derate linearly above 80°C free-air temperature at a rate of $2.1 \text{ mW}/^\circ\text{C}$ (SO-8).
- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_C , to the forward LED input current, I_F , times 100.
- Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
- Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0 \text{ V}$). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8 \text{ V}$).
- Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0 \text{ V}$). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0 \text{ V}$).
- The $1.9 \text{ k}\Omega$ load represents 1 TTL unit load of 1.6 mA and the $5.6 \text{ k}\Omega$ pull-up resistor.
- The $R_L = 20 \text{ k}\Omega$, $C_L = 100 \text{ pF}$ load represents an IPM (Intelligent Power Module) load.
- See Option 020 data sheet for more information.
- Use of a 0.1 pF bypass capacitor connected between Pins 5 and 8 is recommended.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 3000 \text{ V rms}$ for 1 second (leakage detection current limit, $I_{DC} \leq 5 \mu\text{A}$).
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 1500 \text{ V rms}$ for 1 second (leakage detection current limit, $I_{DC} \leq 5 \mu\text{A}$).
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 2000 \text{ V rms}$ for 1 second (leakage detection current limit, $I_{DC} \leq 5 \mu\text{A}$).
- This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
- The difference between $t_{R,4}$ and $t_{F,4}$ between any two devices (same part number) under the same test conditions. (See Power Inverter Dead Time and Propagation Delay Specifications section.)

Figure 1. IM and Pooled Transfer Characteristics.

Figure 2. Current Transfer Ratio vs. Input Current.

Figure 3. Input Current vs. Forward Voltage.

Figure 4. Current Transfer Ratio vs. Temperature.

Figure 5. Logic High Output Current vs. Temperature.

Figure 6. Switching Test Circuit.

Figure 7. Test Circuit for Transient Immunity and Typical Waveforms.

Figure 8. Propagation Delay Time vs. Temperature.

Figure 9. Propagation Delay Time vs. Load Resistance.

Figure 10. Propagation Delay Time vs. Load Resistance.

Figure 11. Propagation Delay Time vs. Temperature.

Figure 12. Propagation Delay Time vs. Load Resistance.

Figure 13. Propagation Delay Time vs. Load Capacitance.

Figure 14. Propagation Delay Time vs. Supply Voltage.

Figure 15. Thermal Derating Curve. Dependence of Safety Limiting Value with Case Temperature per VDE 0884.

Figure 16. Typical Power Inverter.

Figure 17. LMI Delay and Dead Time Diagram.

Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-4500/454 and HCSW-4504 include a specification intended to help designers minimize "dead time" in their power inverter designs. The new "propagation delay difference" specification ($t_{PLH} - t_{PHL}$) is useful for determining not only how much optocoupler switching delay is needed to prevent "shoot-through" current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 17), it is essential that they never conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This "shoot-through" current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of "dead time" at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the

same way), it is important to know the minimum and maximum turn-on (t_{PIN}) and turnoff (t_{PILO}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled "LED1",

"LED2", "OUT1", and "OUT2" are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.

The LED signal to turn on Q2 should be delayed enough so that an optocoupler with the very fastest turn-on propagation delay ($t_{PILOmin}$) will never turn on before an optocoupler with the very slowest turn-off propagation delay ($t_{PILOmax}$) turns off. To ensure this, the turn-on of the optocoupler should be delayed by an amount no less than $(t_{PILOmax} - t_{PILOmin})$, which also happens to be the

maximum data sheet value for the propagation delay difference specification, $(t_{PILO} - t_{PILO})$. The HCPL-4504/0454/0454 and HCNW450-1 specify a maximum $(t_{PILO} - t_{PILO})$ of 1.3 μ s over an operating temperature range of 0-70°C.

Although $(t_{PILO} - t_{PILO})_{max}$ tells the designer how much delay is needed to prevent shoot-through current, it is insufficient to tell the designer how much dead time a design will have. Assuming that the optocoupler turn-on delay is exactly equal to $(t_{PILO} - t_{PILO})_{max}$, the minimum dead time is zero (i.e., there is zero time between the turnoff of the very slowest optocoupler and the turn-on of the very fastest optocoupler).

Calculating the maximum dead time is slightly more complicated. Assuming that the LED turn-on delay is still exactly equal to $(t_{PILO} - t_{PILO})_{max}$, it can be seen in Figure 17 that the maximum dead time is the sum of the maximum difference in turn-on delay plus the maximum difference in turnoff delay.

$$\{(t_{PILOmax} - t_{PILOmin}) + (t_{PILOmax} - t_{PILOmin})\}.$$

This expression can be rearranged to obtain

$$\{(t_{PILOmax} - t_{PILOmin}) - (t_{PILOmax} - t_{PILOmax})\}.$$

and further rearranged to obtain

$$\{(t_{PILO} - t_{PILO})_{max} - (t_{PILO} - t_{PILO})_{min}\}.$$

which is the maximum minus the minimum data sheet values of $(t_{PILO} - t_{PILO})$. The difference between the maximum and minimum values depends directly on the total spread in propagation delays and sets the limit on how good the worst-case dead time can be for a given design.

Therefore, optocouplers with tight propagation delay specifications (and not just shorter delays or lower pulse-width distortion) can achieve short dead times in power inverters. The HCPL-4504/0454/0454 and HCNW450-1 specify a minimum $(t_{PILO} - t_{PILO})$ of -0.7 μ s over an operating temperature range of 0-70°C, resulting in a maximum dead time of 2.0 μ s when the LED turn-on delay is equal to $(t_{PILO} - t_{PILO})_{max}$, or 1.3 μ s.

It is important to maintain accurate LED turn-on delays because delays shorter than $(t_{PILO} - t_{PILO})_{min}$ may allow shoot-through currents, while longer delays will increase the worst-case dead time.

www.hp.com/go/india

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-253-6342 or 888-634-8673

Far East/Australasia: Call your local HP sales office.

Japan: (81-3) 3339-8112

Europe: Call your local HP sales office.

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Obsoletes 59656-6166E

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SHARP PC817

This data sheet is readily available at www.sharp.co.jp/ecg/opto/products.

SHARP

PC817 Series

PC817 Series

High Density Mounting Type
Photocoupler

* Lead forming type (I type) and tape reel type (P type) are also available. (PC817/PC817P)
 * TÜV (VDE0884) approved type is also available as an option.

■ Features

1. Current transfer ratio
(CTR: MIN. 50% at $I_F = 5\text{mA}$, $V_{CE} = 5\text{V}$)
2. High isolation voltage between input and output (V_{iso} : 5000V_{rms})
3. Compact dual-in-line package
 PC817 : 1-channel type
 PC827 : 2-channel type
 PC837 : 3-channel type
 PC847 : 4-channel type
4. Recognized by UL, file No. E64380

■ Applications

1. Computer terminals
2. System appliances, measuring instruments
3. Registers, copiers, automatic vending machines
4. Electric home appliances, such as fan heaters, etc.
5. Signal transmission between circuits of different potentials and impedances

■ Outline Dimensions

(Unit : mm)

* In the absence of confirmation by device specification sheets, SHARP takes no responsibility for any defects that occur in equipment using any of SHARP's devices, shown in catalogs, data books, etc. Contact SHARP in order to obtain the latest version of the device specification sheets before using any SHARP's device.

SHARP**PC817 Series****■ Absolute Maximum Ratings**

(Ta = 25°C)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	*1 Peak forward current	I_{FM}	1	A
	Reverse voltage	V_R	6	V
	Power dissipation	P	70	mW
Output	Collector-emitter voltage	V_{CE0}	35	V
	Emitter-collector voltage	V_{EC0}	6	V
	Collector current	I_C	50	mA
	Collector power dissipation	P_C	150	mW
Total power dissipation		P_{tot}	200	mW
*2 Isolation voltage		V_{iso}	5 000	V _{rms}
Operating temperature		T_{op}	-30 to +100	°C
Storage temperature		T_{stg}	-55 to +125	°C
*3 Soldering temperature		T_{sol}	260	°C

*1 Pulse width $\leq 100\mu s$, Duty ratio : 0.001

*2 40 to 60% RH, AC for 1 minute

*3 For 10 seconds

■ Electro-optical Characteristics

(Ta = 25°C)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage	V_F	$I_F = 20mA$	-	1.2	1.4	V
	Peak forward voltage	V_{FM}	$I_{FM} = 0.5A$	-	-	3.0	V
	Reverse current	I_R	$V_R = 4V$	-	-	10	μA
	Terminal capacitance	C_t	$V = 0, f = 1kHz$	-	30	250	pF
Output	Collector dark current	I_{C0}	$V_{CE} = 20V$	-	-	10^{-7}	A
Transfer characteristics	*4 Current transfer ratio	CTR	$I_F = 5mA, V_{CE} = 5V$	50	-	600	%
	Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_F = 20mA, I_C = 1mA$	-	0.1	0.2	V
	Isolation resistance	R_{iso}	DC500V, 40 to 60% RH	5×10^9	10^{11}	-	Ω
	Floating capacitance	C_f	$V = 0, f = 1MHz$	-	0.6	1.0	pF
	Cut-off frequency	f_c	$V_{CE} = 5V, I_C = 2mA, R_L = 100\Omega, -3dB$	-	80	-	kHz
	Response time	Rise time Fall time	$V_{CE} = 2V, I_C = 2mA, R_L = 100\Omega$	- -	4 3	18 18	μs

*4 Classification table of current transfer ratio is shown below.

Model No.	Rank mark	CTR (%)
PC817A	A	80 to 160
PC817B	B	130 to 260
PC817C	C	200 to 400
PC817D	D	300 to 600
PC8#7AB	A or B	80 to 260
PC8#7BC	B or C	130 to 400
PC8#7CD	C or D	200 to 600
PC8#7AC	A, B or C	80 to 400
PC8#7BD	B, C or D	130 to 600
PC8#7AD	A, B, C or D	80 to 600
PC8#7	A, B, C, D or No mark	50 to 600

* : 1 or 2 or 3 or 4

Fig. 1 Forward Current vs. Ambient Temperature

Fig. 2 Collector Power Dissipation vs. Ambient Temperature

Fig. 3 Peak Forward Current vs. Duty Ratio

Fig. 4 Current Transfer Ratio vs. Forward Current

Fig. 5 Forward Current vs. Forward Voltage

Fig. 6 Collector Current vs. Collector-emitter Voltage

Fig. 7 Relative Current Transfer Ratio vs. Ambient Temperature

Fig. 8 Collector-emitter Saturation Voltage vs. Ambient Temperature

Fig. 9 Collector Dark Current vs. Ambient Temperature

Fig.10 Response Time vs. Load Resistance

Fig.11 Frequency Response

Test Circuit for Response Time

Test Circuit for Frequency Response

Fig.12 Collector-emitter Saturation Voltage vs. Forward Current

● Please refer to the chapter "Precautions for Use"

APPENDIX G: POWEREX DC-DC CONVERTER DATA SHEET

This data sheet is readily available on the Internet at www.pwr.com.

POWEREX

Powerex, Inc., 200 Mills Street, Youngwood, Pennsylvania 15887-1800 (724) 825-7372

M57140-01

Isolated DC-to-DC Converter

Outline Drawing and Circuit Diagram

Dimensions	inches	Millimeters
A	2.03	51.5
B	0.71	18.0
C	39±.06	12.5±1.5
D	.18±.06	4.5±1.5
E	0.07	1.8

Dimensions	inches	Millimeters
F	0.32	0.55
G	0.06	2.1
H	0.08	2.1
J	1.13	28.8

Description:

M57140-01 is an isolated DC-to-DC converter designed to drive IPMs (Intelligent Power Modules). With an input of DC 20V, the module supplies four 15V outputs. Isolation is provided from primary to secondary and also between the secondaries. Interwinding isolation is designed for driving the IPM.

Features:

- ☐ Output Specification:
+15V x 4, Total 3W max.
- ☐ Primary-to-secondary isolation:
2500 VRMS, One Minute
- ☐ Secondary-to-secondary
Isolation Voltage:
1500 VRMS, One Minute
- ☐ Compact, Low Profile Design

Applications:

- ☐ IPMs for General Purpose
Inverter and AC Servo
- ☐ Power Source for MOSFET
Driving Circuits

Ordering Information:

M57140-01

POWEREX

Powerex, Inc., 200 Millie Street, Youngwood, Pennsylvania 15097-1809 (724) 925-7272

M57140-01
Isolated
DC-to-DC Converter

Absolute Maximum Ratings, $V_{IN} = 20V$, $T_A = 25^\circ C$ unless otherwise specified

Characteristics	Symbol	Test Conditions	M57140-01	Units
Input Voltage	V_{IN}	Terminals (4)-(5)-(6)-(1)-(2)-(3)	25	Volts
Load Current	I_L	Terminals (14)-(13)-(12)-(11)-(10)-(9)	30	mA
		Terminals (8)-(7)	100	mA
Operating Temperature	T_{OP}	There Should be	-10 - +75	$^\circ C$
Storage Temperature	T_{STG}	No Condensation	-20 - +85	$^\circ C$
Internal Power Dissipation	P_D	-	1.5	Watts
Primary-to-Secondary Isolation		1 Minute	2500	V_{rms}
Secondary-to-Secondary Isolation		1 Minute	1500	V_{rms}

Electrical Characteristics, $V_{IN} = 20V$, $T_A = 25^\circ C$ unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Source Voltage	V_{IN}	Direct Current	18	20	22	Volts
Output Voltage	V_O	Between Pins (10)-(9)-(12)-(11)-(14)-(13) $I_L = 30mA$	13.5	15.0	16.5	Volts
		Between Pins (8)-(7) $I_L = 100mA$	13.5	15.0	16.5	Volts
Peak Load Current	I_{LP}	Between Pins (10)-(9)-(12)-(11)-(14)-(13) $I_L = 30mA$	-	33	-	mA
		Between Pins (8)-(7) $I_L = 30mA$	-	110	-	mA
Load Regulation	Reg-out	Between Pins (10)-(9)-(12)-(11)-(14)-(13) $I_L = 0 - 30mA$	-	5	10	%
		Between Pins (8)-(7) $I_L = 0 - 100mA$	-	7	12	%
Efficiency	η	Between Pins (10)-(9)-(12)-(11)-(14)-(13) $I_L = 30mA$	-	70	-	%
		Between Pins (8)-(7) $I_L = 100mA$	-	70	-	%

Application Circuit

POWEREX

Powerex, Inc., 200 Mills Street, Youngwood, Pennsylvania 15897-1800 (724) 925-7272

M57140-01
Isolated
DC-to-DC Converter

Application Circuit

Handling Precautions:

- When M57140-01 is used under excessive load condition, output side rectifying diodes will be destroyed. Care should be exercised so as not to operate the device above the rated maximum load current.
- Coating Materials should not be applied on this device because the application of coating materials for waterproofing could cause a stress and destroy a device.

POWEREX

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15667-1800 (724) 825-7272

MS7148-01

Isolated

DC-to-DC Converter

APPENDIX H: ASSEMBLY PROGRAM

The following program originally was composed by Texas Instruments' application engineer Zhenyu Yu. (Yu and Figoli 1998) The program was modified for the application that this paper has outlined.

```

*****
** File Name      : sv20c.asm                      **
** Project : ACI motor drive                      **
**                                                       **
** Originator    : Zhenyu Yu                      **
**               : Texas Instruments              **
**               : DSP Automotive/Industrial Applications **
** Modified by   : Jacob Bemrich                  **
** Target       : TMS320C240/F240  EVM            **
*****
; Description
;-----
; This program implements an open- loop speed control algorithm for
; three-phase AC induction motors using constant V/Hz principle and
; space vector PWM technique.
;
; This is the version of the program that uses s/w determined space-
; vector PWM switching scheme.
;
;*****
; Status          : Worked
; Last update     : 2/2/01
;
;-----
; Date of Mod    | Description
;-----
; 5/18/98        | Made corrections to have decomp matrices for s/w
;                | and h/w implementations.
; 11/20/00       | Modified to run at 1200 Hz and ADC input
;                | frequency adjustment.
; 2/2/01         | cleaned up comments
;-----
; Notes
;-----
; 1. This program implements an int driven sampling and control loop
;    for three-phase AC induction motor control through a 3 -phase
;    voltage source inverter.
; 2. Constant V/Hz principle is used to generate the magnitude of
;    reference voltage from frequency input.
; 3. Space-vector PWM technique is employed to generate a sinusoidal
;    type of three-phase voltage output from the inverter.
; 4. Both PWM and sampling frequencies are 20KHz.
; 5. Maximum scaling and 32 bit integration are used to maximize the
;    accuracy of integer math.
; 6. Frequency input is through ADC15. 0 - 1200Hz
; 7. The D scaling notation used here is related to the popular Q

```



```
; scaling notation by Dx=Q15-x.
```

```
-----
; Peripheral Registers and constants of TMS320C240
;-----
```

```
        .include      " C240APP.H "
ST0      .set    0          ; status register ST0
ST1      .set    1          ; status register ST1
wd_rst_1 .set    055h       ; watchdog timer reset strings
wd_rst_2 .set    0aah       ;
LED_addr .set    0Ch        ; addr of LED display on EVM
```

```
-----
; Variables in B1 page 0
;-----
```

```
        .bss    error,1      ; Number of errors
        .bss    temp0,1      ; temporary storage
        .bss    one,1        ; +1

        .bss    delay_cntr,1 ; Delay counter for inverter
                                ; routine

        .bss    period_flag,1 ; period start flag

        .bss    set_F,1      ; set F input (0-1.0):
                                ; D0 (0-0-0Hz, 1.0-7FE0h-1200Hz)
        .bss    F_W,1        ; set F to angular speed ratio:
                                ; D13
        .bss    S_W,1        ; set angular speed: D13
        .bss    min_W,1      ; lower limit on set W: D13

        .bss    W_U,1        ; angular speed to voltage
                                ; ratio: D-12
        .bss    S_U,1        ; set voltage: D1
        .bss    max_U,1      ; upper limit on set U: D1
        .bss    min_U,1      ; lower limit on set U: D1

        .bss    T_sample,1   ; sampling period: D- 12

        .bss    THETAH,1     ; phase of ref volt vector
                                ; higher word: D3
        .bss    THETAL,1     ; THETA lower word
        .bss    theta_r,1    ; rounded THETAH: D3

        .bss    theta_m,1    ; THETA mapped to 1st quadrant:
                                ; D3
        .bss    theta_i,1    ; theta to index for sine table:
                                ; D7
        .bss    SS,1         ; sin sign modification: D15
        .bss    SC,1         ; cos sign modification: D15
        .bss    index,1      ; index to sine table: D15
        .bss    SIN_1st,1    ; beginning of sin table
        .bss    SIN_last,1   ; end of sin table
```

```

.bss sin_theta,1      ; sin(THETA): D1
.bss cos_theta,1      ; cos(THETA): D1
.bss Ud,1             ; voltage Ud: D3
.bss Uq,1             ; voltage Uq: D3
.bss S,1              ; sector reference U is in: D15

.bss theta_60,1       ; 60: D3
.bss theta_90,1       ; 90: D3
.bss theta_120,1      ; 120: D3
.bss theta_180,1      ; 180: D3
.bss theta_240,1      ; 240: D3
.bss theta_270,1      ; 270: D3
.bss theta_300,1      ; 300: D3
.bss theta_360,1      ; 360: D3

.bss dec_ms,24         ; Decomposition matrices: D1
.bss T1_periods,1 ; scaled Timer 1 period: D10

.bss cmp_1,1           ; component on 1st basic sp
                        ; vector: D15
.bss cmp_2,1           ; component on 2nd basic sp
                        ; vector: D15
.bss cmp_0,1           ; component on 0 basic sp vector
                        ; /2: D15

.bss first_tog,1       ; the 1st-to-toggle channel
.bss sec_tog,1         ; the 2nd-to-toggle channel

.bss svpat,1           ; S/V pattern for ACTR

.bss LED_dir,1         ; LED direction (1: left,
                        ; 0: right)
.bss LED_data,1        ; LED display
LED_freq .set 3000      ; LED update sub-divider
.bss LED_count,1       ; sub-divider counter for LED

;-----
; Basic context in B2
;-----
ST0_save .usect ".context",1 ; saved status register ST0
ST1_save .usect ".context",1 ; saved status register ST1

;-----
; Extended context in B1 page 0
;-----
ACCH .usect ".extcont",1 ; saved accumulator high
ACCL .usect ".extcont",1 ; saved accumulator low
AR0_save .usect ".extcont",1 ; saved AR0 content
AR1_save .usect ".extcont",1 ; saved AR1 content
P_hi .usect ".extcont",1 ; saved P high byte
P_lo .usect ".extcont",1 ; saved P low byte
T_save .usect ".extcont",1 ; saved T content

```

```

;-----
; Program parameters
;-----
debug_data.set 7FFFh ; (1200Hz,7FFF) (1000Hz,6AAC) (600Hz,3FFF)
                    ; (500Hz,3556) (300Hz,1FFF) (250Hz,1AAB)
                    ; (25Hz,2AB)

T_sample_.set 1A37h ; D-12, Ts = 50uS, Fs = 20KHz
                  ; Scaled sampling period
                  ; Ts*2**24
                  ; Ts = Tpwm = 50uS -> 20KHz

Tl_period_.set 500 ; Timer 1 period
                ; Tpwm/50nS/2 = 50uS/50nS/2 = 500

Tl_periods_.set 500*32 ; D10
                  ; Scaled Timer 1 period

; Set frequency to radian frequency conversion ratio
; 1200*2*pi/7FE0h(D0) = 7540.052472756
; Since the ADC is only 10bits the last 6 bits are 0 therefore
; 7FE0h corresponds to 1200Hz=7539.822368616 rad/sec
F_W_.set 30160 ; D13

min_W_.set 0 ; D13
           ; Minimum radian frequency
           ; We did not want the motor, to spin at
           ; 0 setting.

; Radian frequency to ref voltage conversion ratio -> V/Hz constant
; 1.0/sqrt(2)/(1000*2*pi) = 0.0011254 = 15105 (D-12)
; 1.0/sqrt(2)/(600*2*pi) = 0.000187566 = 25174 (D-12)
; 1.0/sqrt(2)/(60*2*pi) = 0.00187566 too big for D- 12.
; 1.0/sqrt(2)/(800*2*pi) = 0.000140674 = 18881 (D-12)
; 1.0/sqrt(2)/(1200*2*pi) = 0.000937829 = 12587 (D- 12)
; 1.0/sqrt(2)/(240*2*pi) = 0.000468915 too big for D-12.
W_U_.set 15105 ; D-12

max_U_.set 11585 ; D1 (1b less res to reduce # of
                 ; shifts)
                 ; Max magnitude of reference voltage
                 ; 1.0/sqrt(2) = 0.7071067811865

min_U_.set 3636 ; D1
               ; Min magnitude of reference voltage
               ; given by 1.0/sqrt(2)*min_F/1000Hz
               ; We needed to energize the coils a
               ; little at 0 Hz that is why it is not
               ; 0.

; Conversion from theta to index for sine table: 360/(0.5pi)

```

```
theta_i_ .set 29335 ; D8
```

```
.data
```

```
-----
; Frequently used angles
-----
*****
** The order between these angles and the decomposition      **
** matrices in the following must not be changed.            **
*****
angles_ .WORD      010c1h ; pi/3: D3
        .WORD      01922h ; pi/2: D3
        .WORD      02183h ; 2*pi/3: D3
        .WORD      03244h ; pi: D3
        .WORD      04305h ; 4*pi/3: D3
        .WORD      04b66h ; 3*pi/2: D3
        .WORD      053c7h ; 5*pi/3: D3
        .WORD      06488h ; 2*pi: D3
```

```
-----
; Decomposition matrices indexed by the sector Uout is in for s/w
; implemented space-vector PWM scheme
-----
```

```
        .WORD      20066      ; D1
        .WORD      -11585
        .WORD      0
        .WORD      23170

        .WORD      -20066
        .WORD      11585
        .WORD      20066
        .WORD      11585

        .WORD      0
        .WORD      23170
        .WORD      -20066
        .WORD      -11585

        .WORD      0
        .WORD      -23170
        .WORD      -20066
        .WORD      11585

        .WORD      -20066
        .WORD      -11585
        .WORD      20066
        .WORD      -11585

        .WORD      20066
        .WORD      11585
        .WORD      0
        .WORD      -23170
```

```

;-----
; Decomposition matrices indexed by the sector Uout is in for h/w
; implemented space-vector PWM scheme
;-----
;          .WORD      20066          ; D1
;          .WORD      -11585
;          .WORD      0
;          .WORD      23170

;          .WORD      20066
;          .WORD      11585
;          .WORD      -20066
;          .WORD      11585

;          .WORD      0
;          .WORD      23170
;          .WORD      -20066
;          .WORD      -11585

;          .WORD      -20066
;          .WORD      11585
;          .WORD      0
;          .WORD      -23170

;          .WORD      -20066
;          .WORD      -11585
;          .WORD      20066
;          .WORD      -11585

;          .WORD      0
;          .WORD      -23170
;          .WORD      20066
;          .WORD      11585

;-----
; Addresses of compare registers of the 1st-to- toggle channels
; indexed by the sector, s, Uout is in
;-----
first_  .WORD  CMPR1      ;
        .WORD  CMPR2      ;
        .WORD  CMPR2      ;
        .WORD  CMPR3      ;
        .WORD  CMPR3      ;
        .WORD  CMPR1      ;

;-----
; Addresses of compare registers of the 2nd-to- toggle channels
; indexed by the sector, s, Uout is in
;-----
second_ .WORD  CMPR2      ;
        .WORD  CMPR1      ;
        .WORD  CMPR3      ;
        .WORD  CMPR2      ;

```

```

        .WORD CMPR1          ;
        .WORD CMPR3          ;

;-----
; Lookup table for ACTR[15 -12] indexed by sector number
;-----
cckwise_ .WORD 0001000000000000b
        .WORD 0011000000000000b
        .WORD 0010000000000000b
        .WORD 0110000000000000b
        .WORD 0100000000000000b
        .WORD 0101000000000000b

;-----
; Reset & interrupt vectors
;-----
        .sect ".vectors"
RSVECT   B      START          ; PM 0 Reset Vector
INT1     B      PHANTOM        ; PM 2 Int level 1
INT2     B      EV_isr_A      ; EV interrupt Group A
INT3     B      PHANTOM        ; EV interrupt Group B
INT4     B      PHANTOM        ; PM 8 Int level 4
INT5     B      PHANTOM        ; PM A Int level 5
INT6     B      PHANTOM        ; PM C Int level 6
RESERVED B      PHANTOM        ; PM E (Analysis Int)
SW_INT8  B      PHANTOM        ; PM 10      User S/W int
SW_INT9  B      PHANTOM        ; PM 12      User S/W int
SW_INT10 B      PHANTOM        ; PM 14      User S/W int
SW_INT11 B      PHANTOM        ; PM 16      User S/W int
SW_INT12 B      PHANTOM        ; PM 18      User S/W int
SW_INT13 B      PHANTOM        ; PM 1A      User S/W int
SW_INT14 B      PHANTOM        ; PM 1C      User S/W int
SW_INT15 B      PHANTOM        ; PM 1E      User S/W int
SW_INT16 B      PHANTOM        ; PM 20      User S/W int
TRAP     B      PHANTOM        ; PM 22      Trap vector
NMI      B      PHANTOM        ; PM 24      Non maskable Int
EMU_TRAP B      PHANTOM        ; PM 26      Emulator Trap
SW_INT20 B      PHANTOM        ; PM 28      User S/W int
SW_INT21 B      PHANTOM        ; PM 2A      User S/W int
SW_INT22 B      PHANTOM        ; PM 2C      User S/W int
SW_INT23 B      PHANTOM        ; PM 2E      User S/W int

        .text
;=====
; Start of main body of code
;-----
START          DINT          ; Set global interrupt mask

;-----
; Reset (disable for now) WD timer
;-----
        LDP    #0E0h          ; Point at Sys Module reg page 0
        SPLK   #wd_rst_1,WD_KEY

```

```

SPLK  #wd_rst_2,WD_KEY
SPLK  #0000000001101111b,WD_CNTL

;-----
; Set the source of CLKOUT to be CPUCLK
;-----
SPLK  #0100000011000000b,SYSCR

;-----
; Clear all SYSSR bits except bit 5, the HP0 bit.
; FLASH programming and WD disable are allowed when bit 5 is 1.
; Note that bit 5 is a read/clear bit. It can't be set.
;-----
splk  #000000000100000b,SYSSR

;-----
; Configure PLL/Clocks so that CPUCLK=20MHz when CLKIN=10MHz
;-----
SPLK  #10110001b,CKCR1    ; Configure PLL
SPLK  #00000001b,CKCR0    ; Disable PLL
SPLK  #11000001b,CKCR0    ; Re-enable PLL

;-----
; Initialize and start ADC
;-----
LDP  #0E0h
SPLK  #0000000000000101b,ADC_CNTL1    ;
SPLK  #0101100111111111b,ADC_CNTL0    ;ADC15 and ADC 7

;-----
; Configure wait state generator - no wait states
;-----
LDP  #6                      ; Point to memory page 0 (B2)
SPLK #1000b,temp0           ; temp0<=0008h
OUT  temp0,0ffffh          ; WSGR <= (temp0)

;-----
; Initialize Event Manager
;-----
SPLK  #0,T1CON
SPLK  #0,T2CON
SPLK  #0,T3CON
SPLK  #0,DBTCON
SPLK  #0,COMCON
SPLK  #0,CAPCON
SPLK  #0,T1CNT
SPLK  #0,T2CNT
SPLK  #0,T3CNT

;-----
; Configure GP Timer 1, the PWM time base
; Put GPT1 in cont-up/down mode for symmetric PWM
;-----
LDP  #232                      ; Point at EV register page

```

```

SPLK  #T1_period_,T1PER
SPLK  #1010100000000010b,T1CON

;-----
; Define PWM output polarities
; PWM1,3,5 - active low; PWM2,4&6 - active high
;-----
SPLK  #0000100110011001b,ACTR

;-----
; Define and enable dead band (50*50nS=2.5uS): 32h = 50
;-----
SPLK  #32e0h,DBTCN

;-----
; Zero the duty cycle of all PWM outputs
;-----
SPLK  #T1_period_,CMPR1
SPLK  #T1_period_,CMPR2
SPLK  #T1_period_,CMPR3

;-----
; Enable PWM outputs and enable compare
;-----
SPLK  #0000001100000111b,COMCON
SPLK  #1000001100000111b,COMCON

;-----
; Enable PWM outputs, compare and space-vector PWM mode
;-----
; SPLK  #0001001100000111b,COMCON
; SPLK  #1001001100000111b,COMCON

;-----
; Initialize variables
;-----
LDP    #6                                ; Point to B1 page 0
SPLK   #0,error                          ; Reset error counter
SPLK   #1,one                            ; +1 => one

SPLK   #T_sample_,T_sample               ; sampling period
SPLK   #T1_periods_,T1_periods           ; max compare value

splk   #0,set_F                          ; zero set F.

SPLK   #F_W_,F_W                        ; D13, set F to angular
                                           ; speed ratio
SPLK   #W_U_,W_U                        ; D-12, angular speed to
                                           ; voltage ratio

SPLK   #min_W_,min_W                    ; lower limit on set W
SPLK   #max_U_,max_U                    ; upper limit on set U
SPLK   #min_U_,min_U                    ; lower limit on set U

```



```

SPLK #0,THETAL ; theta low byte
SPLK #0,THETAH ; theta high byte

LAR ARO,#theta_60 ; point to 1st destination
LAR AR1,#(32-1) ; 32 entries
LACC #angles_ ; point to 1st data item
LARP ARO ;
Init_tb TBLR *+,1 ; move and point to next
; destination
ADD one ; point to next data item
BANZ Init_tb,0 ;

splk #theta_i_,theta_i ; D7, init theta-index
; ratio

SPLK #TB_S_,SIN_1st ; init 1st and last
; entries of sin tb
SPLK #(TB_S_+360),SIN_last

SPLK #0,THETAH ; zero angular position
; high
SPLK #0,THETAL ; zero angular position
; low

splk #01h,LED_data ; Reset LED display on EVM
out LED_data,LED_addr ; Set LED display
splk #LED_freq,LED_count ; reset sub-divider
; counter
splk #1,LED_dir ; set LED display
; direction

;-----
; Enable interrupts and real-time operation
;-----
ldp #232 ; point at EV reg page
SPLK #0ffh,IFRA ; Clear all Group A interrupt flags
SPLK #0ffh,IFRB ; Clear all Group B interrupt flags
SPLK #0fh,IFRC ; Clear all Group C interrupt flags
SPLK #0200h,IMRA ; Mask all but GPT1 UF Grp A ints
SPLK #0h,IMRB ; Mask all ints
SPLK #00h,IMRC ; Mask all Grp C ints
LDP #0 ; point to memory page 0
SPLK #0ffh,IFR ; Clear all core interrupt flags
SPLK #0eh,IMR ; Unmask all EV interrupts to CPU
EINT ; Enable global interrupt

LDP #232 ; Point at EV reg page
SPLK #1010100001000010b,T1CON

;=====
; Start background loop

```

```

;-----
MAIN          setc  xf          ; Toggle xf for debug
purpose

;-----
          ldp #6          ;point at B1 page 0
w_sample LACC  period_flag
          BZ    w_sample          ;wait if not set, if set
                                   ; continue
          SPLK #0,period_flag
;-----
; Update LED display on EVM
;-----
          ldp  #6          ; point at B1 page 0
          lacc LED_count          ;
          sub  one          ; update sub_divide counter
          sac1 LED_count          ; time to update LED display?
          BNZ  LED_nc          ; no
          splk #LED_freq,LED_count ; yes, reset subdivide
                                   ; counter
          bit  LED_dir,BIT0          ; left shift?
          bcnd right_shift,NTC          ; no
          lacc LED_data,1          ; yes
          sac1 LED_data          ; left shift one bit
          bit  LED_data,BIT7          ; time to change
                                   ; direction?
          bcnd LED_update,NTC          ; no
          splk #0,LED_dir          ; yes
          b    LED_update          ;
right_shift lacc LED_data,15          ;
          sach LED_data          ; right shift one bit
          bit  LED_data,BIT0          ; time to change
                                   ; direction?
          bcnd LED_update,NTC          ; no
          splk #1,LED_dir          ; yes
LED_updateout LED_data,LED_addr          ; update LED display
LED_nc

;-----
; Read the reference frequency using the ADC
;-----
          LDP  #0E0h          ;Point at sys mod reg page 0

          lac1 ADC1_DATA          ;Get ADC data from ADC15, 0 ACC high
          SPLK #0101100111111111b,ADC_CNTL0; restart ADC

          ldp  #6          ;point at B1 page 0

          sfr          ;shift right by one bit
          sac1 set_F          ;save: D0

; Replace set_F with debug data. For debug purpose only.

```

```

;          SPLK   #debug_data,set_F   ;

;-----
; Calculate set angular speed based set F
;-----
          LT      set_F           ; set F -> T: D0
          MPY     F_W             ; D0*D13=D(13+1)
          PAC                     ; product -> ACC: D14
          SACH    S_W,1           ; -> set angular speed: D13

          SUBH    min_W           ; compare W with its lower limit: D13
          BGZ     W_in_limit      ; continue if within limit
          LACC     min_W          ; saturate if not
          SACL    S_W             ; D13
W_in_limit

;-----
; Calculate magnitude of ref voltage Uout based on V/Hz principle
;-----
          LT      S_W             ; set angular speed -> T: D13
          MPY     W_U             ; D13*D-12=D(1+1)
          PAC                     ; product -> ACC: D2
          SACH    S_U,1           ; -> mag of reference voltage
                                   ; and -> D1

          SUBH    max_U           ; compare Uout with its upper
                                   ; limit
          BLEZ    U_in_uplimit    ; continue if within limit
          LACC     max_U          ; saturate if not
          SACL    S_U             ;
U_in_uplimit
          LACC     S_U             ;
          SUB      min_U          ; compare Uout with its lower
                                   ; limit
          BGEZ    U_in_lolimit    ; continue if within limit
          LACC     min_U          ; saturate if not
          SACL    S_U             ; D1
U_in_lolimit

;-----
; Reset wd timer and loop back
;-----
          LDP     #0E0h           ; Point at Sys Module reg page 0
          SPLK    #wd_rst_1,WD_KEY ; Reset watchdog timer
          SPLK    #wd_rst_2,WD_KEY

          clrc    xf              ; Debug signal
          B       MAIN           ; Branch back

;=====
; Interrupt driven inner loop
;-----

```

```

EV_isr_A  SST    #ST0,ST0_save      ; save status register ST0
          SST    #ST1,ST1_save      ; save status register ST1
          LDP    #6                  ; point to page 0 of B0
          MAR    *,AR0               ; use AR0
          SACH   ACCH                ;
          SACL   ACCL                ; save ACC
          sph    P_hi                ;
          spl    P_lo                ; save P register
          mpy    one                 ; P<=T
          spl    T_save              ; save T register
          sar    AR0,AR0_save        ; save AR0

          LAR    AR0,#IVRA           ; Identify int source
          LACC   *                   ;
          SUB    #029h               ; GPT1 UF int?
          BCND   T1UF_ISR,EQ         ; Yes
          B      PHANTOM             ; got a phantom int if not

;-----
; Obtain theta (phase of Uout) through 32 bit integration
;-----
T1UF_ISR  LT     S_W                 ; set W -> T: D13
          MPY    T_sample            ; D13*D-12=D(1+1)
          PAC                      ; product -> ACC: D2
          SFR                      ; ->D3
          ADDH   THETAH ; D3+D3=D3 (32 bit)
          ADDS   THETAH ;
          SACH   THETAH ; save
          SACL   THETAH ;
          SUBH   theta_360           ; D3-D3=D3 compare with 2*pi
          BLEZ   T_in_limit          ; continue if within limit
          SACH   THETAH ; mod(2*pi, THETA) if not
T_in_limit ZALH  THETAH ;
          ADDS   THETAH ;
          ADD    one,15 ;
          SACH   theta_r             ; round up to upper 16 bits

;-----
; Determine quadrant
;-----
          LACC   one                 ; assume THETA(THETAH) is in quadrant1
          SACL   SS                  ; 1=>SS, sign of SIN(THETA)
          SACL   SC                  ; 1=>SC, sign of COS(THETA)
          LACC   theta_r             ;
          SACL   theta_m             ; THETA=>theta_m
          SUB    theta_90            ;
          BLEZ   E_Q                 ; jump to end if 90>=THETA

          ; assume THETA(THETAH) is in quadrant2
          splk   #-1,SC ; -1=>SC
          LACC   theta_180           ;
          SUB    theta_r             ; 180-THETA
          SACL   theta_m             ; =>theta_m

```

```

BGEZ  E_Q          ; jump to end if 180>=THETA

                                ; assume THETA(THETAH) is in quadrant3
splk  #-1,SS ; -1=>SS
LACC  theta_r      ;
SUB   theta_180    ; THETA-180
SACL  theta_m      ; =>theta_m
LACC  theta_270    ;
SUB   theta_r      ;
BGEZ  E_Q          ; jump to end if 270>=THETA

                                ; THETA (THETAH) is in quadrant 4
splk  #1,SC        ; 1=>SC
LACC  theta_360    ;
SUB   theta_r      ;
SACL  theta_m      ; 360-THETAH=>theta_m

E_Q

;-----
; sin(theta), cos(theta)
;-----

      lt      theta_m          ; D3. Find index
      mpy     theta_i          ; D3*D8=D(11+1)
      pac                      ; D12

      sach    index            ; D12. Make index an integer (D15)
      lacc    index,13         ;
      sach    index            ; right shift 3 bits => D15

      lac     SIN_1st          ; Look up sin
      add     index            ;
      tblr    sin_theta        ;
      lac     SIN_last         ;
      sub     index            ;
      tblr    cos_theta        ;

      LT      SS               ; Look up cos
      MPY     sin_theta        ; modify sign: D15*D1=D(16+1)
      PAC                      ;
      SACL    sin_theta        ; left shift 16 bits and save: D1
      LT      SC               ;
      MPY     cos_theta        ; modify sin: D15*D1=D(16+1)
      PAC                      ;
      SACL    cos_theta        ; left shift 16 bits and save: D1

;-----
; Calculate Ud & Uq
;-----

      LT      S_U              ; set U -> T: D1
      MPY     cos_theta        ; set U*cos(THETA): D1*D1=D(2+1)
      PAC                      ; product -> ACC: D3
      SACH    Ud,1             ; d component of ref Uout: D2
      MPY     sin_theta        ; set U*sin(THETA): D1*D1=D(2+1)

```

```

PAC                                ; product -> ACC: D3
SACH  Uq,1                        ; q component of ref Uout: D2

;-----
; Determine sector
;-----

MAR  *,AR0                        ; ARP points to AR0

LAR  AR0,#1 ; assume S=1
LACC theta_r                      ;
SUB  theta_60                    ; compare with 60 (in sector 1?)
BLZ  E_S                        ; jump to end if yes

MAR  *+                          ; assume S=2 if not
LACC theta_r                      ;
SUB  theta_120                   ; compare with 120 (in sector 2?)
BLZ  E_S                        ; jump to end if yes

MAR  *+                          ; assume S=3 if not.
LACC theta_r                      ;
SUB  theta_180                   ; compare with 180 (in sector 3?)
BLZ  E_S                        ; jump to end if yes

MAR  *+                          ; assume S=4 if not
LACC theta_r                      ;
SUB  theta_240                   ; compare with 240 (in sector 4?)
BLZ  E_S                        ; jump to end if yes

MAR  *+                          ; assume S=5 if not
LACC theta_r                      ;
SUB  theta_300                   ; compare with 300 (in sector 5?)
BLZ  E_S                        ; jump to end if yes

MAR  *+                          ; S=6 if not
E_S  SAR  AR0,S                  ;

;-----
; Calculate T1 & T2 based on
;
;      Tpwm Uout = V1*T1 + V2*T2
; i.e.
;      [T1 T2] = Tpwm [V1 V2]' Uout
; i.e.
;      [0.5*T1 0.5*T2] = Tp [V1 V2]' Uout
; i.e.
;      [0.5*C1 0.5*C2] = [V1 V2]' Uout = M(s) Uout
; where
;      C1 = T1/Tp, C2 = T2/Tp, are the normalized components
;      M(S) = [V1 V2]' (' - inverse)
;      Uout = Trans[Ud Uq]
;
; M(s) is obtained through table look- up.
; Tp is Timer 1 period, which is half of PWM period.

```

```

-----
        LACC    #(dec_ms-4)
        ADD     S,2          ;
        SACL    temp0        ; get the pointer
        LAR     AR0,temp0    ; point to parameter table

; Calculate 0.5*C1 based on  $0.5*C1 = U_d * M(1,1) + U_q * M(1,2)$ 
        LT      Ud           ; D2
        MPY     **           ; M(1,1) Ud:  $D2 * D1 = D(3+1)$ 
        PAC     ; D4
        LT      Uq           ; D4
        MPY     **           ; M(1,2) Uq:  $D2 * D1 = D(3+1)$ 
        APAC    ;  $0.5*C1: D4 + D4 = D4$ 
        BGEZ    cmp1_big0    ; continue if bigger than zero
        ZAC     ; set to 0 if less than 0
cmp1_big0 SACH    temp0      ; D4
        LT      temp0        ; D4
        MPY     T1_periods    ;  $D4 * D10 = D(14+1)$ 
        PAC     ; D15
;        ADD     one,16 ; Avoid C1=0
        SACH    cmp_1        ; D15

; Calculate 0.5*C2 based on  $0.5*C2 = U_d * M(2,1) + U_q * M(2,2)$ 
        LT      Ud           ; D2
        MPY     **           ; M(2,1) Ud:  $D2 * D1 = D(3+1)$ 
        PAC     ; D4
        LT      Uq           ; D2
        MPY     **           ; M(2,2) Uq:  $D2 * D1 = D(3+1)$ 
        APAC    ;  $0.5*C2: D4 + D4 = D4$ 
        BGEZ    cmp2_big0    ; continue if bigger than zero
        ZAC     ; zero it if less than zero
cmp2_big0 SACH    temp0      ; D4
        LT      temp0        ; D4
        MPY     T1_periods    ;  $D4 * D10 = D(14+1)$ 
        PAC     ; D15
;        ADD     one,16 ; Avoid 0 C2 = 0
        SACH    cmp_2        ; D15

; Calculate 0.5*C0 based on  $0.5*C3 = T_p - 0.5*C1 - 0.5*C2$ 
        LACC    #T1_period_   ;
        SUB     cmp_1         ;
        SUB     cmp_2         ; D15
        BGEZ    cmp0_big0    ; continue if bigger than zero
        ZAC     ; zero it if less than zero
cmp0_big0 SACL    cmp_0        ;

        LACC    cmp_0,15      ; right shift 1b (by left shift 15b)
        SACH    cmp_0         ;  $0.25*C0$ 

-----
; Determine channel toggling sequence and load compare registers
;
        LACC    #(first_-1)   ;

```

```

ADD    S                ; point to entry in look up
                        ; table
TBLR   first_tog        ; get 1st-to-toggle channel
LAR    ARO,first_tog    ; point to the channel

LACC   cmp_0            ;
SACL   *                ; cmp_0 (1/4 C0) => the channel

LACC   #(second_-1) ;
ADD    S                ; point to entry in look up
                        ; table
TBLR   sec_tog          ; get 2nd-to-toggle channel
LAR    ARO,sec_tog      ; point to the channel
LACC   cmp_0            ;
ADD    cmp_1            ; cmp_0+cmp_1 -> 1/4 C0 + 1/2 C1
SACL   *                ; => the channel

LACC   #CMPR3           ;
SUB    first_tog        ;
ADD    #CMPR2           ;
SUB    sec_tog          ;
ADD    #CMPR1           ;
SACL   temp0            ; get 3rd-to-toggle channel
LAR    ARO,temp0        ; point to the channel
LACC   cmp_0            ;
ADD    cmp_1            ;
ADD    cmp_2            ; cmp_0+cmp_1+cmp_2 -> 1/4 C0 +
                        ; 1/2 C1 + 1/2 C2
SACL   *                ; =>the channel

lar    ARO, ARO_save    ; restore ARO
lt     P_lo             ; T<=P_lo
mpy    one              ; P (low byte) <=1*P_lo
lph    P_hi             ; P high byte <=P_hi
lt     T_save           ; restore T
ZALH   ACCH             ;
ADDS   ACCL             ; restore ACC
LDP    #0               ; point to B2
LST    #ST1,ST1_save    ; restore status register ST1
LST    #ST0,ST0_save    ; restore status register ST0

SPLK   #1,period_flag   ;set start flag

EINT                    ;
RET                                ; return

```

```

;=====
; Phantom interrupt handling
;-----
PHANTOM  SST    #ST0,ST0_save    ; save status register ST0
          SST    #ST1,ST1_save    ; save status register ST1
          LDP    #6              ; point to page 0 of B0

```



```

MAR    *,AR0                ; use AR0
SACH   ACCH                  ;
SACL   ACCL                  ; save ACC
sph    P_hi                  ;
spl    P_lo                  ; save P register
mpy    one                   ; P<=T
spl    T_save                ; save T register
sar    AR0,AR0_save ; save AR0

LACC   error                 ; Increase error counter
ADD    one                   ;
SACL   error                 ;

lar    AR0, AR0_save        ; restore AR0
lt     P_lo                  ; T<=P_lo
mpy    one                   ; P (low byte) <=1*P_lo
lph    P_hi                  ; P high byte <=P_hi
lt     T_save                ; restore T
ZALH   ACCH                  ;
ADDS   ACCL                  ; restore ACC
LDP    #0                    ; point to memory page 0
LST    #ST1,ST1_save        ; restore status register ST1
LST    #ST0,ST0_save        ; restore status register ST0
EINT                   ;
RET                                ;

Delay      LDP    #6
           LACC   #10
           SACL   delay_cntr
Delay1     LAC    delay_cntr
           SUBK   1
           SACL   delay_cntr
           BNZ    Delay1
           RET

;-----
; sine table for theta from 0 to 90 per every 0.25 degrees
;-----
TB_S_                                ; sin table
.WORD    0                        ; D1
.WORD    71
.WORD    143
.WORD    214
.WORD    286
.WORD    357
.WORD    429
.WORD    500
.WORD    572
.WORD    643
.WORD    715
.WORD    786
.WORD    857

```

.WORD	929
.WORD	1000
.WORD	1072
.WORD	1143
.WORD	1214
.WORD	1285
.WORD	1357
.WORD	1428
.WORD	1499
.WORD	1570
.WORD	1641
.WORD	1713
.WORD	1784
.WORD	1855
.WORD	1926
.WORD	1997
.WORD	2068
.WORD	2139
.WORD	2209
.WORD	2280
.WORD	2351
.WORD	2422
.WORD	2492
.WORD	2563
.WORD	2634
.WORD	2704
.WORD	2775
.WORD	2845
.WORD	2915
.WORD	2986
.WORD	3056
.WORD	3126
.WORD	3196
.WORD	3266
.WORD	3336
.WORD	3406
.WORD	3476
.WORD	3546
.WORD	3616
.WORD	3686
.WORD	3755
.WORD	3825
.WORD	3894
.WORD	3964
.WORD	4033
.WORD	4102
.WORD	4171
.WORD	4240
.WORD	4310
.WORD	4378
.WORD	4447
.WORD	4516
.WORD	4585

.WORD	4653
.WORD	4722
.WORD	4790
.WORD	4859
.WORD	4927
.WORD	4995
.WORD	5063
.WORD	5131
.WORD	5199
.WORD	5266
.WORD	5334
.WORD	5402
.WORD	5469
.WORD	5536
.WORD	5604
.WORD	5671
.WORD	5738
.WORD	5805
.WORD	5872
.WORD	5938
.WORD	6005
.WORD	6071
.WORD	6138
.WORD	6204
WORD	6270
.WORD	6336
.WORD	6402
.WORD	6467
.WORD	6533
.WORD	6599
.WORD	6664
.WORD	6729
.WORD	6794
.WORD	6859
.WORD	6924
.WORD	6989
.WORD	7053
.WORD	7118
.WORD	7182
.WORD	7246
.WORD	7311
.WORD	7374
.WORD	7438
.WORD	7502
.WORD	7565
.WORD	7629
.WORD	7692
.WORD	7755
.WORD	7818
.WORD	7881
.WORD	7943
.WORD	8006
.WORD	8068

.WORD	8130
.WORD	8192
.WORD	8254
.WORD	8316
.WORD	8377
.WORD	8438
.WORD	8500
.WORD	8561
.WORD	8621
.WORD	8682
.WORD	8743
.WORD	8803
.WORD	8863
.WORD	8923
.WORD	8983
.WORD	9043
.WORD	9102
.WORD	9162
.WORD	9221
.WORD	9280
.WORD	9339
.WORD	9397
.WORD	9456
.WORD	9514
.WORD	9572
.WORD	9630
.WORD	9688
.WORD	9746
.WORD	9803
.WORD	9860
.WORD	9917
.WORD	9974
.WORD	10031
.WORD	10087
.WORD	10143
.WORD	10199
.WORD	10255
.WORD	10311
.WORD	10366
.WORD	10422
.WORD	10477
.WORD	10531
.WORD	10586
.WORD	10641
.WORD	10695
.WORD	10749
.WORD	10803
.WORD	10856
.WORD	10910
.WORD	10963
.WORD	11016
.WORD	11069
.WORD	11121

.WORD	11174
.WORD	11226
.WORD	11278
.WORD	11330
.WORD	11381
.WORD	11433
.WORD	11484
.WORD	11535
.WORD	11585
.WORD	11636
.WORD	11686
.WORD	11736
.WORD	11786
.WORD	11835
.WORD	11885
.WORD	11934
.WORD	11982
.WORD	12031
.WORD	12080
.WORD	12128
.WORD	12176
.WORD	12223
.WORD	12271
.WORD	12318
.WORD	12365
.WORD	12412
.WORD	12458
.WORD	12505
.WORD	12551
.WORD	12597
.WORD	12642
.WORD	12688
.WORD	12733
.WORD	12778
.WORD	12822
.WORD	12867
.WORD	12911
.WORD	12955
.WORD	12998
.WORD	13042
.WORD	13085
.WORD	13128
.WORD	13170
.WORD	13213
.WORD	13255
.WORD	13297
.WORD	13338
.WORD	13380
.WORD	13421
.WORD	13462
.WORD	13502
.WORD	13543
.WORD	13583

.WORD	13623
.WORD	13662
.WORD	13702
.WORD	13741
.WORD	13780
.WORD	13818
.WORD	13856
.WORD	13894
.WORD	13932
.WORD	13970
.WORD	14007
.WORD	14044
.WORD	14081
.WORD	14117
.WORD	14153
.WORD	14189
.WORD	14225
.WORD	14260
.WORD	14295
.WORD	14330
.WORD	14364
.WORD	14399
.WORD	14433
.WORD	14466
.WORD	14500
.WORD	14533
.WORD	14566
.WORD	14598
.WORD	14631
.WORD	14663
.WORD	14694
.WORD	14726
.WORD	14757
.WORD	14788
.WORD	14819
.WORD	14849
.WORD	14879
.WORD	14909
.WORD	14938
.WORD	14968
.WORD	14996
.WORD	15025
.WORD	15053
.WORD	15082
.WORD	15109
.WORD	15137
.WORD	15164
.WORD	15191
.WORD	15218
.WORD	15244
.WORD	15270
.WORD	15296
.WORD	15321

.WORD	15346
.WORD	15371
.WORD	15396
.WORD	15420
.WORD	15444
.WORD	15468
.WORD	15491
.WORD	15515
.WORD	15537
.WORD	15560
.WORD	15582
.WORD	15604
.WORD	15626
.WORD	15647
.WORD	15668
.WORD	15689
.WORD	15709
.WORD	15729
.WORD	15749
.WORD	15769
.WORD	15788
.WORD	15807
.WORD	15826
.WORD	15844
.WORD	15862
.WORD	15880
.WORD	15897
.WORD	15914
.WORD	15931
.WORD	15948
.WORD	15964
.WORD	15980
.WORD	15996
.WORD	16011
.WORD	16026
.WORD	16041
.WORD	16055
.WORD	16069
.WORD	16083
.WORD	16096
.WORD	16110
.WORD	16123
.WORD	16135
.WORD	16147
.WORD	16159
.WORD	16171
.WORD	16182
.WORD	16193
.WORD	16204
.WORD	16214
.WORD	16225
.WORD	16234
.WORD	16244

.WORD	16253
.WORD	16262
.WORD	16270
.WORD	16279
.WORD	16287
.WORD	16294
.WORD	16302
.WORD	16309
.WORD	16315
.WORD	16322
.WORD	16328
.WORD	16333
.WORD	16339
.WORD	16344
.WORD	16349
.WORD	16353
.WORD	16358
.WORD	16362
.WORD	16365
.WORD	16368
.WORD	16371
.WORD	16374
.WORD	16376
.WORD	16378
.WORD	16380
.WORD	16382
.WORD	16383
.WORD	16383
.WORD	16384
.WORD	16384

APPENDIX I: DSP HEADER FILE

```

;*****
; File Name:      C240APP.H
; Project: C240 EVM Apps S/W suite
; Originator/s: Auto/Ind DSP Apps group - Texas Instruments (Houston)
;
; Description: C240 Header file with all Peripheral Register
declarations
;
;      + other useful defines.
;
;-----
; Date of Mod      | DESCRIPTION
;-----
; 3 Oct 96         | Added Event Manager Register declarations.
; 18 Oct 96        | Modified SPI register declarations to match the U.G.
                    | and added some definitions for peripheral data pages
                    | and analysis breakpoint register.
; Oct 22, 96       | dropped "_abs" from all the register names.
;                  | added DP_EV, EV register data memory page
;
;-----
; On Chip Periperal Register Definitions (DATA SPACE)
;-----
;C2xx Core Registers
;-----
IMR      .set      0004h      ;Int Mask Register
GREG     .set      0005h      ;Global memory allocation reg
IFR      .set      0006h      ;Int Flag Register

;System Module Registers
;-----
SYSCR    .set      07018h      ;System Module Control Register
SYSSR    .set      0701Ah      ;System Module Status Register
DIN      .set      0701Ch      ;Device Identification Register
SYSIVR   .set      0701Eh      ;System Interrupt Vector Register

XINT1_CNTL.set 07070h;Int1 (type A) Control reg
NMI_CNTL .set 07072h      ;Non maskable Int (type A) Control reg
XINT2_CNTL.set 07078h;Int2 (type C) Control reg
XINT3_CNTL.set 0707Ah;Int3 (type C) Control reg
PDPINT_CNTL.set 0742Ch;Power Drive Protection Int cntl reg

;Digital I/O
;-----
OPCRA    .set      07090h      ;Output Control Reg A
OPCRB    .set      07092h      ;Output Control Reg B
IPSRA    .set      07094h      ;Input Status Reg A
IPSRB    .set      07096h      ;Input Status Reg B
IOPA_DDR .set      07098h      ;I/O port A Data & Direction reg.
PADATDIR .set      IOPA_DDR
IOPB_DDR .set      0709Ah      ;I/O port B Data & Direction reg.
PBDATDIR .set      IOPB_DDR
IOPC_DDR .set      0709Ch      ;I/O port C Data & Direction reg.
IOPD_DDR .set      0709Eh      ;I/O port D Data & Direction reg.

```

;Watch-Dog(WD) / Real Time Int(RTI) / Phase Lock Loop(PLL) Registers

```

;-----
RTI_CNTR .set 07021h ;RTI Counter reg
WD_CNTR .set 07023h ;WD Counter reg
WD_KEY .set 07025h ;WD Key reg
RTI_CNTL .set 07027h ;RTI Control reg
WD_CNTL .set 07029h ;WD Control reg
CKCR0 .set 0702ah ;PLL Clock Control Register 0
CKCR1 .set 0702ch ;PLL Clock Control Register 1

```

;Analog-to-Digital Converter(ADC) registers * NOT CORRECT *

```

;-----
ADC_CNTL0 .set 07032h ;ADC control register 0
ADC_CNTL1 .set 07034h ;ADC control register 1
ADC0_DATA .set 07036h ;ADC 0 Result Data
ADC1_DATA .set 07038h ;ADC 1 Result Data

```

;Serial Peripheral Interface (SPI) Registers

```

;-----
SPICCR .set 07040h ;SPI Configuration Control Register
SPICTL .set 07041h ;SPI Operation Control Register
SPISTS .set 07042h ;SPI Status Register
SPIBRR .set 07044h ;SPI Baud Rate Register
SPIEMU .set 07046h ;SPI Emulation buffer Register
SPIBUF .set 07047h ;SPI Serial Input Buffer Register
SPIDAT .set 07049h ;SPI Serial Data Register
SPIPC1 .set 0704Dh ;SPI Port Control Register 1
SPIPC2 .set 0704Eh ;SPI Port Control Register 2
SPIPRI .set 0704Fh ;SPI Priority control Register

```

;Serial Communications Interface (SCI) Registers

```

;-----
SCICCR .set 07050h ;SCI Communication Control Register
SCICTL1 .set 07051h ;SCI Control Register 1
SCIHBAUD .set 07052h ;SCI Baud Select register, high bits
SCILBAUD .set 07053h ;SCI Baud Select register, high bits
SCICTL2 .set 07054h ;SCI Control Register 2
SCIRXST .set 07055h ;SCI Receive Status Register
SCIRXEMU .set 07056h ;SCI Emulation data buffer Register
SCIRXBUF .set 07057h ;SCI Receiver data buffer Register
SCITXBUF .set 07059h ;SCI Transmit data buffer Register
SCIPC2 .set 0705Eh ;SCI Port Control Register 2
SCIPRI .set 0705Fh ;SCI Priority Control Register

```

;Event Manager (EV) - EV Base Address = 0x7400

```

;-----
EV_BASE .set 7400h ; Event Manager Base Address(DP 232)
GPTCON .set 00h + EV_BASE ; General Timer Controls
T1CNT .set 01h + EV_BASE ; T1 Counter Register
T1CMP .set 02h + EV_BASE ; T1 Compare Register
T1PER .set 03h + EV_BASE ; T1 Period Register
T1CON .set 04h + EV_BASE ; T1 Control Register
T2CNT .set 05h + EV_BASE ; T2 Counter Register

```

```

T2CMP      .set      06h + EV_BASE      ; T2 Compare Register
T2PER      .set      07h + EV_BASE      ; T2 Period Register
T2CON      .set      08h + EV_BASE      ; T2 Control Register
T3CNT      .set      09h + EV_BASE      ; T3 Counter Register
T3CMP      .set      0ah + EV_BASE      ; T3 Compare Register
T3PER      .set      0bh + EV_BASE      ; T3 Period Register
T3CON      .set      0ch + EV_BASE      ; T3 Control Register
COMCON     .set      11h + EV_BASE      ; Compare Unit Control
ACTR       .set      13h + EV_BASE      ; Compare Unit Output Action Control
SACTR      .set      14h + EV_BASE      ; S Comp Unit Output Action Control
; Zhen 11/03/95

DBTCON     .set      15h + EV_BASE      ; Dead Band Timer Control
CMPR1      .set      17h + EV_BASE      ; Compare Channel 1 Threshold
CMPR2      .set      18h + EV_BASE      ; Compare Channel 2 Threshold
CMPR3      .set      19h + EV_BASE      ; Compare Channel 3 Threshold
SCMPR1     .set      1ah + EV_BASE      ; S Comp Channel 1 Threshold
SCMPR2     .set      1bh + EV_BASE      ; S Comp Channel 2 Threshold
SCMPR3     .set      1ch + EV_BASE      ; S Comp Channel 3 Threshold
CAPCON     .set      20h + EV_BASE      ; Capture Unit Control
CAPFIFO    .set      22h + EV_BASE      ; FIFO1-4 Status Register
FIFO1      .set      23h + EV_BASE      ; Capture Channel 1 FIFO Top
FIFO2      .set      24h + EV_BASE      ; Capture Channel 2 FIFO Top
FIFO3      .set      25h + EV_BASE      ; Capture Channel 3 FIFO Top
FIFO4      .set      26h + EV_BASE      ; Capture Channel 4 FIFO Top
IMRA       .set      2ch + EV_BASE      ; Group A Interrupt Mask Register
IMRB       .set      2dh + EV_BASE      ; Group B Interrupt Mask Register
IMRC       .set      2eh + EV_BASE      ; Group C Interrupt Mask Register
IFRA       .set      2fh + EV_BASE      ; Group A Interrupt Flag Register
IFRB       .set      30h + EV_BASE      ; Group B Interrupt Flag Register
IFRC       .set      31h + EV_BASE      ; Group C Interrupt Flag Register
IVRA       .set      32h + EV_BASE      ; Group A Int. Vector Offset(AD dec
; only)
IVRB       .set      33h + EV_BASE      ; Group B Int. Vector Offset(AD dec
; only)
IVRC       .set      34h + EV_BASE      ; Group C Int. Vector Offset(AD dec
; only)

;-----
; Constant defines
;-----

B0_SADDR   .set      00100h            ;Block B0 start address
B0_EADDR   .set      001FFh            ;Block B0 end address
B1_SADDR   .set      00300h            ;Block B1 start address
B1_EADDR   .set      003FFh            ;Block B1 end address
B2_SADDR   .set      00060h            ;Block B2 start address
B2_EADDR   .set      0007Fh            ;Block B2 end address

DP_PF1     .set      224                ;page 1 of peripheral file (7000h/80h)
DP_PF2     .set      225                ;page 2 of peripheral file (7080h/80h)
DP_PF3     .set      226                ;page 3 of peripheral file (7100h/80h)
DP_EV      .set      232                ; EV register data mem page (7400h)

ABRPT      .set      01fh              ; Analysis BreakPoint Register
PSA_ON     .set      03A1h             ; Turn PSA and FEEDB on

```

PSA_OFF .set 0121h ; Turn PSA and FEEDB off

;Bit codes for Test bit instruction (BIT)

BIT15	.set	0000h	;Bit Code for 15
BIT14	.set	0001h	;Bit Code for 14
BIT13	.set	0002h	;Bit Code for 13
BIT12	.set	0003h	;Bit Code for 12
BIT11	.set	0004h	;Bit Code for 11
BIT10	.set	0005h	;Bit Code for 10
BIT9	.set	0006h	;Bit Code for 9
BIT8	.set	0007h	;Bit Code for 8
BIT7	.set	0008h	;Bit Code for 7
BIT6	.set	0009h	;Bit Code for 6
BIT5	.set	000Ah	;Bit Code for 5
BIT4	.set	000Bh	;Bit Code for 4
BIT3	.set	000Ch	;Bit Code for 3
BIT2	.set	000Dh	;Bit Code for 2
BIT1	.set	000Eh	;Bit Code for 1
BIT0	.set	000Fh	;Bit Code for 0