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Characterization of shallow trench isolation etch line edge roughness

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CHARACTERIZATION OF SHALLOW TRENCH ISOLATION ETCH
LINE EDGE ROUGHNESS

A Thesis

Presented to

The Faculty of the Department of Chemical and Materials Engineering

San Jose State University

In Partial Fulfillment

Of the Requirements for the Degree

Masters of Science

By

Becky Min Hon

August 2003

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ABSTRACT

CHARACTERIZATION OF SHALLOW TRENCH ISOLATION ETCH LINE EDGE ROUGHNESS

by Becky M. Hon

The shallow trench isolation process is currently used in integrated circuit fabrication to isolate CMOS transistors. As devices become smaller, the control over process parameters become tighter. STIE characteristics of concern in this research included LER, CD etch bias, CD uniformity, and defect number. The main issue was the control of LER on 193nm photoresist. A design of experiment was created to characterize LER for this research. Three parameters in shallow trench isolation nitride etch were considered. Gas flow rates CF_4 , CHF_3 , and O_2 , were varied while holding other conditions constant according to the full factorial DOE. The STINITE condition that gave the lowest LER and -20nm CD bias while maintaining low CD uniformity and defect number was the 28:16:8sccm CF_4 : CHF_3 : O_2 condition. It was found that increasing O_2 gas flow rate decreased LER. The tradeoff in obtaining the lowest LER was an increase in defects.

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CHAPTER ONE INTRODUCTION

1.1 Integrated Circuit Fabrication

The semiconductor industry has been a rapidly changing field ever since the first integrated circuit (IC) was invented in 1960. The number of devices manufactured on semiconductor substrates continue to increase in part due to the decrease in minimum feature sizes of the devices. The number of devices had grown to more than 1 billion devices per chip in the year 2000 [1]. Silicon technology, primarily using silicon semiconductor substrates, remains a dominant technology in IC fabrication.

Manufacturing integrated circuits involves the fabrication of layers of insulating, conducting, and semiconducting materials on a silicon wafer. The layers are patterned individually to form structures that perform a specific function. These structures create chips that consist of a combination of devices such as diodes, transistors, and inverters. The devices are interconnected to create specific circuit configurations for desired electrical paths. In the design of ICs it is critical to make the correct connections and prevent cross talk between devices that are not connected [1].

1.2 Shallow Trench Isolation

1.2.1 Device Isolation Technology

Device isolation technology is an essential part of IC fabrication. It is necessary to prevent current from leaking and flowing between adjacent devices. In device isolation, devices are built into local islands of active silicon surrounded by isolating regions. These devices are electrically isolated from each other and only interconnected for the desired circuit.

Various isolation techniques are used for different IC devices. The technique currently used for complimentary metal oxide semiconductor (CMOS) transistors is shallow trench isolation (STI). This technology isolates individual transistors from each other by etching a shallow trench into the silicon and filling the trench with deposited oxide to make it nonconducting. Then the devices are built between the trenches, on the plateaus of the active silicon areas. Shallow trench isolation is typically used for isolation in advanced devices of $0.25\mu\text{m}$ (micron) or less [2].

1.2.2 STI versus Local Oxidation of Silicon

Previously transistors were isolated by local oxidation of silicon (LOCOS) before the introduction of STI. Shallow trench isolation replaces LOCOS as dimensions in submicron CMOS technology continues to decrease. STI is preferred over LOCOS due to its progressive scalability to define and fill narrow trenches without voids and to maintain desired electrical isolation [3]. The main advantages of STI over LOCOS are its effectiveness in eliminating bird's beak encroachment into active regions and ability to provide planar surfaces for further processing.

The bird's beak encroachment occurs in LOCOS during wet oxidation of field oxide. The oxide is supposed to grow where there is no masking nitride, but some oxidant diffuses laterally at the edges of the nitride. This causes some oxide to lift the nitride edges while growing under it, and create a tapered oxide wedge that merges into the pad oxide as shown in Figure 1. This limits the scaling of the channel widths since the actual active part of the device becomes smaller [1]. In contrast, STI uses deposited oxide to fill trenches which eliminates the bird's beak encroachment.

Figure 1: Bird's beak encroachment which shows decrease in active area [2].

Another limitation to LOCOS is the planarity of the surface topography, which causes difficulties for lithography and etching. The non-planarity between isolation oxide and active area does not meet lithography requirements. The very small depth of focus of optical steppers used to pattern circuit features is a major limiting factor. To maximize stepper resolution, everything in the field of view must be within a depth of about $0.5\mu\text{m}$, so the imaging surface must be flat for pattern transfer [1]. Shallow trench isolation has a low topography, thus providing a much planar surface than LOCOS.

1.3 Shallow Trench Isolation Process

1.3.1 Basic STI Process

The STI process begins with the growth of a thin pad oxide on a bare silicon wafer. Next, a silicon nitride (or nitride) layer is deposited by low-pressure chemical vapor deposition (LPCVD). The photoresist (PR) layer is then applied, exposed to a patterned mask, and developed. The nitride and pad oxide is etched away first. Then the trench is etched anisotropically into the silicon. The remaining photoresist (resist) is stripped and a thin layer of thermal oxide is grown on the trench walls. A chemical vapor deposition (CVD) dielectric film such as oxide is used to fill the trench and cover areas of

the wafer where nitride still remains. In the chemical mechanical planarization (CMP) step, the dielectric layer is polished back until it reaches the nitride stop layer. Then the dielectric material is densified at approximately 900°C [2]. Finally, the nitride is stripped, leaving the STI structure as shown in Figure 2 of a wafer cross section.

Figure 2: Isolation trenches in silicon filled with oxide.

1.3.2 Shallow Trench Isolation Etch

The STI process consists of two main etch steps. The first etch is the shallow trench isolation nitride etch (STINITE) and the second is the shallow trench isolation etch (STIE). The layers of materials on the silicon wafer prior to the etch steps of the STI process would consist of a thin oxide layer on silicon approximately 100-200 angstrom ($\text{\AA}$) in thickness, a nitride layer of $\sim 1000\text{-}2000\text{\AA}$, and a photoresist layer with bottom anti-reflective coating (BARC). The BARC layer helps to reduce reflectivity at resist interfaces in order to control linewidth and resist performance. A cross section of the stack of layers of materials with a patterned resist is shown in Figure 3.

Figure 3: Cross section of the stack of layers on silicon wafer.

In the process of STINITE, the pattern from the resist is etched onto the nitride so that the nitride acts as a hard mask when etching the trenches into the silicon. This step is also known as hard mask open. The BARC, nitride, and oxide are plasma etched with gases such as carbon tetrafluoride (CF_4), trifluoromethane (CHF_3), and oxygen (O_2). Etch time is increased to promote over etching so that there is a slight gouge into the silicon. Figure 4a shows the cross section of the wafer with all the layers after etch. The remaining resist and BARC are stripped in another plasma etcher using O_2 and nitrogen (N_2). Further cleaning continues in wet chemistries of sulfuric acid with hydrogen peroxide.

The process of STIE is etching the isolating trenches into the silicon. Approximately 2500-4500Å of silicon is etched in a plasma etcher with gases such as hydrobromic acid (HBr) and chlorine (Cl_2). The cross section of the wafer after STIE is shown in Figure 4b. Any remaining resist or residuals are again stripped and cleaned in wet chemistries. A final clean in hydrofluoric acid (HF) comes before the trenches are filled with oxide in the STI process [2,3].

Figure 4: Cross section of wafer (a) after STINITE with silicon gouge, and (b) after STIE with nitride as hard mask.

1.4 Characteristics of STIE

With scaling beyond $0.25\mu\text{m}$ in CMOS technologies, isolation performance has increasing influence over transistor characteristics. Tighter process control over certain parameters become more important as feature size decrease. Integration of the STI process with the rest of the fabrication process relies on how well the process can be controlled and if desired characteristics are achieved. Research has been done on a variety of parameters of STIE to control and enhance isolation performance. Some of these parameters include thickness of the nitride layer, trench profile, trench depth and depth uniformity, defects, critical dimension (CD) and CD uniformity, and line edge roughness (LER).

The nitride thickness left after etch should be a reasonable amount for accurate pattern transfer and CMP purposes. The desired trench profile is slightly sloped sidewalls with rounded corners to eliminate voids or seams in the oxide of trench fill to prevent isolation leakage. The trench depth and depth uniformity determines the strength of isolation and affects the fill and CMP later on in the process. Defects on devices may

come from exposing the gate oxide to contamination in the etch chamber during the process. These etch defects can cause gate leakage and shifts in threshold voltages by migration of contamination through the active areas of the transistor, thus leading to device failure [4,5].

The CD is the size of the smallest geometrical features of the device. The CD and CD uniformity of STI structures must be controlled during pattern transfer to obtain the desired dimensions, which affects the electrical performance of the device. The LER is the roughness of edges of lines patterned in the resist. The LER found on the sidewall of the structures has a severe limitation on CD control. The roughness may be caused by large polymers in the resist and could be transferred to the hard mask or substrate during etch. Strict requirements for smoother line edges become critical as dimensions become narrower. In the semiconductor industry, when 248 nanometer (nm) photoresist was used, LER of the structures were relatively smooth. But when the process switched to 193nm photoresist to obtain smaller CD's, the same etch process produced severe LER. This has become an issue on process conditions since different effects on LER occur between 248nm and 193nm resists [5,6].

These specific characteristics can determine the quality of the shallow trench isolation etch. They are critical factors after STIE that can affect the rest of the STI process and the strength of the isolation. The effects of these critical factors on quality of STIE would ultimately hinder the results of device performance. If the desired characteristics cannot be achieved during STIE, this could lead to the failure of the device.

CHAPTER TWO LITERATURE REVIEW

2.1 Shallow Trench Isolation Process Characteristics

A variety of research has been done on many characteristics of the shallow trench isolation or processes related to it. These studies were conducted to improve the control of processes for better integration of devices with decreasing feature sizes. The following characteristics such as nitride thickness, trench depth and profile, defects, CD and LER have been analyzed by adjusting lithography steps and etch process conditions. These STIE characteristics are coupled to other STI process steps as well as integration applications.

2.2 Silicon Nitride Layer

The role of the nitride layer affects both the etch and chemical mechanical planarization steps in STI. In the trench etch, the nitride layer is a hard mask in pattern transfer for the silicon etch, but later on in the STI process it is primarily a CMP stop layer over active silicon areas. Part of controlling nitride thickness is to control over-polish during the CMP process. The challenge is being able to stop the polish on the nitride without damaging the silicon underneath. It is necessary to remove as little of the nitride as possible during etch to compensate for over-polishing [7].

The polish rate of small isolated structures is faster than large structures and is slower in narrow gaps than in wider gaps due to localized differences in polish pressure. This is critical since over-polishing could lead to nitride erosion and trench oxide loss, destroying device yield. The effect of pattern density on nitride erosion was examined by Schlueter [8]. The pattern density is the ratio of active area over the total area on the

wafer. A pattern density range of 30% to 90% was compared with three different polishing slurries (A, B, and C) and two conditioning techniques (normal and reduced). The results were plotted in Figure 5 with the remaining nitride over pattern density. It can be seen that nitride erosion increases for decrease in pattern density. This confirms that over-polishing poses a problem for a wide pattern density range. Only slurry C, multi-step process, showed an improvement in nitride erosion.

Figure 5: Nitride loss due to CMP over polish, affected by pattern density [8].

The nitride layer determines the step height between the active silicon surface, after nitride strip, and the surface of the trench-fill oxide. This step height should be large enough to avoid parasitic corner transistor effect (degradation of device performance), related to top corner rounding of the isolation trench and is described later in detail. The control of trench oxide and nitride thickness requires tight control of the step height between the trench oxide surface and the silicon surface. Accurate pattern transfer without undesirable interference effects can be obtained when nitride thickness is optimized within these limits [4].

2.3 Trench Shape and Depth

2.3.1 Top Corner Rounding

Top corner rounding of the isolation trench in silicon is significant in defining the interface between the active area of the device and the isolating region. It is desired to have top corner rounding during trench etch since an abrupt transition from active silicon area to the trench can lead to parasitic transistor characteristics. The sharp corner at the top of the silicon becomes exposed during deglazing steps, thus removing oxide, and the strip of gate oxide becomes narrow along both sides of the transistor gate (active silicon area). This results in a polysilicon wraparound where the poly gate wraps around into the isolation corner and this parasitic effect causes reverse narrow channel effects and a double hump in the device's IV curve [9,10].

Lassig et al. [10] had investigated several techniques of trench etch to improve top corner rounding to the required 30-50nm. A new technique was applied during a short etch step after STINITE and before STIE. By applying the top corner rounding during

etch, encroachment was eliminated and the severity of the effect of polysilicon wraparound was reduced. A generic diagram of Figure 6a shows the trench top corner for a conventional process with the rounded edge encroached into the active area under the nitride. In Figure 6b, the diagram shows top corner rounding from an improved process where there is no encroachment and the wraparound is reduced. The dotted lines indicate the removal of oxide during wet HF dips before the steps of sacrificial and gate oxidation.

Figure 6: Top corner of trench shows (a) rounded edge from conventional processes, and (b) no encroachment from improved process [10].

2.3.2 Sidewall Profile

The control for trench profile becomes more critical as feature sizes decrease. Device designs require the trench sidewall profile to have slopes between 78-88° to help alleviate the sharp corner at the top of the silicon trench. The walls should be slightly sloped but not too tapered as it affects oxide trench fill and device leakage. It has been observed that STIE can vary trench profile due to microloading between narrow and wide features. The microloading is caused by build up of polymer on the sidewall so that features facing larger spacing have thinner polymer build up than features facing narrow

spacing. The polymer film acts as an etch barrier and the profile at the narrow spacing becomes more sloped due to the polymer film thickness [11].

It was observed from experiments done by Yeon and You [12] that film deposited on the sidewall caused the open area to continuously decrease during STIE and taper trench profile. Experiments were done in a magnetron enhanced reactive ion etcher and the trench profile was studied with the addition of helium-oxygen (He-O₂) or N₂ additives as well as the characteristics of the film deposited on the sidewall. It was found that the thickness of the sidewall film build up affected sidewall slope and was dependent on the amount of additive gases, He-O₂ or N₂. Figures 7a and 7b illustrate that the trench slope changed as a function of additive gas flow rate and sidewall film thickness. The increase in gas flow increased thickness, which in turn decreased the trench slope since the open space between the etched features became smaller and trench shape became tapered.

Figure 7: Effect of trench slope to additive gases: (a) He-O₂, and (b) N₂ [12].

In further investigations by Werbaneth and Almerico [13], it was proposed that control over the local etch conditions with high density plasma sources using dual radio frequencies and chlorine-argon (Cl₂-Ar) chemistries helped control trench etch profile. In

one approach to control profile, the nature of the silicon etch product was utilized to promote microloading. By adjusting the local environment in the etched trench, the amount of “sticky” [13] etch product generated during STIE redeposited on the trench wall and affected the degree of taper to the profile. The differences in etch profile microloading was affected by the interaction of energetic bombardment of ions from the plasma with species absorbed on the silicon surface. Figure 8a shows the strong response of profile angle and silicon etch rate due to changing wafer bias power from 45 watt (W) to 75W. Also, the argon (Ar) flow in combination with wafer bias power was adjusted in the reactor to show the effect on trench profile angle as shown in Figure 8b. Increasing the wafer bias power from 10W to 100W decreased the profile angle from 89° to 81°, whereas the profile became less steep with decrease in power along with increase in Ar flow.

Figure 8: Change in trench profile angle from (a) wafer bias power, and (b) combination of Ar flow and wafer bias power [13].

2.3.3 Trench Depth

In a study by Lee et al. [11], it was observed that the trench depth nonuniformity was limited by process settings in a high density plasma etcher with Cl_2 -Ar etch chemistry. The STIE was split into two steps so that the trench depth and sidewall profile were controlled in a main etch first step and the rounded bottom corner was controlled in a bottom-rounding step. The depth nonuniformity was calculated by using the formula: $(\text{max-min})/2 \times \text{average}$. From Figure 9, it can be observed that nonuniformity is a strong function of chamber pressure. The depth nonuniformity was improved from $\pm 13.8\%$ to $\pm 7.3\%$ by decreasing chamber pressure from 9 milliTorr (mT) to 3mT and was further improved to less than $\pm 5\%$ when pressure was decreased from 20mT to 3mT in the bottom-rounding step. The nonuniformity increased with increase in pressure for both etch steps. The process settings of the etcher limited the depth nonuniformity. It was also observed that etch depth increased with increase in pressure.

Figure 9: Trench depth nonuniformity and etch depth over chamber pressure [11].

From additional studies by Lee et al. [11], it was found that the trench depth affected junction leakage which was measured by forcing a reverse voltage of 5 volt (V). The junction leakage varied with trench depth as shown in Figures 10a and 10b for isolation spacing of 0.25 and 0.60 μm . For both cases, the increase in trench depth slightly improved junction leakage. This was due to the fact that the depletion depth of the junction became lower relative to trench depth as the depth increased.

Figure 10: Junction leakage varies with trench depth and nonuniformity in isolation spacing of (a) 0.25 μm , and (b) 0.60 μm [11].

2.4 Defects

Another issue with shrinking feature sizes is controlling defects caused by metallic and particulate contamination. Contamination from one process, such as the etch, can affect the rest of the STI process. Plasma process cycle and chamber cleans can introduce contamination into the etch chamber. Research has been done by Richardson [14] to minimize contamination in high density polysilicon etch systems by eliminating contaminant sources in the chamber. Potential metallic contamination sources include the windows, vacuum fittings, spacers, and liners of the etch chamber where impurities

on these components can react with the chemistry during direct contact with the reactive plasma. Particle contamination could be from the etch by-products such as silicon, silicon oxide, and nitride produced from the etch chemistries. These products accumulate on the chamber walls and may flake off as particle contamination. Periodic chamber wet cleans can help avoid such contamination.

In investigations by Richardson [14], the material of the edge ring used to protect the lower electrode was examined between an alumina ceramic ring and a quartz ring. The edge ring is exposed to ion bombardment and by products from reacting with the plasma may be a major source of metallic contaminants. These contaminants and particles can cause etch defects. In one study, the level of defectivity on test wafers were measured after silicon etching with different process conditions in chambers with a quartz or ceramic edge ring. Figure 11 shows the relative defect level on wafers processed in chambers with ceramic and quartz ring over a number of days after the chamber was initially wet cleaned. It was found that the quartz ring reduced metal contamination as well as etch defects. The decrease was attributed to better adhesion of etch by-products to the chamber walls when metal contamination levels of residues are reduced. This showed that ceramic edge rings could be replaced by quartz rings to reduce contamination and defects during etch.

Figure 11: Defectivity level of test wafers over a period of time after clean [14].

2.5 Critical Dimension

Critical dimension control is vital for small feature sizes since it directly affects device performance. Research done on CD control has primarily focused on the process conditions during lithography steps. Many factors in lithography such as resist material, thickness, focus, exposure energy, and substrate reflection affect CD control across the wafer. Proper control of CD and uniformity is necessary in steps prior to and during trench etch when the structures with the desired CDs are etched into the substrate. CD measurements are made in the lithography process as well as before etch and after etch to monitor pattern transfer.

Of the many investigations by Kim et al. [15], one study looked at different dry developments for the formation of resist patterning and CD uniformities of isolated active patterns. Three dry developments that were applied on 248nm resist included the single layer resist (SLR) approach, two-step dry development of top surface imaging process by silylation (TIPS) and three-step dry development of TIPS. Silylation is the process of incorporating silicon into the resist polymer. The three-step dry development of TIPS

consisted of a breakthrough step for the silicon dioxide mask, oxygen plasma etch for the resist, and additional treatment with fluorine gas.

The CDs of 0.3 μ m channel width isolated active patterns were measured at 26 points on the wafer in different dies. The CDs and CD variation across the wafer at different locations obtained from the different dry developments are shown in Figure 12. The SLR and three-step dry development of TIPS showed similar values in CD variations but SLR showed the lowest average CD. Kim et al. [14] believed that the CD uniformity of the isolated active pattern was more important than average CD within a wafer to sustain the stable electrical property of the device. The ratio of LER in the 0.3 μ m channel width isolated active pattern to average CD value between the three processes was also compared. As a result, the ratios of 6% for SLR, 11.96% for two-step, and 6.62% for three-step dry development of TIPS was obtained. It was concluded that the ratio of LER to CD should be controlled to be lower than 7% for TIPS technology to be a candidate for real device applications with 193nm lithography.

Figure 12: CD variation across the wafer at locations indicated by die number [15].

2.6 Line Edge Roughness

2.6.1 Effects of Process Conditions on LER

The quality of the line edge, or how rough the edges are, on STI structures contributes to CD variations. Line edge roughness is the deviation of the real line edge from a straight line and it limits smaller CD values since the relative part of the roughness for the lines of the structures become larger. There are several sources that contribute to the LER of the final active pattern such as the reticle, aerial image quality, etch mask, polymer molecular properties, and plasma processes. Research done by Kim et al. [15] and Palmateer et al. [16] focused on LER caused by silylation of the photoresist and dry development. It was known that the silicon content of the etch mask in TIPS resist after silylation forms the LER in the active pattern.

In investigating the three different dry development processes previously mentioned, Kim et al. [15] primarily examined LER. A comparison between the etching profiles of main cell and isolated active pattern after nitride etching was made for the different dry development processes. The LER of main cell and isolated active patterns were 10.9nm and 10.8nm for the SLR process, 33.2nm and 23.9nm for the two-step dry development of TIPS, and 14.2nm and 15.6nm for the three-step dry development. It was observed that LER was transferred to the nitride substrate after etching. The LER of the SLR process was less than that of the TIPS process. The smaller LER was induced by the flow characteristics of the resist during hard baking before nitride etch.

Palmateer et al. [16] studied the LER from plasma damage during dry development and pattern transfer of silylated 248nm resist. The resist sidewall roughness was observed on near ideal SiO_2 mask resist after etch. It was found that the resist LER changed with resist chemistry and plasma etch conditions. The effect of the source power in the etcher on LER showed decrease in roughness with increase in power. The LER was also observed during the transfer of resist image into the silicon substrate. Figures 13a and 13b shows plots of LER fluctuations for the 248nm resist with ARC after wet development and after pattern transfer into silicon. The results indicated that the change in LER changed after pattern transfer was affected by the plasma etch. In other words, the LER was contributed by the plasma etch rather than direct transfer from the roughness of the resist.

Figure 13: LER fluctuations of 250nm isolated lines (a) with ARC after wet development, and (b) after pattern transfer [16].

2.6.2 Electrical Property Effects from LER

An analysis was made by Kim et al. [15] on the electrical properties of CMOS transistors from the effects of LER in active pattern on device performance. Again, the three dry development processes were used for comparison in creating the transistors. The cumulative plots of threshold voltage variation within the wafer formed by the different dry development processes are shown in Figures 14a and 14b. The variation in threshold voltage for channel widths of $10\mu\text{m}$ and $0.3\mu\text{m}$ was calculated by Equation 1.

$$\text{Variation} \equiv \sqrt{((V_t)_{\text{average}} - (V_t)_i)^2} \quad \text{Equation 1}$$

In Equation 1, $(V_t)_{\text{average}}$ is the average threshold voltage and $(V_t)_i$ is the threshold voltage of an isolated active pattern. The LER introduced channel width variation in the isolated active pattern of the transistors, causing a variation to the threshold voltage. The channel width is directly proportional to the threshold voltage for narrower widths in the recessed active pattern. For the $10\mu\text{m}$ channel width as shown in Figure 14a, the transistors of different processes showed similar values in threshold voltage. But for the

narrower 0.3 μm channel width as shown in Figure 14b, the two-step dry development of TIPS which induced larger LER showed greater threshold voltage variation.

Figure 14: Threshold voltage variation in transistors formed by different dry developments for channel widths of (a) 10 μm , and (b) 0.3 μm [15].

Kim et al. [15] concluded that larger LER from the two-step dry development severely affected the threshold voltage of the transistors and smaller LER from the three-step dry development did not have much affect on the electrical properties of the device. This indicated that the LER caused variations to the CD that eventually affected device performance which was evident for smaller feature sizes in comparing 10 μm to 0.3 μm channel widths.

2.6.3 LER on 193nm Photoresist

When comparing 248nm and 193nm resists, Pollentier et al. [17] observed that the 193nm resist showed poor etch resistance. Both resists were etched with the same $\text{Cl}_2/\text{HBr}/\text{O}_2$ chemistry in a typical poly gate main etch. The 193nm acrylate type resist

that was used typically has about a 40% higher etch rate than the 248nm resist. This lead to the need for a nitride hardmask for integrating 193nm lithography in processes such as STIE.

Pollentier et al. observed that the LER after wet development was transferred to the substrate during the poly gate etch. The resists with the lowest LER after lithography maintained the lowest LER after etch. But it was observed that the LER was lower after the etch compared to the LER on the resist before etch. In the same article, the chemical interaction between the resist and SiON hardmask was studied. It is known that there is a chemical interaction in 248nm resist due to the nature of chemically amplified resists. The effect of the chemical interaction in the 193nm resist is more severe since profile control is more critical and difficult for smaller device features. The surface of the SiON deposited acts chemically like a base and chemically poisons the resist. The SiON surface needs to be capped to prevent this poisoning.

2.6.4 Effects of STINITE Conditions on LER

Experiments on etch conditions done by Bamnolker [18] are relevant in relating the effects of STINITE conditions to changing LER on STI structures. From prior work in a high-density plasma etcher, it was determined that the LER on the 193nm photoresist mask and on the active pattern after STINITE had significantly changed, but LER after STIE remained relatively the same. The effect of STINITE conditions particularly on LER with 193nm photoresist was analyzed keeping STIE conditions constant. A design of experiment (DOE) was created to include all the STINITE parameters that would have an affect on LER including pressure, radio frequency (RF) power, argon (Ar) gas flow

rate, CF₄ to CHF₃ gas flow rate ratio, and the total gas flow rate (sum of CF₄, CHF₃, and O₂ gas flow rates). The characteristics, or response variables, measured after STIE were LER, CD bias (etch bias), CD uniformity, and the number of defects on the wafer. A two-level, five factor (2^{5-2}) fractional factorial DOE with a total of eight runs was used to screen the parameters.

The DOE parameters chosen included pressure, RF power, argon gas flow rate, CF₄:CHF₃ gas flow rate ratio, and total gas flow rate. These parameters fit within the specifications of the high-density plasma etcher. Table 1 lists the parameters of the experiment with corresponding high and low values. A DOE table was generated in Table 2 which shows the two-level high (-1) and low (+1) patterns of the eight runs.

Table 1: High and low values for the DOE parameters. [18]

Parameter	High (+1)	Low (-1)
Pressure	200mT	80mT
RF power	450W	250W
Ar flow rate	200sccm	100sccm
CF ₄ :CHF ₃	2:1	1:1
Total gas flow rate	60-90sccm	10-50sccm

Table 2: Design of experiment table of all five STINITE parameters. [18]

Pressure (mTorr)	RF Power (W)	Ar Flow Rate (sccm)	CF ₄ :CHF ₃ Flow Rate Ratio	Total Gas Flow (sccm)
-1	-1	-1	-1	1
-1	-1	1	1	-1
-1	1	-1	1	-1
-1	1	1	-1	1
1	-1	-1	1	1
1	-1	1	-1	-1
1	1	-1	-1	-1
1	1	1	1	1

The STIE characteristics that were measured after processing STINITE and STIE are listed in Table 3. As a result, the STINITE process condition from the DOE that provided the lowest LER had the --++- DOE pattern with 80mT pressure, power of 250W, 200 standard cubic centimeters per minute (sccm) Ar flow rate, 2:1 CF₄:CHF₃ ratio and a total gas flow rate less than 50sccm. The process conditions in the low pressure and low power (--++-) condition not only produced the lowest LER, but also had low CD uniformity, low defect number, and a CD bias close to -20nm. The desired CD bias for this specific process was -20nm. In this case, it was desired to have a low CD uniformity. This means that the CDs across the wafer are more uniform. If the CDs across the wafer were nonuniform, then the CD uniformity value would be high.

Table 3: STIE characteristics from process conditions of the DOE [18].

DOE Pattern	LER (nm)	CD Bias (nm)	CD Uniformity (nm)	Defects
----+	15.6	-34	42.5	843
--++-	7.9	-15	24.2	559
-+-+-	9.3	-15	21	532
-++-+	21.5	-31	41.1	1171
+--++	14.5	-18	69	1606
+--+--	9	4	52.7	1053
++---	8.4	18	21.2	611
+++++	8.4	-19	33.6	695

2.7 Potential Research with STIE Characteristics

Research has been done on certain characteristics of STIE which verified the importance in controlling the STI processes. Over-polish in CMP proved to be an issue in controlling nitride thickness, with increase in nitride erosion as pattern density decreased. Without proper control of trench top corners, sharp corners would lead to the

degradation of device performance. The device leakage of oxide trench fill is caused by the profile of trenches where ideal profile angle is between 78-88°. The angle decreased with increase in thickness of sidewall film buildup and wafer bias power of the etcher. The chamber pressure in the etcher influenced the trench depth nonuniformity. The increase in chamber pressure decreased nonuniformity. The lithography steps prior to etch affected the CDs of the active pattern. Minimum CD variation across the wafer was obtained in a three-step dry development process of TIPS in the formation of resist patterns. Process conditions that affected LER included different resist patterning processes and plasma etch conditions. The LER from the SLR process in resist patterning resulted in lower LER values. During plasma etch, LER decreased with an increase in power. It was observed that LER on the resist layer also occurred on the nitride layer and the silicon substrate after etch. The LER affected the electrical properties of the transistor where an increase in LER increased transistor threshold voltage variation.

In general, from the literature reviewed, process conditions had a direct effect on the STIE characteristics. Better control over the process characteristics can be achieved with further adjustments to process conditions as feature size decrease. Currently there has not been any literature that addresses the relationship between specific plasma etch conditions and line edge roughness. As the CD of devices become smaller, the LER becomes increasingly important. The fact that there are different LER effects between the current 248nm resist and next generation 193nm resist should also be considered. Processing with 193nm resist did not produce the same device characteristics as when

248nm resist was used with the same process conditions. The 193nm resist should be used since it is under development for use with smaller device features. Experiments could be developed to focus on variations in trench etch conditions in the plasma etcher such as gas flow rates of the etch chemistry to control CD and improve LER. The effects of plasma etch chemistries in the STINITE process on LER and CD control of 193nm resist could be investigated.

CHAPTER THREE

RESEARCH HYPOTHESIS AND OBJECTIVES

3.1 Hypothesis

Line edge roughness of active device features after shallow trench isolation etch can be improved by adjusting the gas flow rates of the etch chemistries, CF_4 , CHF_3 , and O_2 , in the shallow trench isolation nitride etch process.

3.1.1 Justification

From the literature review, research has been done on etch conditions and its effects on the shape and profile of the trenches. However, little research has been done to characterize the LER caused by variations in plasma etch conditions. As feature sizes continue to shrink, the LER will continue to have an impact on the semiconductor industry. The concern in industry is that the interaction between the etch chemistries with the 193nm resist causes significant LER which was not an issue when 248nm resist was used. In addition, Palmateer et al. [16] had found that damage from plasma etch after pattern transfer induced LER onto active patterns rather than direct transfer from the resist, even for the 248nm resist. Therefore this experiment looked into the effects of the gas flow rates of etch chemistries in STINITE on LER.

3.2 Objective

This research characterized the quality of the shallow trench isolation etch as a function of LER, CD bias, CD uniformity, and defect number. It was determined if varying gas flow rates in STINITE decreased LER while satisfying the requirements for CD bias, CD uniformity, and defect number of the specified process for integration applications.

CHAPTER FOUR MATERIALS AND METHODS

4.1 Experimental Overview

This thesis proposed an experiment to investigate the effects of varying gas flow rates, CF_4 , CHF_3 , and O_2 , in STINITE on LER and CD control. Patterned wafers were etched with experimental STINITE conditions in a high-density plasma etcher. The characteristics measured after STIE included LER, CD bias, CD uniformity, and defect number. The pictures of the trench profile were also taken. The best STINITE condition was determined based on obtaining the lowest LER, as well as low CD uniformity, low defect number, and a -20nm CD bias^{*}. It was desired to have a low CD uniformity, meaning that the CDs across the wafer are more uniform.

The proposed experiment was planned based on a design of experiment to vary the three gas flow rates, CF_4 , CHF_3 , and O_2 . The results from Bamnolker's prescreening experiment [18] giving the lowest LER and CD uniformity were used to determine reference values for parameters in a screening experiment. Then the condition from the screening experiment that gave the lowest LER with -20nm CD bias, low CD uniformity and defect number was used as the center-point condition for the proposed DOE. The STINITE parameters were held constant at the center-point condition for the proposed experiment except for the gas flow rates of CF_4 , CHF_3 , and O_2 . The wafers were etched based on the experimental conditions and STIE characteristics were measured to determine the best condition. The best condition was determined as the

^{*} The -20nm CD bias is required from the lithography process in order to get the desired CD after etch.

condition that gave the lowest LER as well as a CD bias closest to the -20nm, low CD uniformity and defect number. The results were analyzed to characterize the LER produced from STINITE conditions and any interactions between the etch chemistries with 193nm photoresist that induced LER. The flow chart of the experimental overview is shown in Figure 15.

Figure 15: Flow chart of the experimental plan.

4.2 Experimental Methodology

4.2.1 Screening Experiment

The result from Bamnolker's experiment [18] was used to determine the values that will be used in the screening experiment. Two conditions from Bamnolker's results that produced the lowest LER and lowest CD uniformity were chosen. The first condition is in a low power, low pressure regime with conditions 80mT, 250W, 200sccm Ar flow rate, 2:1 CF₄:CHF₃ flow rate ratio, and total gas flow rate less than 50sccm. The second condition is in a high power, high pressure regime with 200mT, 450W, 100sccm Ar flow, 1:1 CF₄:CHF₃ flow, and total gas flow rate less than 50sccm. Three runs were planned for the low pressure, low power regime where the pressure, power and Ar flow rate were kept constant based on the chosen condition. Then the gas flow rates, CF₄, CHF₃, and O₂, were varied while keeping the CF₄:CHF₃ flow ratio at 2:1 and total gas flow rate less than 50sccm. Another three runs were planned for the high pressure, high power regime where the pressure, power, and Ar flow rate were kept constant. The gas flow rates were varied while keeping the CF₄:CHF₃ flow ratio at 1:1 and total gas flow rate less than 50sccm. The conditions for the six runs in the screening experiment are listed in Table 4. The ratio for CHF₃:O₂ were kept at 2:1 for all runs.

Table 4: Screening conditions for STINITE process in two regimes.

Regime	Gas Flow Rates (sccm)			CF ₄ :CHF ₃ :O ₂ Ratio	Total Flow Rate (sccm)
	CF ₄	CHF ₃	O ₂		
80mT/250W/180Ar	24	12	6	4:2:1	42
	20	10	5	4:2:1	35
	16	8	4	4:2:1	28
200mT/450W/100Ar	12	12	6	2:2:1	30
	10	10	5	2:2:1	25
	8	8	4	2:2:1	20

Six wafers were prepared and processed through STINITE and STIE. The characteristics: LER, CD bias, CD uniformity, and defect number, were measured after STIE. The STINITE condition that produced the lowest LER while achieving the desired CD bias, low CD uniformity, and low defect number was determined. This condition was defined as the center-point condition for the proposed DOE.

4.2.2 Design of Experiment

A design of experiment (DOE) was created for the proposed experiment. The center-point condition determined from the screening experiment gave values for pressure, power, Ar flow rate, and CF₄, CHF₃, and O₂ gas flow rates. The pressure, power, and Ar gas flow rate for were held constant and the gas flow rates of CF₄, CHF₃, and O₂ were varied while keeping the total gas flow rate less than 50sccm. A two-level, full factorial (2³) DOE was proposed for the three factors [19]. The high (+1) and low (-1) values of the DOE for the gas flow rates were determined as the change in the center-point value for each factor by about 20%. The proposed patterns for adjusting the parameters in the 2³ DOE and the center-point condition (0, 0, 0) are listed in Table 5.

Table 5: 2³ DOE table for gas flow rates of STINITE chemistries.

Gas Flow Rates		
CF4	CHF3	O2
0	0	0
-1	-1	-1
-1	-1	1
-1	1	-1
-1	1	1
1	-1	-1
1	-1	1
1	1	-1
1	1	1

Nine wafers were used for the eight runs of the DOE plus one for the center-point condition for comparison. Again the wafers were prepared and processed through STINITE and STIE. The STIE characteristics that were measured were LER, CD bias, CD uniformity, and defect number. After all required measurements were made, the pictures of the cross section of the trench profile were taken on the scanning electron microscope (SEM). This verified if the wafers processed with different STINITE conditions and the same STIE condition had similar trench profiles. The best condition from the results that produced the lowest LER with a -20nm CD bias, low CD uniformity, and low defect number was determined. The DOE was repeated for a total of two runs, or two sets of the DOE.

4.3 Materials and Equipment

4.3.1 Wafers

One wafer was used for each experimental STINITE condition and processed in the wafer fabrication facility at Cypress Semiconductor. These eight-inch silicon wafers were prepared for etch with four layers of materials on top of the silicon starting with oxide, nitride, BARC and patterned 193nm photoresist as shown previously in Figure 3. The photoresist on the wafer was patterned similarly to the diagram of wafer as shown in Figure 16 where the blocks on the wafer represents the dies.

Figure 16: Diagram of wafer with pattern of dies on the surface.

There are smaller features within the dies including arrays as shown in Figure 17a. The STI structures are located in the arrays and this experiment did not involve the other structures surrounding them. The STI structures form a repeating pattern in the arrays as shown in Figure 17b. This figure shows the n-doped metal oxide semiconductor (NMOS) structures as the connected H-shaped structures and p-doped

metal oxide semiconductor (PMOS) structures as the unconnected H-shaped structures. The area of these patterns defined by the photoresist is where the transistors will be built on after etch and further processing. After the wafers have been patterned, the LER and CD of the photoresist structures were measured before STINITE.

Figure 17: Patterns within the dies such as (a) arrays and (b) STI structures at different magnifications.

4.3.2 Process Tools

The equipment used to process the wafers through STINITE, STIE, and cleaning steps are listed in Table 6. A brief description of each tool is also listed.

Table 6: Wafer processing equipment for etch and cleans.

Tool	Use
Centura MXP High Density Plasma Etcher with quartz ring	Etches dielectric layers such as SiO _x , SiN _x , and low K materials using RF power to generate plasma.
Gasonics Oxygen Plasma Asher	Down stream plasma etcher that does not directly expose wafer to the plasma to strip resist or polymers.
Akrion Wet Bench	Contains tanks of recirculating chemistry that removes resist residue.
Lam 4420 Poly Etcher	Etches bare silicon including a breakthrough step to etch buildup of oxide layer.

4.3.3 Measurement Tools

The equipment used to measure and analyze STIE characteristics on the processed wafers are listed in Table 7. A brief description of their uses is also listed.

Table 7: Wafer measurement tools and their use on STI structures.

Tool	Use
AMAT VeraSem 3-D	CD metrology tool that measures CD and LER with scanning electron microscope (SEM).
KLA 2351 Wafer Inspection Tool	Scans for defects on wafer by detecting variations to existing pattern from comparing cells within dies on the wafer.
JEOL SEM	Top down view of wafer using SEM to see structures on the surface of the wafer.
Hitachi SEM	Uses electron beams to capture images of the cross-section of samples of the wafer.

4.4 Analytical Methods

4.4.1 CD and LER Measurements

The CD and LER were measured simultaneously with the VeraSem on 11 sites of the wafer at different radial distances. A map of the wafer divided by a grid and the location of the 11 sites are shown in Figure 18. The CD were measured across the linewidth of the PMOS structure in the array from one edge to the other edge as shown in Figure 19 at each site on the wafer. The figure shows a top down view of the PMOS structure taken from the VeraSem after STIE.

Figure 18: Map of wafer with 11 sites highlighted in black.

Figure 19: PMOS structure with arrow drawn across measurement area.

The CD on the photoresist before etch was measured and the CD after etch on the nitride of the PMOS active pattern was measured. The CD bias or etch bias was determined as $CD\text{ bias} = CD_{\text{after etch}} - CD_{\text{before etch}}$. The desired CD bias was determined from the desired CD on the final active pattern of the nitride layer and the CD obtained before etch on the resist mask. The CD uniformity was determined as three times the standard deviation of CD values measured from the 11 sites. The lower the uniformity value, the more uniform the CDs are across the wafer. The program in the VeraSem calculated LER by Equation 2.

$$roughness = 3 \sqrt{\sigma_{\text{left-edge}}^2 + \sigma_{\text{right-edge}}^2} \quad \text{Equation 2}$$

In Equation 2, σ is the deviation of the CD at edge locations to a fitted line.

4.4.2 Defect Measurement

The number of defects on the wafer were scanned by the KLA 2351 wafer inspection tool. Only the arrays in the dies across the wafer were scanned. The tool was programmed to scan only the STI structures in the arrays and not in the areas surrounding the arrays. The arrays are scanned as smaller cells and these cells are compared between each other within the array. The cells are defined as an area of a certain size with the same repeating pattern for each cell. The first cell is compared to the second cell of the same repeating pattern next to it and the second cell is compared to the third cell next to the second and so on for each die across the wafer. The tool's program detects the defects as variations between the cells with sizes as small as $0.15\mu\text{m}$.

The size, location, and number of the defects were recorded onto a wafer map. The defects of one wafer etched with the center-point condition were reviewed on the

JEOL SEM and top down pictures of each defect were taken. About 50 defects were randomly chosen for review and classified according to defect type. The types of defects that occur after STIE were determined by size, shape, and source of the defect.

4.4.3 Scanning Electron Microscope Cross-Sections

The trenches were etched into the silicon in STIE under the same conditions for all wafers in the proposed experiment. Only the STINITE conditions were different. The profile of the trench should not be affected by STINITE conditions but by STIE conditions and the wafers from the experiment should show the same trench profile. The pictures of trench profile from wafers of each experimental condition were taken to confirm this.

The wafers were cut into smaller samples approximately 1cm x 2.5cm in size for the Hitachi SEM. The pictures of the cross-section of the wafer at the center and edge samples were taken for each wafer. The profile of the trenches for PMOS structures were visually inspected.

4.4.4 Analysis of Variance with JMP

The numerical results of LER, CD bias, CD uniformity, and defect number obtained from the experiment were processed utilizing a statistical analysis program called JMP. The program was used to estimate the effects of the factors and interaction of factors in the 2^3 full factorial DOE. The JMP program used analysis of variance (ANOVA) to calculate response factors for each of the STIE characteristics. The basis of this analysis is to fit the experimental results to a determined model and see how well the results fit the model. ANOVA uses the statistic (F) or F-ratio to test the statistical

significance of variances among means obtained from random samples in the given population of the experimental results. It determined the significance of the variation in the result caused by the change in STINITE condition.

The F-ratio was used in the F-test to test the null hypothesis that the variances of two samples are equal. The F-ratio is the ratio of two s squares, estimates of the population variance. More specifically, it is the ratio of (1) over (2) where

(1) is the estimate in which s square of the obtained means of the samples is multiplied by the size of the samples, and

(2) is the estimate calculated as the average of obtained s squares of the samples.

If the F-ratio is larger than 1, then the variances among the means from the samples are considered statistically significant. This means that it can be determined that the probability of obtaining a variance by chance only is relatively low [20]. The variation in the result due to the change in STINITE conditions was partitioned into several variance components, individual factors that may have had an effect on the behavior of each characteristic. The F-test calculated both an F-ratio and the associated Prob>F value for each factor.

The Prob>F value is the probability or significance ratio for the F-ratio. It is the probability of getting an F-ratio by chance alone or random errors greater than the one calculated if the specified model fits no better than the overall response mean. For Prob>F less than 0.05, there is greater than 95% confidence that the specific factor had a significant effect on the characteristic and that the variation was not due to random errors. In other words, there is >95% chance that the variation was due to the change in

parameter and <5% chance that it was due to errors. The null hypothesis is rejected if Prob>F is less than 0.05, and the variances from two samples do indeed differ significantly [21]. The lower the probability ratio, the more the factor affected the response of the result. It was determined which factor or interaction of factors had more of an effect on LER, CD bias, CD uniformity and defect number. For a more detailed explanation of calculations and background to model fitting in ANOVA and the F-test, refer to references [19] to [21] as listed in the reference section.

CHAPTER FIVE EXPERIMENTAL RESULTS

5.1 Results from Screening Experiment

The summary of results obtained from the screening experiment is listed in Table 8. The average LER and average CD bias was determined from the 11-site measurements of each wafer. The total gas flow rate is the sum of the flow rates of CF_4 , CHF_3 , and O_2 .

Table 8: Summary of STIE characteristics measured from screening experiment.

Pressure/ Power/Ar flow rate	$\text{CF}_4:\text{CHF}_3:\text{O}_2$ flow rate (sccm)	$\text{CF}_4:\text{CHF}_3:$ O_2 Ratio	Total flow (sccm)	LER (nm)	Defect #	CD uniformity (nm)	CD bias (nm)
80mT/250W /180sccm	24:12:6	4:2:1	42	8.7	478	22.1	-28.7
	20:10:5	4:2:1	35	9.6	832	14.8	-34.0
	16:8:4	4:2:1	28	11.3	782	19.3	-34.6
200mt/450 W/100sccm	12:12:6	2:2:1	30	9.1	564	20.2	-5.4
	10:10:5	2:2:1	25	NA	>32000	NA	NA
	8:8:4	2:2:1	20	12.4	>32000	39.2	31.0

The wafer inspection tool is programmed to scan the wafer for a maximum of 32000 defects. Once it reaches 32000 defects, the tool automatically stops scanning the wafer. This happened for two wafers in the screening experiment and the defect number is indicated by >32000. The measurements for LER and CD indicated by NA means that the VeraSem was not able make measurements. The program had difficulty recognizing the pattern in the array and could not find the specific site to be measured. The difficulty in recognizing the pattern was due to under etching of silicon on the wafers. The under etching and >32000 defects occurred in wafers etched in the high power, high pressure regime with gas flow rates 10:10:5sccm and 8:8:4sccm of $\text{CF}_4:\text{CHF}_3:\text{O}_2$. The under

etching of these wafers are shown in the JEOL SEM pictures in Figures 20a and 20b. The surface of the H-shaped PMOS and NMOS structures, which is the nitride layer, maintained a smooth surface. But the area surrounding the structures was partially etched silicon. The partial etching left a coarse or bumpy surface. The silicon surface of the wafer etched in 8:8:4sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$ was much more coarse than the wafer etched in 10:10:5sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$. Residue or film could have remained on the wafer after STINITE blocking the silicon layer underneath from being etched during STIE. This is shown by the light and dark regions in Figures 20a and 20b. Under etching of the wafers eliminated those process conditions from being considered for DOE conditions. These two conditions had the lowest total gas flow rate ($<30\text{sccm}$) from screening conditions.

Figure 20: Top down view of under etching on wafers etched in (a) 10:10:5sccm and (b) 8:8:4sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$ of the high pressure, high power regime.

From the results of the screening experiment, the condition that gave the lowest LER with CD bias near -20nm , low CD uniformity, and low defect number was the condition in the low pressure, low power regime with gas flow rates of 24sccm CF_4 ,

12sccm CHF_3 , and 6sccm O_2 . This condition was designated as the center-point condition for the DOE. The parameters held constant for the DOE were the pressure, RF power, and Ar gas flow rate. The values of these parameters are listed in Table 9. The etch gas flow rates were varied from the center-point values according to the DOE pattern in Table 10. Table 10 lists the values for the gas flow rates, ratios, and total gas flow.

Table 9: Values of parameters held constant in STINITE.

Parameters	Pressure	Power	Ar flow rate
Values	80mT	250W	180sccm

Table 10: Parameters for the DOE determined from center-point condition.

DOE Pattern	Gas flow rates (sccm)			$\text{CF}_4:\text{CHF}_3:\text{O}_2$ Ratio	Total Flow (sccm)
	CF_4	CHF_3	O_2		
center-point	24	12	6	4:2:1	42
---	20	8	4	5:2:1	32
--+	20	8	8	2.5:1:1	36
-+-	20	16	4	5:4:1	40
++	20	16	8	2.5:2:1	44
+--	28	8	4	7:2:1	40
+-+	28	8	8	3.5:1:1	44
++-	28	16	4	7:4:1	48
+++	28	16	8	3.5:2:1	52

5.2 Results from Design of Experiment

5.2.1 STIE Characteristic Measurements

The data obtained from the two sets of the DOE is summarized and listed in Tables 11 and 12 in Appendix A. The LER produced as a result of the different gas flow rate ratios is shown in Figure 21. The CD bias obtained is shown in Figure 22 with the desired CD bias target of -20nm is marked by the solid line. The CD uniformity and defect numbers for both runs are shown in Figures 23 and 24 respectively.

Figure 21: LER from each gas flow rate ratio for both runs.

Figure 22: CD bias from each gas flow rate ratio for both runs.

Figure 23: CD Uniformity from each gas flow rate ratio for both runs.

Figure 24: Defect number from each gas flow rate ratio for both runs.

The results showed the same response in behavior to the change in gas flow rate ratios for both sets of the DOE observed in Figures 21 to 24. The repeatability of the results was excellent between the two runs despite day-to-day variations from the process and measurement tools used in the experiment. The two sets of data for LER and CD bias were repeatable within the standard deviations. The condition that gave the lowest LER and CD bias that was closest to the desired -20nm , along with low CD uniformity and low defect number was the condition with 28sccm CF_4 , 16sccm CHF_3 , and 8sccm O_2 gas flow rates. The $28:16:8\text{sccm CF}_4:\text{CHF}_3:\text{O}_2$ condition was considered to be the best condition from the experiment. The $20:16:4\text{sccm CF}_4:\text{CHF}_3:\text{O}_2$ condition was considered the worst condition since it had the highest LER and a positive CD bias for both sets of the DOE which did not meet the criteria of the experiment.

The best condition, $28:16:8\text{sccm CF}_4:\text{CHF}_3:\text{O}_2$, had the lowest LER and the worst condition, $20:16:4\text{sccm CF}_4:\text{CHF}_3:\text{O}_2$ had the highest LER. Figures 25a and 25b shows VeraSem pictures of LER on PMOS structures within the arrays of the wafers from the first set of the DOE. The figures show structures with 6.5nm LER and 11.9nm LER for comparison between the best and worst conditions. It can be seen that the line edges of the structures were not perfectly straight and smooth. The structure in Figure 25b with the highest LER has an uneven and rougher line edge than the structure with the lowest LER in Figure 25a. The pictures of LER for the rest of the wafers in the first set of the DOE are shown in Appendix D.

Figure 25: VeraSEM pictures of wafers with LER (a) 6.5nm from 28:16:8sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$ and (b) 11.9nm from 20:16:4sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$.

The variation of the CDs was plotted as the STIE CD measured versus the radial distance across the wafer for two conditions in Figures 26 and 27. The range of the CDs on the wafer can be seen for the best condition in Figure 26 and for the worst condition in Figure 27. The best condition had a higher CD uniformity than the worst condition. This means that the CDs from the best condition with the higher CD uniformity value were not as uniform across the wafer. The lower the CD uniformity value, the more uniform the CDs were across the wafer. The solid line in Figures 26 and 27 marks the target STIE CD. It can be seen that the best condition produced CDs closest to the target value and the CDs of the worst condition was the farthest from target.

Figure 26: CD variation of 28:16:8sccm CF₄:CHF₃:O₂ across the wafer.

Figure 27: CD variation of 20:16:4sccm CF₄:CHF₃:O₂ across the wafer.

5.2.2 Defect Review

Defects on the wafer etched with the center-point condition from the first run were reviewed. SEM pictures were taken for 59 out of the 283 defects detected from the scanner. The 59 defects reviewed were randomly chosen out of the 283 total defects scanned on the wafer. The location of the defects for this particular wafer are shown in the wafer map of Figure 28. The wafer map shows that the defects detected were spread across the wafer. The defects were categorized into 5 types: resist mask, cone-shaped, blocked etch, particle etch, and surface defects.

Figure 28: Wafer map of defects scanned from center-point condition wafer.

Defects caused by the resist mask as shown in the top down picture of Figure 29 are categorized as resists mask defects. In this case, the defect came from the resist mask pattern. There was either extra patterning or missing patterns on the mask and the defective pattern gets transferred to the nitride layer after etch.

Figure 29: Top down view of resist mask defect due to defect from patterning.

Defects similar to Figures 30a and 30b where a spike or cone-shaped structure is formed after etch is categorized as a cone-shaped defect. Figure 30b shows a 45 degree tilted view of Figure 30a. The defect looks like a small dot within the pattern in the top down view. This was caused by a tiny particle on the wafer that blocks the etch, forming a spike as shown in the tilted view of Figure 30b. Sources of these tiny particles could occur at the interface between ARC/Nitride, Nitride/Oxide, Oxide/Silicon layers. Defect sources could also be from the film (ARC, Nitride, Oxide) or from particles that remain after the cleaning steps.

Figure 30: Cone-shaped defect in (a) top down view as a small point and (b) tilted view as a spike from the etch.

Blocked etched defects are shown in Figures 31a and 31b. Particle etch defects are shown in Figures 32a and 32b. These defects were caused by etching through larger particles and smaller particles on the wafer. The source of a particle etch defect was a small particle (larger than tiny particles that cause cone-shaped defects) that blocks the etch but does not form a spike as shown in the tilted view of Figure 28b. The source of blocked etch defects were large particles (larger than small particles that cause particle etch defects), pieces, or a cluster of small particles that blocked the etch.

Figure 31: Blocked etch defect from (a) cluster of particles and (b) a larger piece.

Figure 32: Particle etch defect in (a) top down view and (b) tilted view.

Surface defects are particles or residue that appear on the surface, on top of the etched structures as shown in Figure 33. The source of the defects came from particles or residue that were deposited on the wafer. The particles were deposited after the etch since it did not block the etch as shown in Figure 33.

Figure 33: Surface defect as residue on top remaining after etch.

The percentage of the different types of defects found from the 59 defects is shown in Figure 34. The majority of the defects, 67.8%, was due to particle etch. The defects found on the wafer were mostly due to particles or pieces that blocked the etch during STINITE or STIE. The major source of the defects in this process could be from particles or pieces depositing on the wafer before etch.

Figure 34: Defect pareto for 1st set DOE wafer etched with center-point condition.

5.2.3 SEM Cross Sections of STIE Trench Profile

The pictures of trench profiles for PMOS and NMOS structures were taken after STIE for comparison. The pictures taken for each wafer at the center and edge samples of PMOS structures from both runs are shown in Appendix E. Figures 35a and 35b show the PMOS trench profile for the wafer etched with the best condition (28:16:8sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$) from the first set of the DOE at the center and edge. Figures 36a and 36b show the PMOS trench profile for the wafer etched with the worst condition (20:16:4sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$) from the first set of the DOE at the center and edge. Figures 35 and 36 show the nitride layer on top of the silicon layer with a thin oxide layer in between.

(a)

(b)

Figure 35: Trench profile of PMOS for best condition of the first run at (a) center and (b) edge.

(a)

(b)

Figure 36: Trench profile of PMOS for worst condition in the first run at (a) center and (b) edge.

By visual inspection, a comparison between the trench slopes for the different conditions in the first set of the DOE show that all wafers have similar profiles. The center and edge samples of the same wafer also show similar slopes which are circled in Figures 35a and 35b as well as Figures 36a and 36b. The trench profiles from the best and worst condition of the second set of the DOE verified that the second run also show similar trench profiles to the first run. The trench profile of the PMOS structure for the best condition at the center is shown in Figure 37a and the worst condition at the center is shown in Figure 37b.

Figure 37: Trench profile of PMOS from the second run of (a) best condition and (b) worst condition at the center.

The pictures of the profiles verified that the STINITE condition did not affect the slope of the trenches. The slopes of the trenches were entirely dependent on STIE conditions. Since all the wafers were etched with the same STIE condition, there were no significant variations to the profile by visual inspection. The profiles of the trenches show a curve as a result of two slopes. There is a slope at the top of the trench as shown

in Figure 37a and there is another slope at the bottom as shown in Figure 37b which results in a curve of the entire trench profile. The polymerization on the trench sidewalls due to the HBrCl etch chemistry in STIE as well as the top CD of the structures affected the profile and slope of the trenches.

CHAPTER SIX ANALYSIS AND DISCUSSION

6.1 Analysis of DOE Results

The data of LER, CD bias, CD uniformity, and defect number from Tables 11 and 12 in Appendix A was processed in an analysis of variance utilizing JMP. The F-ratio and Prob>F values for each variance component were determined by the F-test. The response values and corresponding STIE characteristics are listed in Table 15 in Appendix C for both runs of the DOE. The variance components included the change from 16 to 28sccm CF₄, 8 to 16sccm CHF₃, 4 to 8sccm O₂, and also the interaction of the parameters: CF₄ with CHF₃, CF₄ with O₂, and CHF₃ with O₂.

The criteria for the effect of the factor to be considered significant in causing variance to the result was for Prob>F to be less than 0.05. That is, the variation in the STIE characteristic is solely dependent on the change in the parameter or interaction of parameters and random errors can be excluded. This was determined so that there was less than 5% chance that the variation of STIE characteristics was due to random errors. There was at least 95% confidence that changing the factors would cause a variation to the LER, CD bias, CD uniformity, or defect number. The assumption for random errors was that it also included day-to-day variations from the process and measurement tools.

6.1.1 LER

For LER variations in the first set of the DOE, the three factors that had a significant effect were CF₄, O₂, and the interaction of CHF₃ with O₂. According to Table 15 in Appendix C, there was less than 1.7% chance that the variation was due to random errors rather than the change in O₂ gas flow rate. There was <3.2% chance the variation

was due to error rather than CF_4 and $<3.5\%$ chance due to errors rather than the $\text{CHF}_3\text{-O}_2$ interaction. The effect of the change in parameters can be visually seen in Figure 38. This plot was obtained from JMP showing the response of LER due to the change in gas flow rates. This shows that the change from 4 to 8 sccm of O_2 gas flow rate caused the greatest change in LER. This plot also includes the average LER = 9nm achieved from the first run.

Figure 38: Response of LER for the change in each gas flow rate.

The interaction effect on LER was also obtained from JMP. Figure 39 shows the plots of the response of LER to gas flow rate interactions: CF_4 with CHF_3 , CF_4 with O_2 , and CHF_3 with O_2 . From this figure, it can be observed there was an interaction between CHF_3 and O_2 with the two plots intersecting each other. This corresponds to the $\text{Prob}>F$ value that indicated significant effects from the $\text{CHF}_3\text{-O}_2$ interaction on LER.

Figure 39: Interaction profiles of gas flow rates on LER.

Estimate values were calculated from the JMP analysis, which is the change in values of LER due to each variance component. When O_2 was increased from 4 to 8sccm, the LER was decreased (negative estimate value) 1.4nm from the average. When CHF_3 was changed from 8 to 16sccm, LER increased (positive estimate value) 0.163nm from the average. The values of the estimates and a pareto plot of the estimates are shown in Figure 40. The larger the absolute value of the estimates, the smaller the Prob>F value, the more of an effect the factor had on LER variations. Figure 40 visually shows the effects of the parameters relative to each other. It can be seen that O_2 had the most effect on LER as compared to the other parameters and the Prob>F value quantified it to be significant.

Figure 40: Pareto plot of LER estimates for each variance component.

In the second run of the DOE, the Prob>F values for LER did not show any factors that were considered significant. From Table 15 in Appendix C, the dominant effect on LER came from O₂ where there was less than 13.3% chance that the variations were due random errors. The behavior of LER due to changing gas flow rates of CF₄, CHF₃ and O₂ is plotted in Figure 41 which shows a similar trend to Figure 38. The average LER for the second run is 9.2nm. The pareto of LER and estimates with the relative effects from each component is shown in Figure 42. This shows that the LER decreased by 1.8nm from the average when O₂ was changed from 4 to 8scm.

Figure 41: Response of LER in Run 2 for the change in each gas flow rate.

Figure 42: Pareto plot of Run 2 LER estimates for each variance component.

The largest effect on LER variations for both sets of the DOE was from O₂ gas flow rates. From Figures 38 and 41, it can be seen that LER decreased with increasing CF₄ gas flow rate, LER increased with increasing CHF₃ flow rate and decreased with increasing O₂ flow rate. The decrease in LER from the change in CF₄ and O₂ gas flow rates was much greater than the increase in LER from CHF₃ gas flow rates. The decrease in LER from O₂ gas flow rates was even greater than the decrease from the CF₄ flow rate. It can be observed from Figures 40 and 42 that the top three factors that had the most significant effect on LER included O₂, the CHF₃-O₂ interaction and CF₄. The change in LER from the average for these three factors had similar values between both runs.

6.1.2 CD Bias

The two factors that significantly affected CD bias in the first run were CHF₃ and O₂. There was less than 3.4% chance that the variation in CD bias was due to random errors rather than the change in CHF₃ flow rate and <1.5% chance due to errors rather than O₂. Figure 43 shows plots of the behavior of CD bias due to the change in gas flow rates. It shows that there is a variation in CD bias due to CHF₃ and O₂ but not much of an effect from CF₄. The average CD bias was -16.5nm. The pareto of estimates for CD bias is plotted in Figure 44 showing the relative order of effect on CD bias for each

variance component. Increasing O_2 from 4 to 8 sccm changed the CD bias 17nm in the negative direction from the average.

Figure 43: Response of CD bias for change in each gas flow rate.

Figure 44: Pareto plot of CD bias estimates for each variance component.

Significant effects on CD bias also came from the change in CHF_3 and O_2 gas flow rates in the second run of the DOE. The response of CD bias is shown in the plots of Figure 45 with little change to CD bias from CF_4 as compared to the other gases. The average CD bias is -17.6nm in the second run. Relative effects between variance components are shown in the pareto of Figure 46 with estimates listed next the corresponding variance component. It can be seen that the greatest effect came from changing CD bias -16.7nm from the average by increasing the O_2 gas flow rate.

Figure 45: Response of Run 2 CD bias for change in each gas flow rate.

Figure 46: Pareto plot of Run 2 CD bias estimates for each variance component.

The major effect on CD bias variations for both runs was from O₂. The response of CD bias in Figures 43 and 45 for both runs show that CD bias increased towards a positive value with increasing CF₄ and CHF₃ flow rate, and decreased towards a negative value with increasing O₂ flow rate. The decrease in CD bias from the O₂ gas flow rate is greater than the increase from CF₄ and CHF₃ gas flow rates. Figure 44 and 46 show that the top three factors with the most effect include O₂, CHF₃, and the CF₄-O₂ interaction. The change in CD bias from the average for both runs was close in value for these three factors.

6.1.3 CD Uniformity

For CD uniformity in the first set of the DOE, none of the parameters met the criteria for having significant effects based on Prob>F values of Table 15 in Appendix C. But out of all parameters, CF₄ had the largest effect on CD uniformity variations with the lowest Prob>F value. Figure 47 clearly shows that there was not much change in CD uniformity with respect to the change in each of the gas flow rates. The average CD uniformity was 14.8nm. Figure 48 lists the scaled estimates and shows the pareto of CD uniformity for the different variance components. The plot of the effects are relative for each component, but does not quantify the significance of their effects on CD uniformity variations. Changing CF₄ from 20 to 28sccm increased CD uniformity by 1.8nm from the average.

Figure 47: Response plot of CD uniformity for change in each gas flow rate.

Figure 48: Pareto plot of CD uniformity estimates for each variance component.

In the second set of the DOE, the change in CHF_3 had the most significant effect on CD uniformity. Figure 49 shows the response of CD uniformity due to changing gas flow rates with the greatest effect from CHF_3 . The average CD uniformity is 15.8nm. The pareto plot of estimates for CD uniformity is shown in Figure 50. An increase of CHF_3 decreased CD uniformity by 2.6nm from the average.

Figure 49: Response of Run 2 CD uniformity for change in each gas flow rate.

Figure 50: Pareto plot of Run 2 CD uniformity estimates for each variance component.

The major effect on CD uniformity variations was caused by CF_4 in the first run and by CHF_3 in the second run. Figure 47 shows that for the first run, increasing CF_4 increased CD uniformity, increasing CHF_3 barely changed it, and increasing O_2 increased CD uniformity. Figure 49 shows that for the second run, increasing CF_4 increased CD uniformity, increasing CHF_3 decreased it and increasing O_2 also decreased CD uniformity. The top three factors with the greatest effect on CD uniformity differed

between the two runs. As shown in Figure 48 the top three factors in first run are CF_4 , the $\text{CF}_4\text{-O}_2$ interaction, and O_2 , whereas for the second run in Figure 50 the top three factors are CHF_3 , CF_4 , and the $\text{CF}_4\text{-O}_2$ interaction. But it can be observed that the change in CD uniformity from the average due to CF_4 only for both runs had approximately the same change in value from the average.

6.1.4 Defect Number

The Prob>F values of the first run did not show any significant effects on defect number from any of the parameters. O_2 had the largest effect on variations with less than 27.1% chance of variation was due to errors rather than O_2 . The behavior of the change in defect numbers for the three gas flow rates of the first set of the DOE is shown in Figure 51. The average defect number is 316. The pareto of estimates for defect number is shown in Figure 52. The change in O_2 from 4 to 8 sccm increased the number of defects by 65 from the average.

Figure 51: Response of defect # for change each in gas flow rate.

Figure 52: Pareto plot of defect # estimates for each variance component.

The parameters O₂ and CHF₃ gas flow rates had significant effects on the number of defects in the second run. The most significant effect was from O₂ where there was less than 1.6% chance that the variations were due to errors. Figure 53 shows plots of the response of defect number to the change in gas flow rates. The average defect number is 333. Figure 54 shows the pareto plot for defect number. The change in O₂ from 4 to 8 sccm had the most effect on defect number by increasing the number 63 from the average.

Figure 53: Response of Run 2 Defect # for change in each gas flow rate.

Figure 54: Pareto plot of Run 2 defect # estimates for each variance component.

For both runs, O₂ had a major effect on defect number variations. Both Figures 51 and 53 show the same response in defect number for both runs. The behavior shown is that defect number decreased with increasing CF₄, decreased with increasing CHF₃ and increased with increasing O₂. The increase in defect number from increasing O₂ gas flow rate is greater than the decrease from CF₄ and CHF₃ gas flow rates. It is shown in Figures 52 and 54 that the top three factors with the most effect on defect number are O₂, CHF₃, and the CHF₃-O₂ interaction. The effect of O₂ in both sets of the DOE resulted in similar values for the change of defect number from the average. But as for the CFH₃-O₂ interaction, the defect number increased from average in the first run and decreased from the average in the second run.

6.2 Discussion of Significant Effects

6.2.1 Effects of O₂ on STIE Characteristics

From the analysis in JMP, it can be seen that the common factor with the greatest effect on variations of STIE characteristics was the change in the O₂ gas flow rate. The O₂ flow rate had a dominant effect on LER, CD bias, and defect number as presented in previous sections. Only CD uniformity was the affected the most by the CF₄ flow rate in

the first run and by the CHF₃ flow rate in the second run. From this comparison, it cannot be determined that the same factors had an effect on CD uniformity.

When the O₂ gas flow rate increased, the CD bias became more negative. This meant that the absolute difference between the CD before etch and CD after etch was greater. When the CHF₃ gas flow rate increased, the CD bias changed towards the positive direction. The STIE CD did not decrease as much from STINITE CD (some were even greater than STINITE CD) so that the absolute difference between the CD before etch and CD after etch was smaller. Since CHF₃ is a polymerizing gas, the increase in the CHF₃ flow rate created a build up of sidewall polymers resulting in an anisotropic etch. Larger STIE CD was obtained for CHF₃ gas effects since polymers prevented etching away of the nitride in the lateral direction. On the other hand, the increase in the O₂ flow rate helped etch away the sidewall polymers as well as the resist pattern, exposing nitride to the plasma. Lateral etching occurred in the case which lead to a smaller STIE CD. This is from the principle that O₂ is used to etch away organic materials and strip photoresist. Based on the results, the increase in the O₂ gas flow rate decreased LER. The correlation between LER and STIE CD was that LER decreased and CD increased with an increase in O₂. The increase in the O₂ gas flow rate did not induce as much of a roughness on the resist during etch as it increased the STIE CD.

For both runs of the DOE, the LER decreased with increasing CF₄ gas flow rate, increased with increasing CHF₃ flow rate and decreased with increasing O₂ flow rate. But the decrease in LER from the change in O₂ flow rate was much greater than the increase from CHF₃ flow rate and decrease from CF₄ flow rate. This was indicated by

the result that the best condition was the 28:16:8sccm CF_4 : CHF_3 : O_2 condition, where the three gas flow rates have been increased. Therefore this condition with the high value of the O_2 gas flow rate gave the lowest possible LER from the experiment. In the case of defect numbers for both runs, the defect number decreased with increasing CF_4 flow rate, decreased with increasing CHF_3 flow rate and increased with increasing O_2 flow rate. But the increase in defect number from O_2 gas flow rate was greater than the increase from CF_4 and CHF_3 gas flow rates. This is a sign of a tradeoff in determining that the 28:16:8sccm CF_4 : CHF_3 : O_2 condition was the best condition. Since the gas flow rates were increased in this condition, then the increase in defect number was greater with the increase in the O_2 flow rate. But the greater the O_2 flow rate in the best condition helped to maintain a lower LER. In order to achieve the lowest LER, other characteristics were compromised so that it may not give the lowest CD uniformity or defect number. The tradeoff in obtaining the lowest LER was to have an increase in defects on the wafer. Though the CD uniformity and defect number were not the lowest, it was still acceptable since it was within the specifications of STIE.

6.2.2 Factors That Affected LER

It was found that the change in gas flow rates in STINITE had a significant effect on the response of LER. The question here is whether the O_2 , CF_4 , or CHF_3 gas, or a combination of these gases interacted with the 193nm photoresist to cause LER. Comparisons between conditions in Figure 21 in the result section with the same CF_4 and CHF_3 gas flow rates but different O_2 gas flow rate showed that increasing the O_2 flow rate decreased LER. This means that the increase of the O_2 concentration in the etch

chemistry caused a decrease in LER. This could be related to the O_2 effects on etch rates. The concept is that if a small concentration of O_2 is added to the feed gas, the etch rate of the substrate increases. But if the increase in the O_2 concentration is much larger, the O_2 dilutes the fluorine concentration in the gas which decreases the etch rate. The etching of the substrate is primarily done by fluorine (F) atoms in the plasma produced by the dissociation of CF_4 molecules. And the addition of CHF_3 in the gas feed helps to control the selectivity of the etch. The addition of O_2 is also accompanied by the increase in density of F-atoms in the plasma. The reaction between O_2 atoms or molecules and CF_4 fragments (CF_x , where $x \leq 3$) causes an increase in the F concentration and thus decreases the CF_x fragments in the gas phase. This leads to the decrease in the recombination rates of F and CF_x . The increase in F concentration in turn would cause higher etch rates. As the O_2 concentration increases to about 12% O_2 (by volume), the etch rate continues to increase to a maximum when about 20% O_2 is reached. The addition of O_2 greater than that dilutes the F concentration and decreases the etch rate.

The LER measured on the resist before etch was less than the LER measured on the substrate after etch. The data for this can be found in Table 13 of Appendix A. This confirms that the STINITE chemistries were causing the increase in LER. The assumption is that during the plasma etch, the chemistries interacted with the 193nm photoresist which increased the roughness on the resist, and the increase in LER gets transferred to the substrate. The different gas flow rate ratios from the STINITE conditions suggested that the different concentrations of the etch chemistries resulted in different etch rates of nitride. The variation in etch chemistry concentration had some

sort of interaction with the 193nm resist to induce the different LER observed in Figure 21. During STINITE, some of the resist was etched away at a lower rate as the nitride was being etched. The etching of the resist could also be an indication of the interaction between the etch chemistries and the resist that occurred. An increase in the O_2 concentration would etch away more of the resist during etch resulting in a decrease in STIE CD due to the increase in the size of the resist pattern. The amount of resist being etched away probably affected how much LER was induced on the 193nm resist during STINITE.

The interaction between the etch chemistries and 193nm resist could be tied to the effect of the change in O_2 gas flow rate on LER. The behavior observed was that LER decreased with increasing the O_2 gas flow rate no matter what the flow rate ratio was or whether the CF_4 or CHF_3 gas flow rates were high or low. The effect of O_2 on LER might not be from a direct interaction, but may be the inhibition of other chemistries from interacting with the resist. When increasing the O_2 gas flow rate diluted the other gases, the magnitude of the chemistry-resist interaction to induce LER was not as great. Figure 38 shows that increasing the CF_4 gas flow rate decreased LER and increasing the CHF_3 gas flow rate increased the LER. This suggests that the most important interaction was between CHF_3 and 193nm resist that increased LER. Figure 39 indicated that there was an interaction between CHF_3 and O_2 . This may imply that the increase in the O_2 concentration acted as an inhibitor to CHF_3 that was increasing the LER on the resist.

At this point, it can be established that the CHF_3 gas was interacting with the 193nm resist to induce LER and the addition of O_2 gas inhibited the magnitude of the

effect. The increase in the CHF_3 gas flow rate increased LER whereas the increase in the O_2 gas flow rate decreased LER. CHF_3 is a polymerizing gas which deposits polymers to the sidewalls of etched areas. As a result of this concept, the STIE CD was smaller since lateral etching was blocked by the polymers. The polymers from the increase in CHF_3 could have deposited on the sidewalls of the resist mask to form a rougher surface. Then the sidewall roughness on the resist was transferred to the substrate during etch. The increase in the O_2 concentration could have etched the deposited polymers and thus reduced the LER. O_2 inhibited the effects of CHF_3 in the buildup of polymers.

6.2.3 Gas Flow Rate Ratio or Total Flow Rate Effects

Referring back to Figures 21 to 24 in the result section, the best condition determined for both sets of the DOE was 28:16:8sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$. It was considered to be better than the designated center-point condition from the screening experiment. With a comparison between these two conditions, it was observed that the gas flow rate ratios for the center-point condition was 4:2:1 and the 28:16:8sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$ condition had a 3.5:2:1 ratio. But the total gas flow rate showed that the best condition had a greater total gas flow rate than the center-point condition by 10sccm. If the ratios were assumed to be relatively the same, this could mean that the conditions with the same ratio could decrease LER by increasing the total gas flow rate. It had already been observed from the results of the screening experiment that conditions with less than 30sccm total gas flow rate resulted in a higher LER along with undesirable CD bias, CD uniformity, and defect number. The best condition, 28:16:8sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$, had the highest total gas flow rate overall in the DOE and screening experiment. The rate at

which the gases were flowing through the etch chamber had an effect on the LER. The way the etch chemistries bombarded the surface of the wafers, affected by the total gas flow rate, may have interacted with the resist differently.

Now consider what if ratios 4:2:1 versus 3.5:2:1 were significantly different in affecting how the chemistries interacted with 193nm resist. The $\text{CF}_4:\text{O}_2$ ratio in the best condition, 28:16:8sccm $\text{CF}_4:\text{CHF}_3:\text{O}_2$, was lower with a ratio of 3.5:1 compared to the center point condition with a 4:1 $\text{CF}_4:\text{O}_2$ ratio. The O_2 concentration was greater in the best condition than the center-point condition. Again this leads to the fact that the increase in the O_2 concentration decreased LER after etch. And this could be associated with the assumption that if the CHF_3 gas was interacting with the 193nm resist then the increase in the O_2 concentration inhibited this interaction.

CHAPTER SEVEN CONCLUSION

7.1 Conclusion

The growing trend in the semiconductor industry is to make devices smaller and smaller so that it will work faster. This has lead to strict process requirements to make the devices work correctly. The smaller the devices become the more critical the device or process characteristics become. The characteristics throughout the fabrication processes of the device affect the way the device performs. Process characteristics of concern in particular to STIE include LER, CD bias, CD uniformity, and defect number. STIE is the etch step in the shallow trench isolation process that creates isolation trenches in which the actual devices are built on. The fabrication of CMOS transistors currently requires the use of STIE.

One important issue in the lithography and etch processes is LER. The width of the lines of device structures continue to shrink so that the current 248nm photoresist used to pattern the structures can no longer be used. Another resist under development for this, the 193nm photoresist, is used for dimensions smaller than $0.25\mu\text{m}$. As research is being conducted on the use and integration of 193nm resist in IC fabrication processes, the issue of controlling LER currently continues to come up. LER is the roughness found on the line edges of device structures. This roughness may hinder the performance of the final device and cause it to fail. As line widths become smaller, the effect of LER becomes more significant.

Literature review on past research indicates that tests have been done on varying parameters in the lithography steps to control LER. Some research such as that from Kim

et al. [16] and Palmateer et al. [17] showed that LER may be affected by resist development conditions and plasma damage during etch. Currently, there is no published literature investigating how etch chemistries interact with 193nm resist and how that causes LER. In STIE, LER appears on the nitride hardmask as it is transferred from the resist during etch. There must be a means of controlling this by varying etch parameters. In unpublished studies by Bamnolker [19], it was found that LER from the 193nm resist increased after STINITE, nitride etch, but remained relatively the same after STIE. This indicated that the etch conditions on the 193nm resist during STINITE induced an increase in LER. For the research in this thesis, a screening experiment and a design of experiment was proposed based on the results from Bamnolker's experiment to further expand on the understanding of this finding.

The purpose of the experiment was to characterize STIE LER and analyze how STINITE conditions affected STIE characteristics. The effects of varying gas flow rates of etch chemistry in obtaining desired LER, CD bias, CD uniformity, and defect number was analyzed. The screening experiment was used to determine the values at which to keep certain STINITE parameters constant. The best condition from this was used to keep pressure, power, and Ar flow rate constant while varying only the gas flow rate ratios of CF_4 , CHF_3 , and O_2 . The design of experiment used the gas flow rates of the best condition from the screening experiment as the center-point in designing the two-level, three-factor DOE. The desired results from these experiments were to produce the lowest LER while meeting the required -20nm CD bias as well as maintaining a low CD uniformity and a low defect number.

The best condition achieved from the two runs of the DOE was the STINITE condition with gas flow rates of 28sccm CF₄, 16sccm CHF₃, and 8sccm O₂. This condition gave the lowest LER, CD bias closest to -20nm, a low CD uniformity, and a low defect number. It was determined that the condition gave a lower LER while meeting other characteristic requirements, than what was achieved from the center-point condition from the screening experiment.

The data from the result of the experiment was entered into the JMP program for the F-test in ANOVA. Response factors, Prob>F, were determined for each variance component such as the change in gas flow rates and interactions between two parameters. This gave the percentage of chance that the variation in the characteristic was due to random errors rather than by the STINITE condition. The Prob>F values less than 0.05 was the criteria to consider that the variance component had a significant effect on the behavior of the result. For example, LER variations in the first set of the DOE gave Prob>F value of 0.017 for O₂. This means that there was less than 1.7% chance that the LER variation is due to random errors and greater than 98.3% chance that LER was affected by the change in O₂.

From this analysis it was observed that similar behaviors in the result for both runs of the DOE occurred. Some effects of the variance components on the characteristics were more significant than others and the degree of the effect relative to each other was categorized. The major effect in both sets of the DOE on LER, CD bias, and defect number came from the change in the O₂ gas flow rate. The tradeoff in obtaining the lowest LER was an increase in defects with increasing O₂ for the best

STINITE condition. The values of Prob>F for CD uniformity gave different factors for both runs with the greatest effect on its variations. In this case, it could not be verified which single factor had the most effect on CD uniformity variations.

The single factor that had the most dominant effect on LER was the O₂ gas flow rate. It was observed that the increase in O₂ decreased LER. The difference between the LER on the resist before etch and the LER on nitride after etch suggested that there was an interaction between the etch chemistries and 193nm resist that caused the increase in LER. The CHF₃ and CF₄ gases may have directly induced LER so that when the O₂ concentration increased, there was an inhibition to inducing LER. The difference in gas flow rate ratios or concentration of the etch chemistries produced different etch rates on the nitride and resist. The difference in etch rates between the conditions could be related to the amount of LER induced during the etch. This is based on results that increasing O₂ concentration decreased LER and the concept of the O₂ effects on changing substrate etch rate. Another relation of LER to etch gas concentrations could be from the polymerization of CHF₃ gas. It was established that the CHF₃ gas was interacting with the 193nm resist to induce LER and the addition of O₂ gas inhibited the magnitude of the effect.

CHAPTER EIGHT FUTURE WORK

8.1 Suggestions for Future Work

Based on the analysis of the results, some points of interest for this research came up. These issues may help in the understanding of what affects STIE characteristics. This also touches on the subject of the interaction between etch chemistries and 193nm photoresist. Future work could be done on such issues to further decrease LER as well as better characterize or control STIE characteristics for process integration.

8.1.1 Plasma Etch Conditions

From literature reviewed, research have been mostly done on lithography conditions to find sources for LER. But it was found that there were direct effects of the plasma or etch chemistries on the 193nm resist to induce LER. At this point, the characterization of LER with chemistry and gas flow rate effects was achieved but details to the mechanisms in the chemical interaction with 193nm resist could not be determined. Development of studies based on this experiment to further understand the basis for such interactions could be done. More tests could be performed to help determine the adjustment in the STINITE process to fine tune the control over LER while maintaining the desired characteristics such as CD bias, CD uniformity, and defect number for process integration.

8.1.2 CD Uniformity Variations

CD uniformity variations were affected by the CF_4 gas flow rate in the first run of the DOE and the CHF_3 gas flow rate in the second run. The response of the CD uniformity changed when it was repeated in the second run. The order of relative effect

on CD uniformity by each variance component differed between the first and second run. Depending on whether or not the response of CD uniformity for running STINITE with the best condition could still satisfy the required specification, more work could be done to address the issue of what affects CD uniformity variations.

The fact that the most effect from the CF_4 gas flow rate in the first run could not be considered significant implies that there was at most a 31.1% chance that the variations were due to random errors. To verify whether the gas flow rates really had an effect on CD uniformity, the experiment could be repeated. Then it could be verified if the CHF_3 flow rate had the most significant effect on CD uniformity variations as implicated by the result of the second run. If again there is an uncertainty in the response of CD uniformity, then this suggests that other factors had an effect on variations rather than changing the gas flow rates alone. More tests would have to be considered to find out what other factors may have an effect.

8.1.3 Etch Rate Effects on LER

The etch chemistries: O_2 , CF_4 , or CHF_3 gas or a combination of these gases may have had an interaction with the 193nm resist to cause LER. It is known that a change in the gas flow rate ratios or concentrations affected the rate of etching for both resist and nitride. The etch rate increases or decreases depending on the concentration of O_2 in the feed gas. The increase in the O_2 concentration in the experiment decreased the LER. The LER after etch was still greater than the LER before etch, this means that the increase in the O_2 concentration did not induce as much of a roughness on the structure than the decrease in O_2 concentration.

There could be some sort of correlation to how fast the resist and substrate was being etch compared to the LER that was formed. But further experiments should be conducted with these parameters to verify the correlation. One of the first experiments to do would be to determine the quantity of how small O₂ concentration needs to be to increase etch rate and how large the O₂ concentration needs to be when it starts to dilute the fluorine concentration and decrease the etch rate. At the same time it would be necessary to determine the change in LER for when etch rate is increased and decreased according to the different O₂ concentrations. Correlating the etch rate affected by the concentration of the gases and LER would help in getting an idea of how the gases may interact with the resist during etch.

8.1.4 Flow Rate Effects on LER

From the conditions of the DOE, the best condition had the highest total gas flow rate overall. Based on the results, it was observed that the ratio of the gas flow rates as well as the total gas flow rate had an effect on LER. It had already been observed in the screening experiment that conditions with total gas flow rates less than 30sccm produced higher LER and undesirable characteristics.

The question here is whether keeping the same ratio for the best condition but increasing the total gas flow rate would improve LER. More experiments would have to be developed to confirm this by testing conditions with the same gas flow rate ratios, but varying the total gas flow rates at greater flow than that of the current best condition. It could be determined if increasing the total gas flow rate decreases LER and how much more increase in flow rate is needed. It can be observed if increasing the total gas flow

rate can still keep the other STIE characteristics within control. To address the question if the ratios 3.5:2:1 and 4:2:1 for the gases $\text{CF}_4:\text{CHF}_3:\text{O}_2$ would have significantly different results, another test could be done simultaneously. The best condition and the center-point condition with these ratios could be run with higher total gas flow rates of the same values for both conditions.

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APPENDIX A

Data Collected from STINITE DOE

The summary of LER and CD bias with standard deviations for both runs is listed in Table 11. The LER and CD bias values are averages determined from the 11-site measurements on each wafer of each condition. The summary of CD uniformity and defect number for both runs is listed in Table 12.

Table 11: Average STIE LER and CD bias measured from both sets of the DOE.

CF ₄ :CHF ₃ :O ₂ Flow Rates (sccm)	LER (nm)		CD bias (nm)	
	<i>Run 1</i>	<i>Run 2</i>	<i>Run 1</i>	<i>Run 2</i>
24:12:6	7.9±1.4	8±1.1	-15.3±3.8	-10.6±4
20:8:4	10.6±2.6	9.8±1.7	-4.4±4.7	-4.6±4.4
20:8:8	8.8±1.6	8.5±2.3	-44.8±4.5	-43.7±4.2
20:16:4	11.9±2.6	12.7±2.2	8.9±4.6	5.1±3.1
20:16:8	7.5±1.5	7.3±0.9	-30±3.4	-39.9±3.6
28:8:4	8.5±1.7	10.2±1.8	-8.3±4.4	-7.8±6.2
28:8:8	7.3±2.1	7±1.4	-38.9±4.9	-38.1±5.4
28:16:4	10.6±2.5	11.1±1.3	5.6±4.4	3.9±4.2
28:16:8	6.5±1.2	6.8±1.1	-20.3±3.8	-25.4±4.7

Table 12: CD uniformity and defect number measured from both sets of the DOE.

CF ₄ :CHF ₃ :O ₂ Flow Rates (sccm)	CD uniformity (nm)		Defect #	
	<i>Run 1</i>	<i>Run 2</i>	<i>Run 1</i>	<i>Run 2</i>
24:12:6	12	13.2	283	359
20:8:4	9.8	18.7	333	281
20:8:8	15.7	15.6	384	441
20:16:4	11.4	11.5	182	270
20:16:8	15.4	10.3	410	361
28:8:4	19.5	19	278	273
28:8:8	15.3	20.1	430	427
28:16:4	15.1	14.7	212	255
28:16:8	16.5	16.5	304	353

Table 13 lists the data that was measured during STINITE and STIE with corresponding STINITE conditions and wafer number for both runs.

Table 13: Data collected before and after STIE for both sets of the DOE.

Wfr #	STINITE CF ₄ :CHF ₃ :O ₂			LER (nm)			STIE Defect #	Average CD (nm)			CD Bias (nm)	stdev	STIE CD Uniformity (nm)
	Gas Flows (sccm)	Ratio	Total Flow (sccm)	before	after STIE	stdev		before	stdev (nm)	after STIE			
1st set of DOE	6	24:12:6	4:2:1	42	5.32	7.88	1.4	283	155.2	3.4	139.9	4.0	3.76
	5	20:8:4	5:2:1	32	5.22	10.56	2.6	333	156.1	3.5	151.7	3.3	4.65
	3	20:8:8	2.5:1:1	36	5.11	8.84	1.6	384	158.2	3.1	113.4	5.2	4.45
	7	20:16:4	5:4:1	40	5.55	11.85	2.6	182	154.4	2.3	163.3	3.8	4.61
	8	20:16:8	2.5:2:1	44	4.94	7.47	1.5	410	154.1	5.0	124.1	5.1	3.36
	9	28:8:4	7:2:1	40	5.55	8.47	1.7	278	153.9	4.9	145.6	6.5	4.43
	10	28:8:8	3.5:1:1	44	4.95	7.3	2.1	430	153.5	3.9	114.6	5.1	4.91
	11	28:16:4	7:4:1	48	5.1	10.64	2.5	212	153.7	3.2	159.3	5.0	4.41
	4	28:16:8	3.5:2:1	52	4.39	6.54	1.2	304	156.3	4.1	136.0	5.5	3.82
	12	24:12:6	4:2:1	42	5.36	7.97	1.1	359	152.0	4.9	141.4	4.4	3.96
2nd set DOE	13	20:8:4	5:2:1	32	4.75	9.8	1.7	281	152.1	5.9	147.5	6.2	4.36
	14	20:8:8	2.5:1:1	36	5.23	8.49	2.3	441	152.7	3.6	109.0	5.2	4.16
	15	20:16:4	5:4:1	40	5.46	12.67	2.2	270	153.3	2.7	158.4	3.8	3.06
	16	20:16:8	2.5:2:1	44	4.84	7.26	0.9	361	153.4	3.2	123.5	3.4	3.59
	17	28:8:4	7:2:1	40	4.68	10.23	1.8	273	152.6	4.0	144.8	6.3	6.18
	18	28:8:8	3.5:1:1	44	4.54	6.97	1.4	427	153.2	2.9	115.1	6.7	5.43
	19	28:16:4	7:4:1	48	5.6	11.13	1.3	255	151.3	3.1	155.2	4.9	4.23
	20	28:16:8	3.5:2:1	52	4.95	6.81	1.1	353	152.0	3.8	126.6	5.5	3.68

APPENDIX B

Spec Limits for STIE Characteristics

The limits and targets for the STIE characteristics to monitor the STI process is listed in Table 14. These values were determined for the integration of STIE into the overall device fabrication. USL is the upper spec limit and LSL is the lower spec limit. The $CD_{\text{before etch}}$ is the CD on the resist before etch and $CD_{\text{after etch}}$ is the CD on the nitride substrate after STIE.

Table 14: Spec limits and targets for STIE characteristics.

Characteristic	USL	LSL	Target
$CD_{\text{before etch}}$	172nm	128nm	150nm
$CD_{\text{after etch}}$	155nm	105nm	130nm
STIE LER	12nm	0.1nm	9nm
STIE Defect #	450	0	250

APPENDIX C

Response Factors from the F-test

The F-ratio and Prob>F values are listed in Table 15 for LER, CD bias, CD uniformity, and defect number. The response from variance components are listed for both runs.

Table 15: Variance components and corresponding response factors from both runs.

Source of Variance	Run 1		Run 2	
	F Ratio	Prob>F	F Ratio	Prob>F
LER				
CF ₄ (20,28)	386.778	0.032	1.138	0.479
CHF ₃ (8,16)	18.778	0.144	0.640	0.570
O ₂ (4,8)	1469.444	0.017	22.404	0.133
CF ₄ (20,28)*CHF ₃ (8,16)	18.778	0.144	0.111	0.795
CF ₄ (20,28)*O ₂ (4,8)	9.000	0.205	0.071	0.834
CHF ₃ (8,16)*O ₂ (4,8)	336.111	0.035	3.004	0.333
CD Bias				
CF ₄ (20,28)	6.891	0.232	3.381	0.317
CHF ₃ (8,16)	358.629	0.034	238.752	0.041
O ₂ (4,8)	1800.941	0.015	1860.113	0.015
CF ₄ (20,28)*CHF ₃ (8,16)	1.891	0.400	0.084	0.820
CF ₄ (20,28)*O ₂ (4,8)	50.766	0.089	21.878	0.134
CHF ₃ (8,16)*O ₂ (4,8)	3.754	0.303	2.707	0.348
CD Uniformity				
CF ₄ (20,28)	3.534	0.311	140.028	0.054
CHF ₃ (8,16)	0.064	0.842	289.000	0.037
O ₂ (4,8)	0.896	0.517	1.361	0.451
CF ₄ (20,28)*CHF ₃ (8,16)	0.360	0.656	14.694	0.162
CF ₄ (20,28)*O ₂ (4,8)	2.867	0.340	36.000	0.105
CHF ₃ (8,16)*O ₂ (4,8)	0.243	0.708	4.694	0.275
Defect #				
CF ₄ (20,28)	0.129	0.781	11.982	0.179
CHF ₃ (8,16)	1.789	0.409	198.160	0.045
O ₂ (4,8)	4.870	0.271	1497.095	0.016
CF ₄ (20,28)*CHF ₃ (8,16)	0.080	0.825	0.006	0.951
CF ₄ (20,28)*O ₂ (4,8)	0.022	0.907	0.006	0.951
CHF ₃ (8,16)*O ₂ (4,8)	0.244	0.708	92.456	0.066

APPENDIX D
Top Down VeraSem Pictures for the First Set of the DOE

(a) W#6 center

(b) W#6 edge

Figure 55: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#6 from the first run.

(a) W#5 center

(b) W#5 edge

Figure 56: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#5 from the first run.

(a) W#3 center

(b) W#3 edge

Figure 57: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#3 from the first run.

(a) W#7 center

(b) W#7 edge

Figure 58: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#7 from the first run.

(a) W#8 center

(b) W#8 edge

Figure 59: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#8 from the first run.

(a) W#9 center

(b) W#9 edge

Figure 60: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#9 from the first run.

(a) W#10 center

(b) W#10 edge

Figure 61: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#10 from the first run.

(a) W#11 center

(b) W#11 edge

Figure 62: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#11 from the first run.

(a) W#4 center

(b) W#4 edge

Figure 63: PMOS structures showing STIE LER at (a) center and (b) edge of wafer#4 from the first run.

APPENDIX E
SEM Cross-Section Pictures of STIE Trench Profile

(a) W#6 center

(b) W#6 edge

Figure 64: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#6 of the first run.

(a) W#5 center

(b) W#5 edge

Figure 65: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#5 of the first run.

(a) W#3 center

(b) W#3 edge

Figure 66: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#3 of the first run.

(a) W#7 center

(b) W#7 edge

Figure 67: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#7 of the first run.

(a) W#8 center

(b) W#8 edge

Figure 68: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#8 of the first run.

(a) W#9 center

(b) W#9 edge

Figure 69: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#9 of the first run.

(a) W#10 center

(b) W#10 edge

Figure 70: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#10 of the first run.

(a) W#11 center

(b) W#11 edge

Figure 71: Cross-sections of trench profile on PMOS structures at (a) center and (b) edge for wafer#11 of the first run.

(a) W#15 center

(b) W#15 edge

Figure 72: Cross-sections of PMOS trench profile at (a) center and (b) edge for wafer#15 of the second run.

(a) W#20 center

(b) W#20 edge

Figure 73: Cross-sections of PMOS trench profile at (a) center and (b) edge for wafer#20 of the second run.