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Thermal design improvement of bipolar power transistors with Si²⁸ isotopes

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THERMAL DESIGN IMPROVEMENT
OF BIPOLAR POWER TRANSISTORS
WITH Si²⁸ ISOTOPES

A Thesis
Presented to
The Faculty of the Department of
General Engineering
San Jose State University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science

By
Larry C. Olsen

August 2004

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A handwritten signature in black ink, appearing to read "Peter Reischl", written over a horizontal line.

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ABSTRACT

THERMAL DESIGN IMPROVEMENT OF BIPOLAR POWER TRANSISTORS WITH Si²⁸ ISOTOPES

by Larry C. Olsen

The power-handling capability of a bipolar power transistor is limited primarily by the ability of the power transistor to dissipate heat and distribute the thermal energy within the transistor evenly. Excessive heat in a heterojunction bipolar transistor (HBT) can cause the collector current to collapse. By improving the thermal conductivity of the semiconductor substrate on which the device is built, the *pn* junction temperatures can be lowered, and the thermal energy can be more evenly distributed throughout the transistor. AlGaAs/GaAs power HBTs usually are built on a silicon substrate to improve the transistor thermal conductivity because natural mixed-isotope Si has a thermal conductivity 2.6 times better than GaAs. Purified mono-isotope Si²⁸, however, has a thermal conductivity 1.6 times better than natural mixed-isotope Si, or 4.2 times better than GaAs. Therefore, designing a power HBT on a Si²⁸ substrate will further improve the thermal properties.

This assertion is proven with a thermal analysis computer simulation of a 5-emitter finger AlGaAs/GaAs power HBT, designed with emitter ballast resistors on a Si²⁸ substrate. The analysis reveals a new power transistor design that can produce higher output currents with smaller emitter ballast resistors before reaching thermal instability.

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TABLE OF CONTENTS

Abstract	iv
Acknowledgements	v
List of Figures	vii
List of Variables	xiii
Chapter	page
1. Introduction	1
2. Semiconductor Isotopes	4
2.1 Isotopes Defined	4
2.2 Si ²⁸ and Ge ⁷⁰ Thermal Conductivity	5
2.3 The Isotope Industry	8
3. Bipolar Power Transistor Thermal Stability	11
3.1 Thermal Instability Causes	11
3.2 Thermal Stability Criteria in a Multi-Emitter Power HBT	15
3.3 Bipolar Power Transistor Design	20
3.4 Emitter Resistor Ballasting	22
4. Power Transistor Thermal Analysis Program	25
4.1 Program Platform	25
4.2 Mathematical Models	26
4.3 Program Interface	36
4.4 Program Flow	41
4.5 2 Bugs and 2 Fixes	44
4.6 Improving the Thermal Analysis Program	44
5. Thermal Analysis of a 5-Emitter Finger AlGaAs/GaAs Power HBT with a Si ²⁸ Substrate	48
5.1 Thermal Analysis Data	48
5.2 Transistor Design Parameters	52
5.3 Thermal Analysis Results	52
6. Conclusion	56
6.1 A Better Power Transistor	56
6.2 Suggested Further Study	57
Appendix 1 Thermal Conductivity of Isotopes	59
Appendix 2 Power Transistor Thermal Analysis Data	64
Bibliography	95

LIST OF FIGURES

Figure	page
<p>Figure 2.1 The thermal conductivities, κ, in W/cm-°K, of natural 3-isotope silicon and 99.8588% purified Si²⁸ isotope plotted against temperature in °K [Ruf et al. - 2001]. The solid lines (____), dashed lines (-----), and circled points (oooooo) are theoretically modeled curves. The other curves are actual experimental data. The Purified Si²⁸ thermal conductivity is about 60% greater than natural silicon at 300 °K and about 600% greater at cryogenic temperatures. The left graph is on log-log scale. The right graph is a magnified view on semi-log scale of the right end of the first graph to show the improvement of κ near room temperatures.</p>	7
<p>Figure 3.1 Positive electrothermal feedback loop in a <i>pn</i>-junction circuit. For a constant external-applied base-emitter voltage, V_{be}, the internal base-emitter junction voltage, V_{be-jn}, will decrease with increasing temperature, causing the junction current to increase to satisfy circuit boundary conditions limited by the clamped V_{be}. Without a balancing negative-feedback current, the thermal energy can increase exponentially and destroy the device [Adlerstein – 1998].</p>	12
<p>Figure 3.2 The base and collector current densities, J_b and J_c, of an HBT power transistor versus base-emitter voltage, V_{be}, measured at four different temperatures. [Liou and Bayraktaroglu – 1994]. This graph demonstrates the effect of positive temperature coefficient current feedback.</p>	13
<p>Figure 3.3 Measured common-emitter I-V characteristics at 25 °C for a typical HBT. The collector current collapse loci separate the normal and the collapse regions of operation. [Liu and Khatibzadeh – 1994].</p>	14
<p>Figure 3.4 A 5-emitter power HBT thermal profile. Each emitter finger adds heat to its neighboring finger, causing the middle finger to reach the highest temperature. The middle finger then draws the most current due to positive thermoelectric feedback [Walkey et al. – 2002].</p>	16
<p>Figure 3.5 Bipolar transistors with all bases tied, all emitters tied and all collectors tied to make one large high-power transistor. This technique boosts power-handling capability significantly. Emitter ballast resistors are added to improve thermal stability.</p>	21

Figure 3.6 Vertical cross section of a typical *npn* power bipolar junction transistor. The vertical structure increases power-handling capability by providing better thermal energy distribution. The thin emitter and base layers are where the current density is greatest. The thicker collector regions act as thermal sinks [Mohan et al. – 1989].

21

Figure 3.7 A multi-emitter *npn* power transistor cross section. The interleaved base and emitter fingers reduce emitter current crowding and emitter heating, thereby improving thermal stability [Mohan et al. -1989].

22

Figure 3.8 A transistor connected in the common-emitter amplifier configuration with intrinsic emitter resistance, r_e , and external emitter ballast resistance, R_E . The emitter ballast resistors provide negative feedback to the negative base-emitter junction voltage change, η , which is due to temperature rise at the junction from self-heating.

23

Figure 4.1 A typical power transistor cross section. Most of the heat is produced at the collector-base junction beneath the emitter finger mesas. The collector and substrate layers, which are much thicker than the emitter and base layers, essentially act as heat sinks [Liu et al. – 1993].

30

Figure 4.2 The emitter fingers are divided into arrays of heat source cells. If the power transistor die is much larger than the total surface area of all emitter fingers combined, then each finger can approximate a single heat source cell. This assumption reduces the number of calculations and time to converge to a solution significantly.

31

Figure 4.3 The Newton-Raphson method converges on a solution to $f(x)$ by dropping tangent lines to the x -axis that are each successively closer to the point at which the curve crosses the x -axis (the solution).

33

Figure 4.4 A 5-emitter finger power transistor die layout. The *Dimensions* portion of the program input menus allows the user to change the die length, width and thickness, and the emitter finger lengths, widths and positions with respect to the lower-left corner of the die.

36

Figure 4.5 The program interface consists of drop-down menus for material, electrical and die dimension input, and output data in the form of data and an emitter finger temperature versus emitter finger position graph. An error window at the bottom of the graph indicates when program limits are reached.

37

Figure 4.6 Program Flow Chart

43

Figure 5.1 The 5-emitter finger AlGaAs/GaAs power transistor on Si²⁸ substrate proposed for analysis. The Excel/Visual Basic thermal analysis program can be easily modified to analyze other transistor types and geometries by changing drop-down menu values. It can also be expanded to analyze power transistors with more than five emitter fingers.

48

Figure 5.2 The junction temperature of the middle emitter finger is calculated for the three different substrate materials as the substrate thickness is varied. With the Si²⁸ substrate, the emitter temperature changes very little as the substrate thickness increases, indicating a superior thermal design.

54

Figure 5.3 The junction temperature of the middle emitter finger is calculated for the three substrate materials as the emitter ballast resistance is varied. The transistor with the GaAs substrate becomes unstable when the ballast resistance goes below 18 Ω . The transistor with the natural Si substrate becomes unstable when the ballast resistance goes below 3 Ω . The transistor with the Si²⁸ substrate, however, remains stable at 354 °K even when the ballast resistance is reduced to zero Ω .

55

Figure A1.1 Energy bandgap structures for Si, Ge, and GaAs [Sze - 1981] showing the narrowest point, Γ , in the bandgap, E_g . This point will be narrower by about 0.065% for G⁷⁴ isotope.

63

Figure A2.1 5-emitter finger AlGaAs/GaAs power transistor thermal profile from Liu and Bayraktaroglu research paper in Solid-State Electronics – 1993. Oddly, they did not use the Kirchoff transformation to adjust their data for the temperature dependence of the substrate thermal conductivity.

65

Figure A2.2 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at 40 mA, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

67

Figure A2.3 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at **30 mA**, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

68

Figure A2.4 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at **20 mA**, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

69

Figure A2.5 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at **10 mA**, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

70

Figure A2.6 Validation data from the 1994 Bayraktaroglu and Liu research paper with 5 μ m spacing between each finger and total emitter current at 50 mA. The finger spacing was adjusted by them to demonstrate the effect on the thermal stability. Clearly, the thermal properties become worse as emitter fingers are positioned closer together as the heating affects by neighboring fingers is increased.

71

Figure A2.7 Reproduction of the data form the 1994 Bayraktaroglu and Liu research paper with 5 μ m spacing between each finger using the thesis thermal analysis tool. The total emitter current was 50 mA. Correlation is within 2.7% of their data.

72

Figure A2.8 Thermal analysis data and emitter dimensions from the 2001 research paper by Lee, Oh, and Kang. The total device DC input power was held at 260 mW. The emitter finger spacings were widened around the middle finger to demonstrate a method for improving thermal stability.

73

Figure A2.9 Reproduction of the thermal data in the 2001 research paper by Lee, Oh, and Kang using the thesis thermal analysis software. Correlation with their data is within 2.6%.

74

Figure A2.10 The GaAs substrate reference thermal run with substrate @ 100 μ m.

75

Figure A2.11 A natural silicon substrate thermal run with substrate @ 100 μ m. The transistor is running cooler, and the thermal profile is much more even than the profile with the GaAs substrate.

76

Figure A2.12 A Si²⁸ substrate thermal run with substrate @ 100μm. The thermal profile is clearly the coolest and flattest of the three substrate materials and solidly thermally stable.

77

Figure A2.13 A GaAs substrate thermal run with substrate @ 50μm. The thermal profile improves dramatically with a thinner substrate, and the power transistor is more solidly thermally stable.

78

Figure A2.14 A natural silicon substrate thermal run with substrate @ 50μm. The thermal profile improves significantly. The emitter finger are all sharing approximately the same current, and temperatures are all well below the thermal instability level.

79

Figure A2.15 A Si²⁸ substrate thermal run with substrate @ 50μm. The thermal profile is almost flat, and the power transistor is thermally very stable. All emitter fingers share approximately the same current.

80

Figure A2.16 A GaAs substrate thermal run with substrate @ 10μm. The thermal profile improves dramatically again. Thinning the substrate has made the power transistor significantly more thermally stable.

81

Figure A2.17 A natural silicon substrate thermal run with substrate @ 10μm. The thermal profile is almost flat, and the power transistor is thermally stable. Emitter finger current sharing is almost optimum.

82

Figure A2.18 A Si²⁸ substrate thermal run with substrate @ 10μm. The thermal profile is nearly flat, and the central emitter finger collector current is now lower than the end finger currents. The thermal stability is close to optimum.

83

Figure A2.19 GaAs substrate thermal run with R_e @ 19Ω. The power transistor remains thermally stable, but is operating over 150 °K hotter from lowering the ballast resistance just 1Ω. Emitter finger current sharing is poor. The center emitter finger conducts approximately 40% of the available current.

84

Figure A2.20 GaAs substrate thermal run with R_e @ 18Ω. The power transistor operating temperature has moved into thermal instability after lowering the emitter resistance only 2Ω. The center emitter finger now conducts 67% of the available

current. At over 900 °K it is above the semiconductor intrinsic temperature and transistor action has theoretically ceased.

85

Figure A2.21 A natural silicon substrate thermal run with R_e @ 18Ω. The power transistor remains thermally stable.

86

Figure A2.22 A Si^{28} substrate thermal run with R_e @ 18Ω. The power transistor is more thermally stable than the natural silicon substrate thermal run.

87

Figure A2.23 A natural silicon substrate thermal run with R_e @ 10Ω. The power transistor remains thermally stable after cutting the ballast resistance in half.

88

Figure A2.24 A Si^{28} substrate thermal run with R_e @ 10Ω. The thermal profile remains nearly flat, and power transistor remains solidly thermally stable.

89

Figure A2.25 A natural silicon substrate thermal run with R_e @ 3.0Ω. The power transistor remains thermally stable after dropping the ballast resistance values by 85%.

90

Figure A2.26 A natural silicon substrate thermal run with R_e @ 2.9Ω. The power transistor moves into thermal instability at this ballast resistance value.

91

Figure A2.27 A Si^{28} substrate thermal run with R_e @ 2.9Ω. The power transistor remains thermally stable. The thermal run with the natural silicon substrate has gone unstable at this point.

92

Figure A2.28 A Si^{28} substrate thermal run with R_e @ 1Ω. The power transistor remains thermally stable.

93

Figure A2.29 A Si^{28} substrate thermal run with R_e @ 0.0Ω. The power transistor remains thermally stable with no ballast resistance. The lack of any ballast resistance, however, will affect transistor operation adversely at RF frequencies.

94

LIST OF VARIABLES

<u>Variable</u>	<u>Units</u>
β_{DC} = DC gain	--
$\beta(T)$ = temperature- <i>dependent</i> DC gain	--
β_0 = pre-exponential DC gain factor	--
γ = emitter injection efficiency ratio	--
$\gamma_{mn} = \sqrt{\lambda_m^2 + \mu_n^2}$ eigen value factor	--
ϑ^{Si} = Debye temperature for silicon	$^{\circ}K$
ϑ^{Ge} = Debye temperature for germanium	$^{\circ}K$
κ = thermal conductivity	W/cm- $^{\circ}K$
$\kappa^{Si}(T_{max})$ = maximum temperature- <i>dependent</i> κ for Si	W/cm- $^{\circ}K$
$\kappa^{Ge}(T_{max})$ = maximum temperature- <i>dependent</i> κ for Ge	W/cm- $^{\circ}K$
κ_0 = κ at the ambient temperature	W/cm- $^{\circ}K$
$\kappa(T_0)$ = temperature- <i>dependent</i> thermal conductivity	W/cm- $^{\circ}K$
κ_{th} = temperature- <i>independent</i> thermal conductivity	W/cm- $^{\circ}K$
$\lambda_m = m \frac{\pi}{L}$ eigen value	--
λ = phonon wavelength	cm
μ_n = electron mobility	cm/s
μ_p = hole mobility	cm/s
$\mu = e\langle\tau\rangle/m^*$ = charge mobility equation	cm/s

<u>Variable</u>	<u>Units</u>
η = change in base-emitter turn-on voltage with change in temperature	$\Delta V_{be-jn}/^{\circ}\text{K}$
$\rho = 1/\sigma = 1/e(n\mu_n + p\mu_p)$	Ω/cm
θ = temperature assuming temperature- <i>independent</i> κ_{th}	$^{\circ}\text{K}$
$\sigma = e(n\mu_n + p\mu_p)$	mho/cm
$\langle \tau \rangle$ = scattering rate	seconds
τ_{ac} = acoustic or lattice or phonon scattering (phonon-electron interaction)	seconds
τ_{ion} = ionized impurity or Coulomb scattering	seconds
$\tau_{neutral}$ = neutral impurity scattering	seconds
$\tau_{Normal}^{-1} = AvT^3\lambda^{-1}$	per seconds
$\tau_{Umklapp}^{-1} = BvT\lambda^{-1}e^{(-C/T)}$	per seconds
$\tau_{Boundary}^{-1} = v/D$	per seconds
$\tau_{Isotope}^{-1} = 4\pi^3 v T^3 \lambda^{-4} V_o x(1-x)(12-x)^{-2}$	per seconds
v = average phonon velocity	(cm/s)
a = empirical fitting parameter (4350 for Si, 533 Ge and 450 for GaAs)	--
A = cross sectional area of the <i>pn</i> -junction	cm^2
b = empirical fitting parameter (1.40 for Si, 1.19 for Ge and 1.22 for GaAs)	--
BV_{ceo} = back collector-emitter open voltage	volts
C = specific heat	calorie
D_E, D_B = emitter and base diffusion coefficients	cm/s
$D_n(T)$ = temperature- <i>dependent</i> diffusion coefficient	cm/s
e = charge of an electron = 1.6×10^{-19} amps/second	coulombs

<u>Variable</u>	<u>Units</u>
ΔE_a = activation energy ΔE_a	electron-volts
Note: ΔE_a is defined differently for abrupt-junction and graded- junction transistors.	
In abrupt-junction transistors it is the emitter-junction valence-band offset, as defined in the drift-diffusion emission model. For a graded-junction transistor it is the emitter-base bandgap difference.	
$F_{mj} = \sin(\lambda_m) \cdot \left(X_j + \frac{1}{2} \right) - \sin(\lambda_m) \cdot \left(X_j - \frac{1}{2} \right)$	eigen factor --
$G_{nj} = \sin(\mu_n) \cdot \left(Y_j + \frac{w}{2} \right) - \sin(u_n) \cdot \left(Y_j - \frac{w}{2} \right)$	eigen factor --
I_{cj} = the collector current flowing through the j^{th} heating element (emitter finger) as mA defined in Eq. 4.2.2 on page 26	
I_{ck} = the collector current flowing through each heating element (emitter finger)	mA
I_{co} = collector reverse saturation current	mA
$I_S = q \cdot A \cdot D_n(T) \cdot \frac{n_i(T)^2}{W_B \cdot N_A}$	= transistor reverse saturation current 10^{-18}A
I_{critical} = current level at which transistor moves into instability	mA
k = Boltzmann's constant	electron-volts
L = length of the die	cm
L_p = phonon mean free path	cm
l = length of each emitter finger	cm
$n_i(T)$ = temperature- <i>dependent</i> intrinsic charge carrier concentration	$\#/\text{cm}^3$
N_B, N_E = base and emitter doping levels	$\#/\text{cm}^3$
N_A = acceptor doping concentration	$\#/\text{cm}^3$

<u>Variable</u>	<u>Units</u>
p = number of holes per cubic centimeter	$\#/cm^3$
Q = thermal energy	Watt
R_{th} = temperature- <i>dependent</i> thermal resistance of each emitter finger	Ω
R_e = emitter finger ballast resistance + intrinsic resistance	Ω
R_{ek} = the <i>total</i> resistance of each emitter finger	Ω
t = thickness of the die	cm
T = temperature of emitter finger center	$^{\circ}K$
T_C = corrected temperature adjusted for temperature- <i>dependent</i> thermal conductivity	$^{\circ}K$
T_A = absolute temperature	$^{\circ}K$
T_k = the temperature at the center of each emitter finger as defined in Eq. 4.2.1	$^{\circ}K$
T_0 = temperature of ambient environment	$^{\circ}K$
$T_{jn}(I_c)$ = collector current- <i>dependent</i> junction temperature	$^{\circ}K$
V_{be} = the base-emitter external bias voltage	volts
$\Delta V_{be}/T$ = The change in base-emitter voltage with change in temperature	$\Delta V_{be-jn}/^{\circ}K$
Note: $\Delta V_{be}/T$ – The change in base-emitter voltage with change in temperature (η in Eq. 4.2.2 above) is an empirically derived factor, dependent on the bandgap energy, E_g , the apparent conduction band discontinuity, ΔE_c , and the ambient temperature, T_0 .	
V_{ce} = collector-emitter bias voltage	volts
V_0 = atomic volume	cm^3
W_B, W_E = base and emitter widths	cm
W = width of the die	cm

<u>Variable</u>	<u>Units</u>
w = width of each emitter finger	cm
x = material thickness	cm
x = the ratio of the charge carrier kinetic energy to the thermal energy, kT	--
x_{Si28} = isotope fraction	--
X_k = the center coordinate of each emitter finger in the x-direction	cm
Y_k = the center coordinate of each emitter finger in the y-direction	cm

CHAPTER 1

Introduction

Thermal stability has remained the primary limitation on the power-handling capability of bipolar power transistors since the early 1950s. The power density of a bipolar power transistor device is typically boosted by paralleling a set of discrete transistors with common collectors, common bases, and common emitters. The power limitation depends on the ability of the transistor materials to dissipate and evenly distribute the thermal energy across the transistor array. Exceeding the specified thermal limits of a bipolar power transistor can cause thermal instability in the form of secondary breakdown (“thermal runaway”), or in the case of heterojunction bipolar power transistors (HBTs), in the form of collector current collapse. Improving the thermal conductivity of the semiconductor substrate on which the power transistor is built has historically proven to be one of the best ways to lower the individual transistor junction temperatures and evenly distribute the thermal energy [Marty et al. – 1993]. Better heat dissipation also will reduce charge leakage, reduce device noise, and slow down metal electromigration, thereby improving operating performance and device reliability. Substrate thermal conduction can best be improved by thinning the substrate and by choosing substrate materials with superior thermal conductivity.

The isotopes of all semiconductors exhibit higher thermal conductivities than their naturally occurring mixed-isotope semiconductor counterparts. Pure Ge⁷⁰ isotope has 20% higher thermal conductivity at room temperature than natural germanium, and pure

Si^{28} isotope has 60% higher thermal conductivity at room temperature than natural silicon [Burden - 2002]. The two semiconductor manufacturers, Intel^[TM] and AMD^[TM], have recently developed CMOS microprocessors on pure Si^{28} isotope substrates to exploit this property [Magee - 2002]. Prototypes from both companies are presently being tested (third quarter of 2002). Power transistor devices can also benefit from the new semiconductor isotope technology. Thermal stability can be improved, and the inherent reliability can be extended. A power transistor built on a semiconductor isotope substrate will have significantly higher power-handling capability than a classically constructed power transistor.

In this thesis, a new high-speed bipolar power transistor design, comprised of five parallel AlGaAs/GaAs HBTs built on a Si^{28} substrate, is proposed for analysis. The classical design technique of adding emitter finger ballast resistors to each transistor in the array for thermo-electric feedback is used in the design to augment even distribution of the thermal energy generated during circuit operation. A new thermal-analysis software program was developed for this thesis to analyze the thermal profile of the new power transistor, based on a power transistor thermal model developed by Dr. Guang-Bo Gao at Beijing Polytechnic University and Dr. Hadis Morkoc at the University of Illinois in 1989.

The following chapter begins with an overview of the physics of thermal conductivity in semiconductor isotopes. Current mathematical models and research data for semiconductor isotope thermal conductivity are discussed, and the newly emerging isotope industry is described. Basic power transistor design concepts are explained,

emphasizing how emitter ballast resistors are used to generate electrothermal feedback to improve thermal stability. The design, operation, and underlying mathematical models of the thermal-analysis software program are described in the next chapter. This description is followed with the results of the analysis of the new AlGaAs/GaAs power HBT, thesis conclusions, and suggestions for further work. The analysis reveals a power transistor with significant improvement in thermal stability and a substantial increase in power handling capability. The thermal-analysis program also proves to be an effective tool for selecting minimized values of the emitter ballast resistors.

CHAPTER 2

Semiconductor Isotopes

2.1 Isotopes Defined

Isotopes are atoms of the same element with differing atomic weights. The atomic number, or number of protons in the nucleus, remains the same for all isotopes of an element. But, the mass number, or number of protons plus neutrons, differs. The number of neutrons in the nucleus can vary naturally or be varied artificially, yielding a single element with several different atomic weights. More than 80% of the natural elements, including all of the elemental semiconductors, are composed of mixes of stable isotopes. Isotopes such as silicon and germanium are designated in the research literature as Si^x and Ge^x , where the “x” superscript is the mass number of the element. Silicon occurs in nature as a mix of three isotopes: 92.23% Si^{28} , 4.67% Si^{29} , and 3.10% Si^{30} . Germanium occurs naturally as a mix of five isotopes: 36.5% Ge^{74} , 27.4% Ge^{72} , 20.5% Ge^{70} , 7.8% Ge^{73} , and 7.8% Ge^{76} [Lide - 2002].

Scientists are motivated to study different isotopes of elements because the fundamental physical properties of the elements will vary as the isotope mix is varied. Some of the differences are very subtle and some are quite dramatic. From a pure research point of view, they are all interesting. From the point of view of a semiconductor device engineer, several of these property enhancements merit exploitation. By varying the isotope mix of the elemental semiconductors, a device engineer can affect the charge mobilities, device noise immunity, energy bandgap, rates

of impurity diffusion, and thermal expansion coefficient of the semiconductor crystal lattice [Haller – 1999]. The lattice constant of a crystal of a single isotope is slightly smaller than the lattice constant of the naturally occurring mixed-isotope element, and the size of the lattice constant directly affects the width and shape of the energy bandgap. This is a critical parameter in all semiconductor device designs. Phonon and electron scattering effects will vary with isotope mix proportions. Because electron scattering directly affects charge transport in the crystal lattice, the electrical resistance will be affected. Phonon scattering is directly related in a very complex way to the thermal conductivity of a material. The prospect of improving the thermal conductivity, κ , of a device material system is probably the most intriguing aspect of isotope purification for the device engineer [Haller - 1995]. An overview of some of these isotope properties is briefly explained in Appendix 1.

2.2 Si²⁸ and Ge⁷⁰ Thermal Conductivity

The superior thermal conductivity, κ , of semiconductor isotopes has been a subject of close study by solid state physicists since the 1920s. Research originally focused on Ge⁷⁰ because it was much easier to purify, and it was easier to technically measure the thermal conductivity of Ge than that of other materials of interest. The Ge⁷⁰ isotope has been found to have about 1.2 times the thermal conductivity of natural Ge at 300 °K [Capinski et al. - 1997, Morelli et al. - 2002]. A 99.9% pure Si²⁸ isotope, however, has a maximum thermal conductivity 6 times higher than natural Si at cryogenic temperatures and 1.6 times higher at room temperature (300 °K) [Ruf et al.- 2000, Morelli et al. -

2002]. This effect was first correctly predicted in 1941 by the Russian physicist Ivan Pomeranchuk. He observed that thermal conductivity in natural five-isotope Ge did not increase exponentially with decreasing temperature, as modeled by the generally accepted thermal conductivity theory of the German physicist R. E. Peierls, which was developed in 1929. Pomeranchuk explained that even in highly purified crystals of Ge, disturbances in the periodicity of the crystal lattice will occur because of the differences in isotope sizes. These disturbances will create phonon scattering and produce thermal resistance. His predictions were first tested and verified by researchers T. H. Gebelle and G. W. Hull in 1958 at Bell Labs [Gebelle and Hull - 1958]. They, in turn, predicted that their measurements on Ge could be extrapolated to Si. They claimed that the thermal conductivity of Si should be directly proportional to the thermal conductivity of Ge, as scaled by the ratio of the respective Debye temperatures, ϑ^{Si} and ϑ^{Ge} which is 1.75.

$$\vartheta^{\text{Si}}/\vartheta^{\text{Ge}} = 1.75 \quad \text{Eq. 1.1}$$

The Debye temperature is an important intrinsic material characteristic that marks a mathematical boundary between classical and quantum physics effects in crystal lattices. Above the Debye temperature, the classical Maxwell-Boltzmann statistics can be used to model physical behavior. Below the Debye temperature, more complex quantum statistics are required. The American physicist P. G. Klemens used the Debye temperature ratio of Si and Ge to predict the maximum thermal conductivity of Si²⁸, which is approximately three times the maximum thermal conductivity of Ge⁷⁴.

$$\kappa^{\text{Si}}(T_{\text{max}})/\kappa^{\text{Ge}}(T_{\text{max}}) \simeq 3.0 \quad \text{Eq. 1.2}$$

This theory was verified experimentally by a research team led by Thomas Ruf at the Max Planck Institute in 2000, and again by D. T. Morelli, J. P. Heremans, and G.A. Slack at Delphi Research Labs in 2002. Actual test data from the research of the Dr. Thomas Ruf research team at Max Planck Institute appears in Figure 2.1.

Figure 2.1 The thermal conductivities, κ , in W/cm-°K, of natural 3-isotope silicon and 99.8588% purified Si^{28} isotope plotted against temperature in °K [Ruf et al. - 2001]. The solid lines (—), dashed lines (-----), and circled points (oooooo) are theoretically modeled curves. The other curves are actual experimental data. The Purified Si^{28} thermal conductivity is about 60% greater than natural silicon at 300 °K and about 600% greater at cryogenic temperatures. The left graph is on log-log scale. The right graph is a magnified view on semi-log scale of the right end of the first graph to show the improvement of κ near room temperatures.

The physical theory of why and how isotopes affect thermal conductivity is complex, and not yet completely understood by physicists today. A complete explanation of the current theory is beyond the scope of this thesis. However, a brief overview is provided in Appendix 1. The experimental data for the thermal conductivity of single-isotope Si came decades behind theory because successful techniques for isolating Si^{28} in substantial quantities were not developed until the last decade. The experimental and theoretical curves in Figure 2.1 clearly show the superior thermal conductivity of single isotope Si^{28} over natural Si across a wide temperature range. The Si^{28} isotope would undoubtedly be very beneficial in enhancing the thermal properties of semiconductor devices that operate at cryogenic temperatures, such as charge-coupled devices, as well as devices that normally operate near room temperature.

2.3 The Isotope Industry

For over half a century scientists have known techniques for isolating various isotopes, but only in relatively small quantities that were adequate only for research. Within the last few years, however, a new industry has evolved that focuses on isolating and purifying different isotopes for use in the manufacture of a variety of consumer products, such as fluorescent lights, lasers, scientific instruments, and, most notably, semiconductor devices. Si^{28} and Ge^{76} are now available on the open market in sufficient quantities, and at competitive prices, warranting their use in the mass production of electronic components [Burden - 2002]. The new isotope engineering industry is an outcome of the Russian and Ukrainian nuclear industries. The Electrochemical Plant

Isotope Separation Facility in Zelenegorsk, Russia has successfully used gas centrifuge, chemical exchange, and laser separation techniques to mass-produce large quantities of raw isotopes. They are now able to support a growing world market for isotopes. One of the largest customer sectors for them is the semiconductor materials companies, such as Isonics Corporation, an American start-up based in Golden, Colorado. Isonics Corporation converts the raw isotopes they buy from the Electrochemical Plant Isotope Separation Facility into Si^{28} trichlorosilane gas, Si^{28} polysilicon, and Si^{28} epitaxial bulk wafers, all of which are base materials used by semiconductor device manufacturers, such as Intel and AMD [Magee - 2002].

The cost and availability of quantities of Si^{28} isotope which are substantial enough for a large semiconductor chip manufacturing run, have improved over the past decade to the point where incorporation into most existing semiconductor device designs is now viable. Isonics Corporation offers 4-inch, 5-inch, 6-inch, and 8-inch Si^{28} bulk wafers of 99.9% purity, and natural silicon wafers with Si^{28} epitaxial layers up to 12 microns thick, with 25-micron epitaxial layers planned in the near future. Lead times are typically only 4 to 6 weeks. They also offer these wafers pre-doped with options of boron, phosphorus, arsenic, or antimony in concentrations of $1 \times 10^{13}/\text{cm}^3$ to $1 \times 10^{19}/\text{cm}^3$. Isonics Corporation produces Si^{28} trichlorosilane gas for chip foundries that want to make their own Si^{28} wafers. Costs presently are still relatively high at \$2 to \$25 over the cost of a natural bulk wafer, and \$.10 to \$1 higher for epitaxial wafers, depending on the wafer size, doping option, and quantity. However, these costs will inevitably be forced down by economies of scale in the future. When the device- performance improvements are

dollar-costed, along with dollar savings in thermal engineering technology, then the true cost of Si²⁸ isotope devices can be assessed [Burden - 2002].

CHAPTER 3

Bipolar Power Transistor Thermal Stability

3.1 Thermal Instability Causes

The power-handling capability of a bipolar power transistor is limited primarily by the operating thermal profile. Power-handling capability is defined as the maximum thermally stable power density [Gao et al. – 1989]. Junction temperatures in a power transistor connected as an amplifier can rise to the point that a transistor no longer amplifies, and often leads to the destruction of the device. High junction temperatures create additional thermally generated charge carriers that can drive a doped semiconductor material past the intrinsic temperature, about 550 °K, where majority and minority carriers become equal, and transistor current gain drops to unity [Yang – 1988]. In other words, transistor action ceases. Or, the junction temperature can reach the classical thermal runaway limit, characterized by a precipitous drop in collector-emitter voltage, V_{ce} , accompanied by an exponential surge in collector current, I_c . Both of these phenomenon are the result of positive electrothermal feedback, caused by the positive temperature coefficient of the emitter current. As illustrated in Figure 3.1, if the current in a positive electrothermal feedback loop circuit is increased by ΔI , the circuit temperature will increase by δT according to dT/dI . This temperature increase, in turn, will increase the current further by δI , according to $(dI/dT)_{V_{be}}$, assuming the base-emitter voltage, V_{be} , is clamped at a constant voltage. These incremental temperature increases occur at the transistor *pn* junctions, and can destroy a transistor if negative electrothermal

feedback is not added to the circuit to counter-balance the effect of the positive electrothermal feedback.

Figure 3.1 Positive electrothermal feedback loop in a *pn*-junction circuit. For a constant external-applied base-emitter voltage, V_{be} , the internal base-emitter junction voltage, V_{be-jn} , will decrease with increasing temperature, causing the junction current to increase to satisfy circuit boundary conditions limited by the clamped V_{be} . Without a balancing negative-feedback current, the thermal energy can increase exponentially and destroy the device [Adlerstein – 1998].

Figure 3.2 The base and collector current densities, J_b and J_c , of an HBT power transistor versus base-emitter voltage, V_{be} , measured at four different temperatures. [Liou and Bayraktaroglu – 1994]. This graph demonstrates the effect of positive temperature coefficient current feedback.

Figure 3.2 displays the V_{be} versus base and collector current densities, J_b and J_c , at several different static temperatures for a typical HBT, illustrating the positive temperature coefficient. The V_{be} required to maintain the current at a given value decreases as the temperature increases.

A regular planar Si power transistor also has a current gain, β_{DC} , that increases with temperature, which can lead to thermal runaway. Energy bandgap engineering in a single-emitter HBT, however, produces a transistor with a β_{DC} that will *decrease* with temperature. This property weakens the thermoelectric feedback effect produced by the positive emitter current temperature coefficient so much that *thermal instability does not occur*. However, power transistors are typically designed with multi-emitters to boost

power-handling capability. In a multi-emitter finger power HBT, a thermal instability phenomenon known as “current gain collapse” (or “collector current collapse” or “current crush”) can occur. The onset of the

Figure 3.3 Measured common-emitter I-V characteristics at 25 °C for a typical HBT. The collector current collapse loci separate the normal and the collapse regions of operation. [Liu and Khatibzadeh – 1994].

phenomena happens before the thermal runaway limit is reached. In the current gain collapse region of the HBT Gummel plot in Figure 3.3, the collector current abruptly collapses, at which point the transistor is useless for amplification. The phenomenon occurs in both common-base-connected and common-collector-connected HBT power amplifiers, and an HBT device can be biased in and out of the collapse region [Liu et al. – 1993]. The research of Dr. G. Gao and Dr. H. Morkoc lead them to the conclusion that the collector current collapse phenomenon can best be deterred by improving the thermal conductivity of the semiconductor substrate on which the power HBT is built

[Gao et al. – 1989]. A silicon isotope such as Si^{28} could improve the thermal conductivity of a AlGaAs/GaAs HBT substrate significantly.

3.2 Thermal Stability Criteria in a Multi-Emitter Power HBT

The cause of current gain collapse in an HBT is the uneven temperature distribution across the power transistor emitter-finger junctions. The emitter fingers in the center of the die will experience higher junction temperatures due to thermal coupling than the other fingers (see Figure 3.4). Because of the associated higher positive electrothermal feedback, this finger will draw more of the available current than the other fingers and consequently become even hotter. If the thermal dissipation is not balanced among the emitter fingers with ballast resistors, the middle finger can become hot enough to draw all of the available current and dissipate most of the thermal energy. When this happens, the overall β_{DC} of the power device plummets, and power amplification ceases.

Figure 3.4 A 5-emitter power HBT thermal profile. Each emitter finger adds heat to its neighboring finger, causing the middle finger to reach the highest temperature. The middle finger then draws the most current due to positive thermoelectric feedback [Walkey et al. – 2002].

The critical collector current level, I_{critical} , at which collector current collapse will occur has been calculated by Dr. William Liu and Dr. Ali Khatibzadeh in 1994 [Liu and Khatibzadeh – 1994].

$$I_{\text{critical}} = N \cdot \left(K \cdot \frac{T_A}{q} \right) \cdot \left(\frac{1}{R_{\text{th}} \cdot \eta \cdot V_{\text{ce}} - R_e} \right) \quad \text{Eq. 3.1}$$

Where:

N = number of emitter fingers

K = Boltzmann's constant (eV/°K)

T_A = ambient temperature (°K)

q = electron charge (Coulombs)

R_{th} = temperature-dependent thermal resistance of each emitter finger (°K/W)

R_e = emitter finger ballast resistance + intrinsic resistance (Ω)

η = change in base-emitter turn-on voltage with change in temperature ($\Delta V_{\text{be-jn}}/\text{°K}$)

V_{ce} = collector-emitter voltage (V)

Above I_{critical} , most of the current will be conducted through the middle emitter finger.

Below this threshold, the current (and thermal energy) will be approximately evenly distributed across the emitter fingers.

The primary cause of the uneven temperature distribution that leads to thermal instability in a multi-emitter finger power HBT is the thermal dependence of the current

gain, β_{DC} , of each transistor in the array. The β_{DC} depends primarily on the emitter injection efficiency, γ , defined as the fraction of the minority electrons injected from the emitter into the base.

$$\gamma = \frac{I_{nE}}{(I_{nE} + I_{pE})} \quad \text{Eq. 3.1}$$

$$\beta_{DC} = \frac{\gamma}{\gamma - 1} \quad \text{Eq. 3.2}$$

The emitter efficiency, γ , is highly dependent on the collector-base junction temperature, which is highly dependent on the collector current, I_c . More explicitly, γ (and therefore β_{DC}) depend on the energy bandgap structure, junction geometry, doping levels, and junction temperatures. A more detailed mathematical definition of emitter-injection efficiency is given in Eq. 3.3. Here it is apparent that the emitter-injection efficiency decreases as junction temperature increases, leading to a β_{DC} that decreases with temperature.

$$\gamma(T_{jn}(I_c)) = \frac{1}{\left[1 + \left(\frac{D_E}{D_B} \right) \cdot \left(\frac{N_B}{N_E} \right) \cdot \left(\frac{W_B}{W_E} \right) \cdot \exp \left[- \left(\frac{\Delta E_a}{kT_{jn}(I_c)} \right) \right] \right]} \quad \text{Eq. 3.3}$$

Where:

D_E, D_B = emitter and base diffusion coefficients

N_B, N_E = base and emitter doping levels

W_B, W_E = base and emitter widths (μm)

ΔE_a = an activation energy

$T_{jn}(I_c)$ = collector current-dependent junction temperature ($^{\circ}\text{K}$)

k = Boltzmann's constant

Note that the activation energy, ΔE_a , is defined differently for abrupt-junction and graded-junction transistors. In abrupt-junction transistors, ΔE_a is also known as the emitter-junction valence-band offset, as defined in the drift-diffusion emission model.

For a graded-junction transistor ΔE_a is the emitter-base bandgap difference.

Negative electrothermal feedback in a multi-emitter power transistor design is usually provided by adding emitter ballast resistance to the emitter fingers. The resistances act to evenly distribute the thermal energy across the emitter fingers. This technique, however, also degrades transistor performance because it requires additional electrical energy and dissipates additional thermal energy. A better technique to counter the positive electrothermal feedback is to improve thermal dissipation of the transistor through the semiconductor substrate, which acts primarily as a support structure and a thermal heat sink for the device. Silicon is commonly used as a substrate in AlGaAs/GaAs power transistor design because silicon has a thermal conductivity 3 times the thermal conductivity of GaAs. An isotope of silicon, such as Si^{28} , however, has a thermal conductivity 6 times the thermal conductivity of GaAs, and would clearly be a better substitute.

3.3 Bipolar Power Transistor Design

A typical bipolar power transistor is designed with multiple transistors (all bases tied together, all emitters tied together, and all collectors tied together) to boost the power as illustrated in Figure 3.5. An AlGaAs/GaAs power HBT composed of 120 transistors connected in this way was reported to generate over 12 watts as an integrated part of a single monolithic transceiver IC [Liu and Bayraktaroglu - 1993]. Power transistors are most often designed as vertical structures (as in Figure 3.6) to maximize the cross-sectional area available for current flow and to minimize the thermal resistance of the device. Another technique used to improve thermal dissipation is to increase the surface area of the total collective emitter by increasing the number of emitters. The emitter finger surfaces are the primary source of device heat. The individual emitter finger dimensions are kept long and narrow, and the fingers are interleaved with the base fingers (as shown in Figure 3.7) to relieve the emitter current crowding, which is due to lateral voltage differentials between emitter and base elements. Current crowding degrades the

Figure 3.5 Bipolar transistors with all bases tied, all emitters tied and all collectors tied to make one large high-power transistor. This technique boosts power-handling capability significantly. Emitter ballast resistors are added to improve thermal stability.

Figure 3.6 Vertical cross section of a typical *npn* power bipolar junction transistor. The vertical structure increases power-handling capability by providing better thermal energy distribution. The thin emitter and base layers are where the current density is greatest. The thicker collector regions act as thermal sinks [Mohan et al. – 1989].

thermal-stability threshold. The collector regions are typically much thicker than the emitter or base regions. Because emitter and collector currents are approximately equal, the current density in the emitter layer is much higher than the collector current density. Therefore, the emitter fingers are essentially heat sources, and the collector layer and device substrate act as heat sinks.

Figure 3.7 A multi-emitter *n**p**n* power transistor cross section. The interleaved base and emitter fingers reduce emitter current crowding and emitter heating, thereby improving thermal stability [Mohan et al. -1989].

3.4 Emitter Resistor Ballasting

A classic technique used in the design of bipolar power transistors to lower junction temperatures and evenly distribute the thermal energy is to add external ballasting resistors to the emitter fingers, and sometimes to the base inputs. The addition of ballast

resistance weakens the positive electrothermal feedback from the temperature-dependent β_{DC} by providing a negative electrothermal feedback loop in the base-emitter circuit. Ballast resistances however, also reduce overall device current gains and degrade transistor performance. The ideal power transistor would have zero emitter resistance. By designing a power transistor on a Si²⁸ substrate, emitter resistances can theoretically become totally unnecessary (see Chapter 5). But, some small emitter resistance is always designed in, notwithstanding the thermal instability problem, to maintain quality RF properties in the power device [Adlerstein – 1998]. Consequently, it is

Figure 3.8 A transistor connected in the common-emitter amplifier configuration with intrinsic emitter resistance, r_e , and external emitter ballast resistance, R_E . The emitter ballast resistors provide negative feedback to the negative base-emitter junction voltage change, η , which is due to temperature rise at the junction from self-heating.

very important in power transistor design to minimize the values of the emitter-ballast resistances as much as possible. Several power transistor researchers [Arnold – 1967, Winkler – 1967, Gao et al. – 1989, Adlerstein – 1998, Liao and Lee – 2002] have

developed precise models useful for selection of minimum emitter-ballast resistances.

Other researchers have taken a modeling plus trial and error approach, as was done in this thesis, by modeling thermal profiles of multi-emitter power transistors with various emitter resistances to determine the threshold of thermal instability [Gao et al. – 1989, Liu and Bayraktaroglu – 1993, Liou and Bayraktaroglu – 1994, Kim et al. – 1998].

CHAPTER 4

Power Transistor Thermal Analysis Program

4.1 Program Platform

The thermal analysis program developed for this thesis was adapted to a commercial Microsoft Excel 97 ^[TM] spreadsheet software package. The program is based on the theoretical power transistor thermal modeling research of Guang-Bo Gao at the Beijing Polytechnic University and Hadis Morkoc at the University of Illinois in 1989. They developed the nonlinear thermal feedback model on an IBM 4381 main frame computer to research thermal design considerations of high-power heterojunction bipolar power transistors (HBTs), including the effect of substrate material selection on the power-handling capability. The Excel program is backward and forward compatible with older versions of Excel, and is easily convertible to other spreadsheet languages, such as dBase IV ^[TM] or Quattro Pro ^[TM]. In developing the program, extensive use was made of Excel's built-in Visual Basic ^[TM] programming language interpreter and programmer's tool kit, which has a large array of preprogrammed function and routine modules for ease of program construction. The universal availability of Excel spreadsheet software, and the compact size ($\approx 1.0\text{Mb}$) of the thermal analysis program developed for this thesis, make this new tool easily portable to any PC. The application program file is small enough to attach to an email and transmit over the Internet. All of the program development and subsequent thermal analysis of the multi-emitter power HBT was done on a 700 MHz Pentium III laptop computer.

The program was customized specifically for the thermal analysis of 5-emitter finger bipolar power transistors, homojunction or heterojunction, comprised of any semiconductor material. However, the program can be easily modified to solve other transistor thermal problems because of the simple modular structure. By modifying the underlying model equations in the spreadsheet cells, other transistor designs can be analyzed, and emitter finger counts higher or lower than five can be setup. The time it takes for the program to converge on a solution is proportional to the number of calculations performed in each thermal run, which is proportional to the cube of the emitter finger count:

$$\text{Speed of analysis} \propto \text{number of calculations} \propto (\text{number of emitter fingers})^3$$

Therefore, addition of emitter finger modules to increase the finger count slows the calculation speed proportionately. The program, as configured to collect the thermal analysis data for the transistor analysis in this thesis, performs approximately 3.5 million calculations per thermal analysis run and takes about 11 minutes and 15 seconds to converge to a solution.

4.2 Mathematical Models

The mathematical engine in the thermal analysis program is based on the theoretical model detailed in a 1989 research paper collaboration, “Thermal Design Studies of High-Power Hetrojunction Bipolar Transistors,” by Dr. Guang-Bo Gao from Beijing

Polytechnic University and Dr. Hadis Morkoc from the University of Illinois in 1989. Their model is based primarily on two other research papers: the thermal analysis in the seminal research paper, “Steady-State Junction Temperatures of Semiconductor Chips,” by Dr. Robert Lindsted and Dr. Rohinton Surty from IBM Components Division in 1972, which solves the classical Laplace heat equations for a semiconductor die (Eq. 4.2.1), and the drift-diffusion emission model from “GaAlAs-GaAs Ballistic Heterojunction Bipolar Transistor” by Dr. D. Ankri and Dr. L. F. Eastman in 1982, which models the performance of an abrupt emitter-junction *npn* GaAlAs/GaAs HBT. The Gao/Morkoc model is a coupling of a set of self-consistent simultaneous solutions to the heat-flow equations of Lindsted and Surty and a set of solutions to the drift-diffusion emission current density equations of Ankri and Eastman.

$$\begin{aligned}
T_k = & \left(\frac{2}{L \cdot W \cdot l} \right) \cdot \left(\frac{V_{ce}}{K_{th}} \right) \cdot \sum_{j=1}^N \left[\sum_{m=1}^{\infty} \left(\frac{\tanh(\lambda_m \cdot t)}{\lambda_m^2} \right) \cdot F_{mj} \cos(\lambda_m \cdot X_k) \right] \cdot I_{cj} \\
& + \\
& \left(\frac{2}{L \cdot W \cdot w} \right) \cdot \left(\frac{V_{ce}}{K_{th}} \right) \cdot \sum_{j=1}^N \left[\sum_{n=1}^{\infty} \left(\frac{\tanh(\mu_n \cdot t)}{\mu_n^2} \right) \cdot G_{nj} \cos(\mu_n \cdot Y_k) \right] \cdot I_{ck} \\
& + \\
& \left(\frac{4}{L \cdot W \cdot l \cdot w} \right) \cdot \left(\frac{V_{ce}}{K_{th}} \right) \cdot \sum_{j=1}^N \left[\sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \left(\frac{\tanh(\gamma_{mn} \cdot t)}{\lambda_m \cdot \mu_n \cdot \gamma_{mn}} \right) \cdot F_{mj} \cdot G_{nj} \cos(\lambda_m \cdot X_k) \cdot \cos(\mu_n \cdot Y_k) \right] \cdot I_{cj} \\
& + \\
& \left(\frac{t}{L \cdot W} \right) \cdot \left(\frac{V_{ce}}{K_{th}} \right) \cdot \sum_{j=1}^N I_{cj} + T_A
\end{aligned} \tag{Eq. 4.2.1}$$

Where:

L = transistor die length (μm)

W = transistor die width (μm)

t = transistor die thickness (μm)

l = emitter finger lengths (μm)

w = emitter finger widths (μm)

X_k = the center coordinate of each emitter finger in the x-direction (μm)

Y_k = the center coordinate of each emitter finger in the y-direction (μm)

V_{ce} = collector-emitter bias voltage (V)

I_{cj} = the collector current flowing through the j^{th} heating element (emitter finger) as defined in Eq. 4.2.2 (A)

κ_{th} = **temperature-independent** thermal conductivity of the die substrate material (W/cm-°K)

$$\lambda_m = m \cdot \frac{\pi}{L} \quad (\text{eigenvalue})$$

$$\mu_n = n \cdot \frac{\pi}{W} \quad (\text{eigenvalue})$$

$$\gamma_{mn} = \sqrt{\lambda_m^2 + \mu_n^2} \quad (\text{eigenvalue})$$

$$F_{mj} = \sin(\lambda_m) \cdot \left(X_j + \frac{l}{2} \right) - \sin(\lambda_m) \cdot \left(X_j - \frac{l}{2} \right) \quad (\text{factor})$$

$$G_{nj} = \sin(\mu_n) \cdot \left(Y_j + \frac{w}{2} \right) - \sin(\mu_n) \cdot \left(Y_j - \frac{w}{2} \right) \quad (\text{factor})$$

The emitter current equations developed by R. P. Arnold and D. S. Zoroglu (Eq. 4.2.2) in their research paper, “A Quantitative Study of Emitter Ballasting,” published in IEEE Transaction on Electronic Devices in 1974, is usually used in place of the Anki/Eastman drift-diffusion emission model in power transistor modeling research papers because it is a conceptually simpler model, and explicitly relates the thermal stability of a power transistor to the emitter ballast resistors. The current flowing through each emitter finger (the heating elements) is strongly influenced by the emitter-ballasting resistors, added for electrothermal feedback, as described in Chapter 3.

$$I_{ck} = I_{co} \cdot \exp \left[\left(\frac{q}{k \cdot T_A} \right) \cdot [V_{bejnk} - \eta \cdot (T_k - T_A)] \right] \quad \text{Eq. 4.2.2}$$

Where:

$$V_{bejnk} = V_{be} - R_{ek} \cdot I_{ck} \quad (\text{V})$$

I_{ck} = the collector current flowing through each heating element (emitter finger) (A)

I_{co} = collector reverse saturation current (A)

V_{be} = the base-emitter external bias voltage (V)

R_{ek} = the **total** resistance of each emitter finger (Ω)

q = electron charge in Coulombs (C)

k = Boltzmann's constant in electron-volts (eV)

$\eta = \Delta V_{be} / ^\circ\text{K}$, the change in base-emitter with change in substrate temperature ($^\circ\text{K}$)

T_k = the temperature at the center of each emitter finger as defined in Eq. 4.2.1 ($^\circ\text{K}$)

T_A = the ambient temperature at the base of the substrate material ($^{\circ}\text{K}$)

Dr. Gao and Dr. Morkoc viewed the individual transistors in the transistor array mathematically as transistors that could be divided further into smaller subtransistor arrays with common bases, common emitters, and common collectors (see Figure 4.2). Because the highest current density occurs at the emitter-base junctions, the emitters of each transistor in a subtransistor array are the primary sources of heat during transistor operation. Professors Gao and Morkoc referred to them as heat cells. The collectors and die substrate consequently diffuse the heat generated by each emitter heat cell. All other surfaces are considered adiabatic.

Figure 4.1 A typical power transistor cross section. Most of the heat is produced at the collector-base junction beneath the emitter finger mesas. The collector and substrate layers, which are much thicker than the emitter and base layers, essentially act as heat sinks [Liu et al. – 1993].

Thus, by calculating the temperature in each cell, a collective map of these elemental temperatures becomes the thermal profile over the entire power transistor die. However, other power transistor researchers [Liu and Bayraktaroglu – 1993, Liu and Khatibzadeh – 1994, Kim et al. – 2001, Liao et al. – 2002] that have used the Gao/Morkoc thermal profile model simplified their calculations by not dividing each emitter finger into heat cells, and instead considered each entire emitter finger to be a heat source. This simplifying assumption is valid when the sum of the emitter finger surface areas is considerably smaller than the total die surface area. The number of calculations required to generate the thermal profile is thereby reduced significantly, and the iterative thermal calculation converges to a solution faster.

Figure 4.2 The emitter fingers are divided into arrays of heat source cells. If the power transistor die is much larger than the total surface area of all emitter fingers combined, then each finger can approximate a single heat source cell. This assumption reduces the number of calculations and time to converge to a solution significantly.

The total number of solutions of each set of equations (denoted by k -subscript in Eqs. 4.2.1 and 4.2.2) required to generate the thermal profile is equal to the number of emitter fingers (heat source cells) in the transistor design. For a 5-emitter finger AlGaAs/GaAs power HBT, there will be 5 equations for temperature, T_k , and 5 equations for collector currents, I_{ck} , or a total of 10 coupled nonlinear homogeneous partial differential equations that are solved simultaneously. This key concept allowed a simpler and more portable approach to developing the thermal analysis program on an Excel spreadsheet with Visual Basic routines.

Newton- Raphson Method

Solving 10 nonlinear homogeneous partial differential equations simultaneously, however, can be a daunting task, even for a professional mathematician. In the words of W. Press, B. Flannery, S. Teukolsky, and W. Vetterling in Numerical Recipes – The Art of Scientific Computing [Cambridge University Press – 1986], “We make an extreme, but wholly defensible, statement: There are *no* good, general methods for solving systems of more than one nonlinear equation. Furthermore, it is not hard to see why (very likely) there *never will be* any good general methods.” The nonlinear solution method selected in most of the power transistor research papers that utilized the Gao/Morkoc model for thermal simulation is the classic Newton-Raphson method. Successive approximations to the solutions of functions are calculated in this method by extending tangent lines to the curves of the functions down to the x-axis repeatedly, each time moving the tangent line down the curve, shortening the resulting error and

Figure 4.3 The Newton-Raphson method converges on a solution to $f(x)$ by dropping tangent lines to the x -axis that are each successively closer to the point at which the curve crosses the x -axis (the solution).

converging on the point at which the function crosses the x -axis, which are the solutions to the equations (see Figure 4.3). This method works best for smooth, well-behaved functions, and both Eq. 4.2.1 and 4.2.2 are relatively smooth and well-behaved. The designers of the Excel spreadsheet have conveniently added a software routine for the Newton-Raphson method to their calculation toolkit. Consequently, programming Excel to solve power transistor thermal-analysis problems primarily consisted of the effort to generate Eqs. 4.2.1 and 4.2.2 in Excel spreadsheet cells by writing Visual Basic software routines. The solutions to these simultaneous nonlinear equations could then automatically be generated with the iterative calculation feature built in to the Excel programming language.

Kirchoff Transformation

The substrate thermal conductivity variable, K_{th} , in Eq. 4.2.1 is assumed to be temperature-***independent*** to simplify the calculations. Thermal conductivity, however, is ***very*** temperature-***dependent***, as is evidenced by the thermal conductivity-versus-temperature curves of the Si²⁸ isotope in Figure 2.1. To compensate for this heavy thermal-conductivity temperature dependence in the transistor thermal profile calculations, power transistor researchers [Liou et al. – 1993, Marty et al. – 1993, Kim et al. – 1998, Lee et al. – 2001, Liao and Lee – 2002] used the Kirchoff Transformation (Eq. 4.2.3), which was suggested originally by a research paper on heat sinks by W. B. Joyce in 1975 at Bell Labs [Joyce – 1975]. Dr. Joyce employed the Kirchoff transformation to develop temperature transformation equations that convert constant thermal conductivity temperatures, T_{κ_0} , to temperature-***dependant*** thermal conductivity temperatures, $T_{\kappa(T)}$.

$$\theta = T_0 + \left(\frac{1}{\kappa_0} \right) \cdot \int_{T_0}^T \kappa(T) dT \quad \text{Eq. 4.2.3}$$

Kirchoff Transformation

Where:

T = corrected temperature adjusted for temperature-***dependent*** thermal conductivity (°K)

θ = uncorrected temperature with temperature-***independent*** thermal conductivity (°K)

T_0 = temperature of ambient environment (°K)

κ_0 = thermal conductivity at the ambient temperature (°K/W)

$\kappa(T)$ = temperature-***dependent*** thermal conductivity (°K/W)

The temperature-*dependent* equations of thermal conductivity are experimentally derived from curves. Empirical fitting parameters for each thermal conductivity curve distinguish the materials. The temperature-dependent thermal conductivity, $\kappa(T)$, for Si, Ge, and GaAs can be expressed as [Kokkas – 1974].

$$\kappa(T_0) = aT^{-b} \quad \text{Eq. 4.2.4}$$

Where:

T_0 = ambient temperature ($^{\circ}\text{K}$)

a = empirical fitting parameter (4350 for Si, 533 for Ge and 450 for GaAs)

b = empirical fitting parameter (1.40 for Si, 1.19 for Ge, and 1.22 for GaAs)

Applying the Kirchoff transformation to equation 4.2.4 yields the simple conversion equation [Liou and Bayraktaroglu – 1994].

$$T = \left[\left(\frac{1}{T_0^{b-1}} \right) - \left[(b-1) \cdot \frac{(\theta - T_0)}{T_0^b} \right] \right]^{\left[\frac{-1}{(b-1)} \right]} \quad \text{Eq. 4.2.5}$$

Where:

T = corrected temperature adjusted for temperature-*dependent* thermal conductivity ($^{\circ}\text{K}$)

θ = uncorrected temperature, with temperature-*independent* thermal conductivity ($^{\circ}\text{K}$)

T_0 = temperature of ambient environment ($^{\circ}\text{K}$)

b = empirical fitting parameter (1.40 for Si, 1.19 for Ge, and 1.22 for GaAs)

Adjusting the temperature profiles generated by Eq. 4.2.1 for temperature-dependant thermal conductivity is a simple matter of filtering the solution points through Eq. 4.2.5 with the properly selected empirical material thermal conductivity-fitting parameter.

4.3 Program Interface

The program interface is customized to analyze a 5-finger AlGaAs/GaAs power HBT configured as shown in Figure 4.4. However, the interface is easily modifiable to accommodate other transistor types and emitter finger counts higher or lower than five. The program inputs are selected from pull-down menus (**Value** column in the center of Figure 4.5). Program inputs consist of the transistor die dimensions, the positions on the die of each emitter finger, the material and circuit biasing parameters, and the material thermal parameters.

Figure 4.4 A 5-emitter finger power transistor die layout. The *Dimensions* portion of the program input menus allows the user to change the die length, width and thickness, and the emitter finger lengths, widths and positions with respect to the lower-left corner of the die.

Figure 4.5 The program interface consists of drop-down menus for material, electrical and die dimension input, and output data in the form of data and an emitter finger temperature versus emitter finger position graph. An error window at the bottom of the graph indicates when program limits are reached.

These inputs are selectable as follows:

Die Configuration

Die Length - Selectable from 0 to 500 μm

Die Width - Selectable from 0 to 500 μm

Die Thickness - Selectable from 0 to 500 μm

Emitter Width - Selectable from 0 to 10 μm

Emitter Length - Selectable from 0 to 100 μm

Emitter Positions

$X_{I \Rightarrow 5}$ - The center coordinate of each emitter finger in the x-direction

$Y_{I \Rightarrow 5}$ - The center coordinate of all five emitter fingers in the y-direction

Electrical Variables

Emitter-Collector voltage, V_{ce} - External common-emitter amplifier biasing in (volts)

Base-Emitter voltage, V_{be} - External common-emitter amplifier biasing (volts)

Total base current, I_{bT} - Total external input DC current bias applied to all 5 common power transistor bases (milliamps)

Collector reverse saturation current, I_o – Although the saturation current, in 10^{-20} amps, is treated as a constant to simplify calculations, it is in reality temperature sensitive. The collector reverse saturation current (or scaling current) is proportional to the cross-sectional area of the *pn*-junction and the electron and hole charge concentrations.

Pre-factor current gain @ 300 °K, β_o – The pre-exponential factor, β_o , [Liou and Bayraktaroglu – 1994] is a convenient lumped factor used to calculate the temperature-*dependent* DC current gain, $\beta(T)$, of the transistor, and is related to $\beta(T)$ with the following formula:

$$\beta(T) = \beta_o \cdot \exp\left(\frac{\Delta E_{va}}{kT}\right) \quad \text{Eq. 4.3.1}$$

Where:

$\beta(T)$ = temperature-adjusted DC gain of the transistor (unit-less ratio)

β_0 = pre-exponential factor (unit-less ratio)

ΔE_{va} = the emitter junction valence-band offset (eV)

k = Boltzmann's constant (eV/°K)

T = temperature of emitter finger center (°K)

Apparent Valence Band Discontinuity, $\Delta V_{be}/T$ or η – The change in base-emitter voltage with change in temperature parameter (renamed η in Eq. 4.2.2 for convenience) is an empirically derived factor, dependent on the bandgap energy, E_g , the apparent conduction band discontinuity, ΔE_c , and the ambient temperature, T_0 . The definition of the conduction band discontinuity is analogous to that of the apparent valence band discontinuity described here.

$$\eta = \frac{(E_g + \Delta E_c)}{T_0} \quad \text{Eq. 4.3.2}$$

Typically η values for all semiconductor materials range from minus 1.4 to minus 2.5 mV/°K. For GaAs, it is approximately minus 2.06 mV/°K [Liou and Bayraktaroglu – 1994].

Apparent Valence Band Discontinuity, ΔE_{va} – This parameter is an activation energy, ΔE_{va} , also known as the emitter junction valence-band offset, as defined in the

Ankri/Eastman drift-diffusion emission model [Ankri and Eastman – 1982]. ΔE_{va} is used to calculate the thermal-*dependent* DC gain, $\beta(T)$, as in Eq. 4.3.1. Typical values are 50 to 70 meV, which are highly dependent on the mole fraction of Al in the AlGaAs emitter layer. This is a characteristic of abrupt emitter-base junction transistors. For graded emitter-base junction transistors, the difference in bandgap energy, ΔE_a , is used [Kroemer – 1982].

Thermal Variables

Heat Sink Temperature, T_0 – Ambient temperature at the bottom of the substrate material ($^{\circ}\text{K}$)

Thermal Conductivity @ T_0 , K_{th} – Substrate material thermal conductivity at the ambient heat sink temperature ($\text{W}/\text{cm}\text{-}^{\circ}\text{K}$)

Thermal Conductivity Fitting Parameter, b – An empirical parameter for determining emitter finger temperature adjusted for temperature-dependent thermal conductivity, as calculated with the Kirchoff transformation (see Eq. 4.2.5)

Program outputs consist of the tabulated final emitter finger temperatures and emitter currents and a graph of the emitter finger temperatures versus the position of the emitter finger on the die. Temperature outputs are given in two versions: a version adjusted with the Kirchoff transformation method (see Mathematical Models in section 4.2), which compensates for the temperature dependence of thermal conductivity, and an unadjusted

version. The unadjusted data is used to validate the thermal program data with the unadjusted data from several research papers.

To run the program, simply select the desired inputs from the pull-down menus, and then bring up the *[Calc Sheet]* button from the *<Tools>* menu at the top of the Excel window as follows:

<Tools> => <Options> => <Calculation> => [Calc Sheet]

In the *<Calculation>* menu are three selectable options: **I**terations, **M**aximum **i**terations, and **M**aximum **c**hange. These are the controls that setup the Excel spreadsheet for the Newton-Raphson method of solutions. Clicking the *[Calc Sheet]* button starts the analysis. The data in Chapter 5 of this thesis was collected with **Maximum iterations** set to 1000 and **Maximum change** set to .0001. With these settings, each thermal run took about 11 minutes and 15 seconds to converge to the solution.

4.4 Program Flow

The program starts with an initial guess at the collector currents of 1 mA for each emitter finger. Because the collector currents are approximately equal to the emitter finger currents, they are used to calculate the emitter finger temperatures with the solutions to the Laplace heat flow equations (Eq. 4.2.1). The finger temperatures are then used to recalculate the thermal-dependant base-emitter voltage for each finger using

a variation of Eq. 4.2.2. New collector currents are then generated by adding 0.00001 mA to the current per loop. During each loop the thermal-dependent emitter-base voltage, V_{bei} (see Figure 4.6), is recalculated and compared to the external V_{be} bias selected from the input menus until they are equal. V_{bei} is the transistor's internal base-emitter junction voltage, denoted as variable V_{bejnk} in Eq. 4.2.2. Next the temperature-dependent $\beta(T)_i$ for each finger is calculated and used with the input parameter total base current, I_{bT} , and total emitter current, $\sum I_{ci}/\beta(T)_i$, to calculate the iteration error. This error is compared to an arbitrary convergence limit, 0.0001.

$$I_{bT} - \sum I_{ci}/\beta(T)_i < 0.0001? \quad \text{Eq. 4.4.1}$$

When the program converges, the emitter finger versus temperature graph is generated automatically by the built-in Excel graphing routine. Figure 4.6 illustrates the program flow.

Power Transistor Thermal Analysis Program

Figure 4.6 Program Flow Chart

4.5 Two Bugs and Two Fixes

The program contains two known problems that may result in erroneous temperatures. Fortunately, both problems have simple workarounds. When the program converges to the solution for a temperature profile of a thermally-unstable transistor, that is when all emitter current is being conducted through the middle emitter finger, the program produces correct temperature values as the transistor is stepped deeper into the instability solution by increasing input parameter values. But, stepping incrementally back down from a thermally unstable transistor mode into a stable mode may leave the transistor hung in instability beyond the true threshold. To reset the program simply rerun the model with a very low base current (< 0.1 mA). This will force the transistor out of instability. The program also will exhibit a metastable condition under certain transistor parameter input conditions. The program may begin to oscillate between two calculation iterations and fail to converge. To pull the program out of this metastable state, press the **<Esc>** key. This will bring up the Visual Basic debugger. Select the **<Debug>** button, and exit the debugger by collapsing it. A program caution window will display “This will close the editor. Do you want to do this?” Select the **<Yes>** button, and exit and reopen the Excel spreadsheet to restart a new thermal run.

4.6 Improving the Thermal Analysis Program

Accuracy

The solutions to the thermal equations are in the form of an infinite Fourier series. Because calculating an infinite number of terms will take infinity, the loops that calculate

the terms must be limited in number. For the thermal runs in Chapter 5, the loops were limited to 1000-loop iterations each. The accuracy of the thermal analysis can thus be improved by simply increasing the number of iterations. This will, of course, slow the speed of the program. Another way to improve accuracy would be to refine the transistor models used in the program. All of the transistor equations used are physical models, and therefore approximations based on the assumptions of the researchers that derived the models. For example, instead of assuming a static reverse saturation current, I_0 , selected from a pull-down menu, a saturation current model could easily be programmed into a spreadsheet cell that depends on temperature-dependent diffusion coefficients and the temperature-dependent intrinsic charge carrier quantity as in Eq. 4.4.1.

$$I_S = q \cdot A \cdot D_n(T) \cdot \frac{n_i(T)^2}{W_B \cdot N_A} \quad \text{Eq. 4.4.1}$$

Where:

q = electron charge (Coulombs)

A = cross-sectional area of the pn-junction (μm^2)

$D_n(T)$ = temperature-*dependent* diffusion coefficient (cm/s)

$n_i(T)$ = temperature-*dependent* intrinsic charge carrier concentration ($\#/\text{cm}^3$)

W_B = width of the base layer (μm)

N_A = acceptor doping concentration ($\#/\text{cm}^3$)

Speed

The program can be sped up considerably by removing the data points between the emitter fingers. The data points of primary interest in the thermal analysis of a multi-emitter power transistor are the peak temperatures in the center of each emitter finger. Removing the superfluous data points will decrease the number of calculations performed in each thermal run by approximately 50%, and ostensibly speed up the program by 50%. The resulting output graph, however, will be less representative of the actual physical thermal profile. Also, changing graphics from color to black and white will use fewer computer system resources. Another way to accelerate convergence to a solution is to compile the Visual Basic code in the program. The Excel programming package contains this option. Compiling will speed up the software routines. However, once compiled, the program cannot be modified. Another option is to simply run the program on a faster computer. The thermal run outputs displayed in Appendix 2 were all made on a 700 MHz Pentium III with 256 Mb of working memory. The thermal profiles generated for this thesis each took approximately 10 to 15 minutes to converge to a solution.

Size

The entire thermal program comprises a file of approximately 1.0 Mb. This size of file is small enough to attach to an email and successfully transmit through most Internet services. But, the size of the program can be decreased significantly, if needed, by

removing the superfluous graphic pictures of the die and transistor circuit. Also, the program will run just as well without the temperature versus emitter finger position graph and the data points between the fingers. Output is then tabular. Modifying the program to delete these features will shrink the program size considerably.

CHAPTER 5

Thermal Analysis of a 5-Emitter Finger AlGaAs/GaAs Power HBT on a Si²⁸

Substrate

5.1 Thermal Analysis Data

Two sets of thermal data were collected with the thesis thermal analysis software for a 5-emitter finger AlGaAs/GaAs HBT power HBT transistor designed on GaAs, natural Si and Si²⁸ substrates that effectively act as heat sinks (see Figure 5.1). One set compares thermal profiles as the thickness of each substrate type is thinned from 100 μm to 10 μm .

Figure 5.1 The 5-emitter finger AlGaAs/GaAs power transistor on Si²⁸ substrate proposed for analysis. The Excel/Visual Basic thermal analysis program can be easily modified to analyze other transistor types and geometries by changing drop-down menu values. It can also be expanded to analyze power transistors with more than five emitter fingers.

The other set compares the thermal profiles with each substrate material as the emitter ballast resistance values of the elemental transistors are varied from 20Ω down to zero. The theoretical data clearly demonstrates the superior thermal stability properties achievable when the power HBT is designed on a Si^{28} substrate, and also proves that the emitter ballast resistors can be virtually eliminated with a Si^{28} substrate design.

Validation data to verify proper operation of the thermal analysis software tool was obtained from two current industry research papers on AlGaAs/GaAs power HBT transistor design that utilized the model developed in 1989 by Dr. Guang-Bo Gao and Dr. Hadis Morkoc. The research paper, “Theoretical Calculations of Temperature and Current Profiles in Multi-Finger Heterojunction Bipolar Transistors,” written by Dr. William Liu and Dr. Burhan Bayraktaroglu at the Texas Instruments Central Research Laboratories in 1993, analyzes the thermal profile of a 5-emitter finger AlGaAs/GaAs power HBT, and the research paper, “Emitter Structure of Power Heterojunction Bipolar Transistor for Enhancement of Thermal Stability,” written by Dr. J. G. Lee, Dr. T. K. Oh, Dr. B. Kim, and Dr. B. K. Kang in 2001, analyzes the thermal stability of a 5-emitter finger AlGaAs/GaAs power HBT. The same transistor configurations and material parameters used in each of these papers were duplicated with the drop-down menus in the thesis thermal analysis software. The thermal data generated by the thesis thermal analysis tool duplicated the data in each of these research papers within 3% or better, verifying good correlation. The actual validation data and the transistor design parameters from the papers and the thesis thermal analysis runs are reprinted in Appendix 2. Tables I, II, and III provide summaries of the data validation results.

Table I
Bayraktaroglu and Liu Data versus Thesis Data
(Validation data to verify proper operation of the thermal analysis program)

Total emitter current	10 mA	20 mA	30 mA	40 mA
Finger #1 heat – Baraktaroglu & Liu	335 °K	345 °K	365 °K	380 °K
Finger #1 heat – Thesis	329 °K	356 °K	372 °K	374 °K
Finger #2 heat – Baraktaroglu & Liu	336 °K	370 °K	408 °K	450 °K
Finger #2 heat – Thesis	333 °K	366 °K	404 °K	442 °K
Finger #3 heat – Baraktaroglu & Liu	338 °K	380 °K	432 °K	491 °K
Finger #3 heat – Thesis	334 °K	370 °K	428 °K	496 °K
Finger #4 heat – Baraktaroglu & Liu	336 °K	370 °K	408 °K	450 °K
Finger #4 heat – Thesis	333 °K	366 °K	404 °K	442 °K
Finger #5 heat – Baraktaroglu & Liu	335 °K	345 °K	365 °K	380 °K
Finger #5 heat – Thesis	329 °K	356 °K	372 °K	374 °K

The validation data in Table I was generated by calculating the temperature in °K at the center of each emitter finger when the sum of the currents in all five emitter fingers were held at 10 mA, 20 mA, 30 mA, and 40 mA. Emitter finger #1 temperatures are equal to emitter finger #5 temperatures, and emitter finger #2 temperatures are equal to emitter finger #4 temperatures due to the symmetry of the device. Finger spacings were all at 15 μm apart as shown in Figure 5.1. The worst-case temperature calculations were within 2.6% of each other. Oddly, the emitter temperatures in the Bayraktaroglu/Liu research were not Kirchoff-adjusted for the temperature dependence of the thermal conductivity of GaAs. All of the other research papers on AlGaAs/GaAs HBT thermal design cited in

this thesis adjusted their data for the temperature dependence of thermal conductivity with the Kirchoff transformation (Eq. 4.2.5).

Table II
Bayraktaroglu and Liu Data versus Thesis Data
 (Validation data to verify proper operation of the thermal analysis program)

Total emitter current	50 mA
Finger #3 heat – Baraktaroglu&Liu	650 °K
Finger #3 heat – Thesis	666 °K

The validation data in Table II was generated by calculating the temperature at the center of emitter finger #3 with the sum of currents in all five emitters held at 50 mA and each finger spaced 50 μ m apart. The temperature calculations are within 2.4% of each other.

Table III
Lee, Oh and Kang Data versus Thesis Data
 (Validation data to verify proper operation of the thermal analysis program)

Total emitter current	260 mW
Finger #1 heat – Lee, Oh and Kang	362 °K
Finger #1 heat – Thesis	369 °K
Finger #2 heat – Lee, Oh and Kang	378 °K
Finger #2 heat – Thesis	376 °K
Finger #3 heat – Lee, Oh and Kang	364 °K
Finger #3 heat – Thesis	362 °K
Finger #4 heat – Lee, Oh and Kang	378 °K
Finger #4 heat – Thesis	376 °K
Finger #5 heat – Lee, Oh and Kang	362 °K
Finger #5 heat – Thesis	369 °K

The data in Table III was generated by calculating the temperature at the center of each emitter finger while holding the total DC power of the device at 260 mW. Fingers #2 and #4 were positioned 40 μm from the center #3 emitter. Fingers #1 and #5 were positioned 20 μm from emitters #2 and #4, respectively. See Figure A2.8 in Appendix 2. The worst-case temperature calculations are within 1.9% of each other.

5.2 Transistor Design Parameters

The design parameters used for the power HBT are the same design parameters used in the Liu and Bayraktaroglu research paper. Die and emitter finger dimensions are as shown in Figure 5.1. The transistor electrical and physical parameters are listed in Table IV in Appendix 2. Throughout all thermal analysis runs the die dimensions were held constant at 300 μm x 460 μm x 100 μm ; the emitter finger dimensions were held constant at 20 μm x 2 μm ; and the emitter finger spacings were held constant at 15 μm . The transistors were biased the same each time, holding the total emitter current at 40 mA. Subsequent thermal runs change the substrate material thermal conductivities to those of natural silicon and Si^{28} , and vary the substrate thickness. The runs are performed again with the substrates held at 100 μm thickness as the material conductivities and emitter ballast resistances are varied.

5.3 Thermal Analysis Results

The graphs in Figures 5.2 and 5.3 summarize the results of the thermal analysis of the various test configurations. The curves clearly show a significant improvement in

thermal stability with the Si^{28} substrate in every case. For the thermal runs with different substrate thickness, the Si^{28} substrate keeps the power transistor 130% to 170% cooler than the GaAs substrate. For the thermal runs with emitter ballast resistances varied, the power transistor with the GaAs substrate becomes thermally unstable with just a 2Ω reduction in emitter ballast resistance. The power transistor with the Si^{28} substrate remains thermally stable even when the ballast resistance is reduced to zero. The semiconductor intrinsic temperature is defined as the temperature at which the number of thermally-generated charge carriers exceeds the number of charge carriers supplied by the dopant. In GaAs this temperature is typically about 825 °K. Consequently, any emitter finger temperatures above 825 °K are essentially meaningless, because the transistor action has ceased. To assure a safe transistor reliability margin, radio circuits are usually designed with sufficient heat sinking to keep the junction temperatures of the transistors below 425 to 475 °K in any emitter finger.

Figure 5.2 The junction temperature of the middle emitter finger is calculated for the three different substrate materials as the substrate thickness is varied. With the Si^{28} substrate, the emitter temperature changes very little as the substrate thickness increases, indicating a superior thermal design.

Figure 5.3 The junction temperature of the middle emitter finger is calculated for the three substrate materials as the emitter ballast resistance is varied. The transistor with the GaAs substrate becomes unstable when the ballast resistance goes below 18 Ω . The transistor with the natural Si substrate becomes unstable when the ballast resistance goes below 3 Ω . The transistor with the Si²⁸ substrate, however, remains stable at 354 °K even when the ballast resistance is reduced to zero Ω .

CHAPTER 6

Conclusion

6.1 A Better Power Transistor

Building a power transistor on a Si^{28} isotope substrate can improve the thermal stability of a multi-emitter power transistor. The thermal modeling of a AlGaAs/GaAs power HBT presented in this thesis has demonstrated that by substituting the natural semiconductors in a transistor substrate with semiconductor isotopes, the thermal profile of the transistor can be smoothed and flattened. The threshold for the onset of thermal instability can be improved significantly. Emitter ballast resistors, typically added to power transistor emitter fingers to improve thermal stability, can decrease the device efficiency by dissipating additional power and can add cost to the manufacturing process. The thermal properties of a power transistor can be improved with Si^{28} substrates to the point where emitter ballast resistors are no longer necessary.

The cost of mono-isotope wafers and wafers with mono-isotope epilayers is relatively high today. At this point in time, a production version of a power transistor on a semiconductor isotope substrate may be impractical. As this technology eventually folds into the mainstream of the semiconductor industry, economies of scale will inevitably drive down the costs of semiconductor isotopes rapidly. Several microprocessor companies have already taken the first steps to make this happen.

The thermal analysis program developed for this thesis is useful for further studies of transistor thermal properties. The program is compact and is written on the universally

available Excel spreadsheet with the Visual Basic programming language. It is therefore easily transferable to any PC. The modular structure of the program makes it a flexible tool that can be easily modified for other transistor thermal-analysis problems. Further study on transistors with isotopes in their material systems can be achieved with this software.

6.2 Suggested Further Study

Many other transistor parameters and phenomena besides the thermal-stability threshold are temperature dependent. Thermal noise, device reliability, the Kirk effect, the Webster effect, collector/emitter crowding, β_{ac} , β_{dc} , collector current fall time, and power amplifier power efficiency are a few examples. But many others exist. Any of these physical variables may be positively affected by introducing semiconductor isotopes into the material system. A good tool for studying any of these temperature-dependent variables is the thermal analysis software developed for this thesis.

In further studies on power transistors built on Si²⁸ substrate, experimental work should be performed to substantiate the findings in this thesis. Experiments to further validate the thermal analysis program could be relatively cheap and simple. The temperature dependence of the base-emitter junction voltage, V_{be-jn} , of any bipolar transistor can be easily measured with two power supplies, two multimeters, and a thermal chamber. This is a common experiment. This data could be used to further validate and calibrate the thermal-analysis program. The design and manufacture of a bipolar power transistor with a Si²⁸ substrate could be accomplished with the facilities

available in the San Jose State University Microelectronics Lab. The blank isotope wafers for this experiment could probably be acquired from Isonics Corporation in Golden, Colorado.

APPENDIX 1

Thermal Conductivity of Isotopes

Thermal Conductivity Modeling

The thermal conductivity, K , is defined as the rate of movement of thermal energy in Watts (W) per unit thickness of the medium (cm) per unit area (cm^2) per unit of temperature change in Kelvin ($^\circ\text{K}$).

$$K = \frac{-1}{A} \cdot \frac{d}{dt} Q \cdot \frac{d}{dT} x \quad (\text{W/cm-}^\circ\text{K}) \quad \text{Eq. 2.8}$$

Where:

A = material area (cm^2)

x = material thickness (cm)

Q = thermal energy (W)

T = temperature ($^\circ\text{K}$)

Thermal energy in metals is primarily transported by electrons through electron-phonon collisions, and thermal energy in insulators is transported primarily by phonons through phonon-phonon collisions. The semiconductor transport mechanism lies somewhere in between the two. The thermal conductivity, K , for an insulator is commonly modeled as proportional to the phonon mean free path, which is the mean distance the phonon travels before it encounters a collision.

$$K = \frac{1}{3} C \cdot v \cdot L \quad \text{Eq. 2.9}$$

Where:

C = specific heat (calories)

v = phonon velocity (cm/s)

L = phonon mean free path (cm)

The 1/3 constant in this model is empirical and therefore somewhat arbitrary [Kittel - 1953, p245]. The phonon mean free path, L , is proportional to an average scattering relaxation time, $\langle \tau \rangle$, just as in the electrical conductivity theory. Also, as in the electrical conductivity, several different complex phonon scattering mechanisms interplay to produce $\langle \tau \rangle$ and the mean free path, L . The most prevalent mechanism is Normal or N-scattering, so-called because it conserves the crystal lattice momentum. It dominates the thermal conductivity property at cryogenic temperatures. But, by itself, it would lead to a thermal conductivity prediction of infinity at room temperature. N-scattering and three other independent scattering processes were incorporated into a thermal conductivity model by Joseph Callaway in 1958 [Callaway - 1959] that successfully modeled the thermal conductivity of germanium over temperature from 2 °K to 100 °K. The other three processes, boundary scattering, Umklapp (German for “flipping over”) scattering, and isotope scattering, are called U-scattering processes, and they do not preserve lattice momentum. They dominate thermal conductivity at higher temperatures [Haller - 1999].

$$\tau_{\text{Normal}}^{-1} = AvT^3\lambda^{-1} \quad \text{Eq. 2.10}$$

$$\tau_{\text{Umklapp}}^{-1} = BvT\lambda^{-1}e^{(-C/T)} \quad \text{Eq. 2.11}$$

$$\tau_{\text{Boundary}}^{-1} = v/D \quad \text{Eq. 2.12}$$

$$\tau_{\text{Isotope}}^{-1} = 4\pi^3vT^3\lambda^{-4}V_0x(1-x)(12-x)^{-2} \quad \text{Eq. 2.13}$$

Where:

v = average phonon velocity (cm/s)

λ = phonon wavelength (cm)

x = isotope fraction

V_0 = atomic volume (cm³)

T = absolute temperature (°K)

A, B, C, D = empirical fitting parameters

The models of these individual processes can be approximately linearly added to model the total effect. However, determining thermal conductivity over temperature from these relaxation times requires integrating the sum of them in the Maxwell-Boltzmann equation, as is done for electrical conductivity, which cannot be done analytically.

Approximations are required [Callaway - 1959], and discussions of this are beyond the scope of this thesis. Even this complex model, however, does not take into account all of the scattering mechanisms in nature that cause thermal conductivity. A complete model has not yet been developed to date. The accuracy of the Callaway model has been substantiated with recent experimental data for silicon, germanium, and diamond [Capinski - 1997] [Gebelle and Hull - 1958].

Energy Bandgaps

Energy bandgap engineering is the manipulation of the width and shape of the semiconductor energy bandgaps in the emitter, base, and collector regions of a bipolar transistor through control of semiconductor material combinations and region geometries. Through energy bandgap engineering, the electric fields present in the transistor base, emitter-base junction, and base-collector junction, in conjunction with the forces imparted to electron and hole charge carriers in the band gap, can be optimized to speed up a transistor device. The enhanced speed of Si/SiGe HBTs is achieved through energy bandgap engineering. For most HBTs a wide energy bandgap emitter is engineered and a narrow energy bandgap base is engineered to optimize speed [Yuan - 1999, p54].

Because the effect of isotope purification on semiconductor bandgaps is to narrow them, ostensibly, isotopes could be used to further narrow the base energy bandgap. Lattice constants in isotopes are shorter than lattice constants in their natural parent element. The shortening of the lattice constant seen in isotopes narrows the bandgap. Also, independently, electron-phonon coupling effects in isotopes act to narrow the bandgap [Haller - 1999]. The total effect, however, is relatively small and of little consequence to the semiconductor device designer. Several groups of physicists in the past decade have successfully modeled and measured the effect of isotope engineering on energy bandgaps. Electron energy versus quantum electron wave vector (or k -space) maps are used to display and analyze energy bandgap data (see Figure A1.1). The regions in k -space for which solutions to the wave equation exist are called Brillouin zones. The

energy extrema are labeled Γ , L, Δ , X, K, and W at the symmetry points, and with Miller indices at their positions in k-space.

Figure A1.1 Energy bandgap structures for Si, Ge, and GaAs [Sze - 1981] showing the narrowest point, Γ , in the bandgap, E_g . This point will be narrower by about 0.065% for G^{74} isotope.

The Γ -point is an energy minimum in the first Brillouin zone, looking down the [100] plane. The combined effect from isotope purification G^{74} crystals of lattice shortening and electron-phonon interaction at room temperature was reported to be $0.49 \pm 0.03 \text{ meV/amu}$ [Haller - 1995], which is only about a 0.065% change at the minimal indirect band gap Brillouin zone Γ -point in the lattice. Consequently, this effect is of little interest to the semiconductor device engineers, and will probably remain of interest only to scientists.

APPENDIX 2

Power Transistor Thermal Analysis Data

This appendix contains theoretical data from the thermal analysis of the experimental 5-emitter finger AlGaAs/GaAs power HBT generated by the Excel/Visual Basic thermal analysis software tool developed for this thesis. The first section displays a set of validation data used to verify proper operation of the thermal analysis software tool. This data was obtained from two current industry research papers on AlGaAs/GaAs power HBT transistor design that utilized the model developed in 1989 by Dr. Guang-Bo Gao and Dr. Hadis Morkoc. The same transistor configurations and material parameters used in each of these papers were duplicated with the drop-down menus in the thesis thermal analysis software. The thermal data generated by the thesis thermal analysis tool duplicated the data in each of these research papers within 3% or better, verifying good correlation. The second section displays two sets of thermal data collected with the thesis thermal analysis software for a 5-emitter finger AlGaAs/GaAs HBT power HBT transistor designed on GaAs, natural Si and Si²⁸ substrates. One set compares the thermal profiles as the thickness of each substrate type is thinned from 100 μm to 10 μm . The other set compares the thermal profiles with each substrate material as the emitter ballast resistance values of the elemental transistors are varied from 20 Ω down to zero. The theoretical data clearly demonstrates the superior thermal stability properties achievable when the power HBT is designed on a Si²⁸ substrate, and also proves that the emitter ballast resistors can be virtually eliminated with a Si²⁸ substrate design.

Figure A2.1 5-emitter finger AlGaAs/GaAs power transistor thermal profile from Liu and Bayraktaroglu research paper in Solid-State Electronics – 1993. Oddly, they did not

use the Kirchhoff transformation to adjust their data for the temperature dependence of the substrate thermal conductivity.

Table IV
Power Transistor Electrical, Material, and Dimensional Design Parameters

Variable Description	Symbol	Value	Value
Die Configuration			
Die Length	L_x (μm)	0.03	300
Die Width	W_y (μm)	0.046	460
Die Thickness	t (μm)	0.01	100
Emitter Width	w_y (μm)	0.0002	2
Emitter Length	l_x (μm)	0.002	20
Emitter Position			
Emitter 1 center x-coordinate	x_1 (μm)	0.02	200
Emitter 2 center x_1 -coordinate	x_2 (μm)	0.0215	215
Emitter 3 center x_1 -coordinate	x_3 (μm)	0.023	230
Emitter 4 center x_1 -coordinate	x_4 (μm)	0.0245	245
Emitter 5 center x_1 -coordinate	x_5 (μm)	0.026	260
Emitter 1=>5 center y_1 -coordinate	$y_{1 \rightarrow 5}$ (μm)	0.015	150
Electrical Variables			
Emitter-Collector Voltage	V_{ce} (V)	10	10
Base-Ground Voltage	V_{be} (V)	1	1
Total Base Current	I_{bT} (mA)	0.001	1
Collector Reverse Saturation Current	I_{c0} (mA)	4E-22	4E-22
Emitter Finger Resistance	R_e (Ω)	20.0	20.0
Pre-factor Current Gain @ 300°K	β_0	11.72	11.72
$\Delta V_{be}/T$	η (V/°K)	-2.06E-03	-2.06E-03
Apparent Valence-Band Discontinuity	ΔE_{va} (eV)	0.05	0.05
Emitter Finger 1 Current	I_{c1} (mA)	11.248	11.248
Emitter Finger 2 Current	I_{c2} (mA)	11.334	11.334
Emitter Finger 3 Current	I_{c3} (mA)	11.368	11.368
Emitter Finger 4 Current	I_{c4} (mA)	11.334	11.334
Emitter Finger 5 Current	I_{c5} (mA)	11.248	11.248
Thermal Variables			
Heat Sink Temperature	T_0 (°K)	300	300
Thermal Conductivity @ T_0	K_{th} (W/°K*cm)	0.56	0.56
Thermal Conductivity Fitting Parameter	b	1.22	1.22

This table displays the power transistor die dimensions, emitter dimensions and positions (in μm and cm), electrical variables, and thermal variables used in the thermal analysis runs. The emitter currents, I_{cx} , were allowed to vary as total base current, I_{bT} , collector-

emitter voltage, V_{ce} , and base-emitter voltage, V_{be} , were held constant. Material thermal conductivity, κ_{th} , and thermal conductivity fitting parameter, b , were changed each run to match GaAs, natural Si, and Si^{28} .

Figure A2.2 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at 40 mA, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

Figure A2.3 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at 30 mA, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

Figure A2.4 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at **20 mA**, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

Figure A2.5 Duplication of the validation data from the 1994 Bayraktaroglu and Liu research paper with total emitter current held at **10 mA**, generated with the thesis thermal analysis program. Correlation with their data is within 2.5%.

Figure A2.6 Validation data from the 1994 Bayraktaroglu and Liu research paper with 5μm spacing between each finger and total emitter current at 50 mA. The finger spacing was adjusted by them to demonstrate the effect on the thermal stability. Clearly, the thermal properties become worse as emitter fingers are positioned closer together as the heating affects by neighboring fingers is increased.

Figure A2.7 Reproduction of the data form the 1994 Bayraktaroglu and Liu research paper with 5μm spacing between each finger using the thesis thermal analysis tool. The total emitter current was 50 mA. Correlation is within 2.7% of their data.

Figure A2.8 Thermal analysis data and emitter dimensions from the 2001 research paper by Lee, Oh, and Kang. The total device DC input power was held at 260 mW. The emitter finger spacings were widened around the middle finger to demonstrate a method for improving thermal stability.

Figure A2.9 Reproduction of the thermal data in the 2001 research paper by Lee, Oh, and Kang using the thesis thermal analysis software. Correlation with their data is within 2.6%.

5.2 Thermal Runs versus Substrate Thickness

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
51	42	38	42	51
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.84	0.65	0.52	0.65	0.84
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
5.20	9.76	12.90	9.76	5.20

Figure A2.10 The GaAs substrate reference thermal run with substrate @ 100μm.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
58	56	56	56	58
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.80	0.79	0.79	0.79	0.80
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
11.35	11.42	11.44	11.42	11.35

Figure A2.11 A natural silicon substrate thermal run with substrate @ 100μm. The transistor is running cooler, and the thermal profile is much more even than the profile with the GaAs substrate.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.82	0.81	0.81	0.81	0.82
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.59	12.51	12.48	12.51	12.59

Figure A2.12 A Si^{28} substrate thermal run with substrate @ 100μm. The thermal profile is clearly the coolest and flattest of the three substrate materials and solidly thermally stable.

Figure A2.13 A GaAs substrate thermal run with substrate @ 50 μ m. The thermal profile improves dramatically with a thinner substrate, and the power transistor is more solidly thermally stable.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
59	57	57	57	59
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.81	0.79	0.79	0.79	0.81
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
11.57	11.60	11.61	11.60	11.57

Figure A2.14 A natural silicon substrate thermal run with substrate @ 50μm. The thermal profile improves significantly. The emitter finger are all sharing approximately the same current, and temperatures are all well below the thermal instability level.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-in}	V_{be2-in}	V_{be3-in}	V_{be4-in}	V_{be5-in}
0.82	0.81	0.81	0.81	0.82
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.59	12.51	12.48	12.51	12.59

Figure A2.15 A Si²⁸ substrate thermal run with substrate @ 50μm. The thermal profile is almost flat, and the power transistor is thermally very stable. All emitter fingers share approximately the same current.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
50	49	49	49	50
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.76	0.74	0.73	0.74	0.76
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
9.64	10.06	10.12	10.06	9.64

Figure A2.16 A GaAs substrate thermal run with substrate @ 10μm. The thermal profile improves dramatically again. Thinning the substrate has made the power transistor significantly more thermally stable.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
62	62	62	62	62
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.82	0.81	0.81	0.81	0.82
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.42	12.40	12.39	12.40	12.42

Figure A2.17 A natural silicon substrate thermal run with substrate @ 10μm. The thermal profile is almost flat, and the power transistor is thermally stable. Emitter finger current sharing is almost optimum.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
67	67	67	67	67
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.83	0.83	0.83	0.83	0.83
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
13.44	13.39	13.39	13.39	13.44

Figure A2.18 A Si²⁸ substrate thermal run with substrate @ 10μm. The thermal profile is nearly flat, and the central emitter finger collector current is now lower than the end finger currents. The thermal stability is close to optimum.

5.3 Thermal Runs versus Emitter Ballast Resistor Value

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
55	43	36	43	55
V_{be1-in}	V_{be2-in}	V_{be3-in}	V_{be4-in}	V_{be5-in}
0.91	0.68	0.41	0.68	0.91
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
3.59	9.13	15.96	9.13	3.59

Figure A2.19 GaAs substrate thermal run with R_e @ 19Ω . The power transistor remains thermally stable, but is operating over 150°K hotter from lowering the ballast resistance just 1Ω . Emitter finger current sharing is poor. The center emitter finger conducts approximately 40% of the available current.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	50	31	50	63
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.99	0.85	0.14	0.85	0.99
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
1.36	4.61	24.08	4.61	1.36

Figure A2.20 GaAs substrate thermal run with R_e @ 18Ω . The power transistor operating temperature has moved into thermal instability after lowering the emitter resistance only 2Ω . The center emitter finger now conducts 67% of the available current. At over 900°K it is above the semiconductor intrinsic temperature and transistor action has theoretically ceased.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
58	56	56	56	58
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.82	0.81	0.81	0.81	0.82
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
11.33	11.43	11.46	11.43	11.33

Figure A2.21 A natural silicon substrate thermal run with $R_e @ 18\Omega$. The power transistor remains thermally stable.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-in}	V_{be2-in}	V_{be3-in}	V_{be4-in}	V_{be5-in}
0.84	0.84	0.84	0.84	0.84
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.59	12.50	12.49	12.50	12.59

Figure A2.22 A Si^{28} substrate thermal run with $R_e @ 18\Omega$. The power transistor is more thermally stable than the natural silicon substrate thermal run.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
58	56	56	56	58
V_{be1-in}	V_{be2-in}	V_{be3-in}	V_{be4-in}	V_{be5-in}
0.92	0.90	0.90	0.90	0.92
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
11.16	11.50	11.62	11.50	11.16

Figure A2.23 A natural silicon substrate thermal run with $R_e @ 10\Omega$. The power transistor remains thermally stable after cutting the ballast resistance in half.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.95	0.94	0.94	0.94	0.95
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.56	12.52	12.51	12.52	12.56

Figure A2.24 A Si^{28} substrate thermal run with $R_e @ 10\Omega$. The thermal profile remains nearly flat, and power transistor remains solidly thermally stable.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
59	56	54	56	59
V_{be1-in}	V_{be2-in}	V_{be3-in}	V_{be4-in}	V_{be5-in}
1.01	0.98	0.96	0.98	1.01
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
9.93	11.59	13.69	11.59	9.93

Figure A2.25 A natural silicon substrate thermal run with $R_e @ 3.0\Omega$. The power transistor remains thermally stable after dropping the ballast resistance values by 85%.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
70	61	29	61	70
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
0.93	0.87	0.25	0.87	0.93
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
0.01	0.01	81.07	0.01	0.01

Figure A2.26 A natural silicon substrate thermal run with $R_e @ 2.9\Omega$. The power transistor moves into thermal instability at this ballast resistance value.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
1.04	1.03	1.03	1.03	1.04
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.52	12.54	12.55	12.54	12.52

Figure A2.27 A Si²⁸ substrate thermal run with Re @ 2.9Ω. The power transistor remains thermally stable. The thermal run with the natural silicon substrate has gone unstable at this point.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
1.06	1.05	1.05	1.05	1.06
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.50	12.55	12.57	12.55	12.50

Figure A2.28 A Si²⁸ substrate thermal run with Re @ 1Ω. The power transistor remains thermally stable.

$\beta(T)_1$	$\beta(T)_2$	$\beta(T)_3$	$\beta(T)_4$	$\beta(T)_5$
63	62	62	62	63
V_{be1-jn}	V_{be2-jn}	V_{be3-jn}	V_{be4-jn}	V_{be5-jn}
1.07	1.06	1.06	1.06	1.07
I_{c1}	I_{c2}	I_{c3}	I_{c4}	I_{c5}
12.49	12.55	12.58	12.55	12.49

Figure A2.29 A Si²⁸ substrate thermal run with $R_e @ 0.0\Omega$. The power transistor remains thermally stable with no ballast resistance. The lack of any ballast resistance, however, will affect transistor operation adversely at RF frequencies.

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