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Rafika Smati
San Jose State University

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**A MODEL OF EMISSION CHARACTERIZATION DURING THE
COURSE OF CHIP MANUFACTURING**

A Thesis

Presented to

The Faculty of the Department of Chemical Engineering

San Jose State University

In Partial Fulfillment

of the requirement for the Degree

Master of Science

By

Rafika Smati

December 2004

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APPROVED FOR THE DEPARTEMNET OF CHEMICAL ENGINEERING

Dr. Gregory L. Young

Dr. Stacy Gleixner

Dr. Sebastien Raoux, Applied Materials Corporation

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ABSTRACT

**EMISSION CHARACTERIZATION DURING THE COURSE OF
CHIP MANUFACTURING**

by Rafika Smati

The semiconductor industry is changing rapidly. Wafer size is increasing to 300 mm. Copper is replacing aluminum as interconnect metal. These new technologies may cause the increase of air emission. In proactive fashion, the semiconductor industry has set an environmental performance goal for its processes.

This thesis presents a model of consumption and emission for major modules: shallow trench isolation, gate, and two interconnect modules (standard and dual damascene). A model of chemical consumption and emissions is built, based upon the contribution of each module in chip process. Overall, 80 percent of the emission is from the CVD and 20 percent from the etch processes, also it is found that a higher clean gas used compared to process gas. A reduction of 90 percent PFC emissions has been demonstrated. A destruction of PFC introduces an increase in HAPs emission. Finally the change to Cu/ Low k dual damascene increases the VOC emission.

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Chapter 1

Introduction

1.1 Outline

The new emphasis on the development of green and environmentally friendly semiconductor processing presents unique challenges both in reducing gas consumption and in quantitative measurements of emissions. Semiconductor processes are changing rapidly as evidenced in the 1997 Edition of the National Technology roadmap for semiconductor. The rapid transition to 300mm wafer, copper replacement of aluminum and tungsten metallization, and new low and high k materials could result in an increase of consumption and emission of greenhouse and hazardous air pollutant (HAP) (Refer to Appendix C for Glossary) for etching and chamber cleaning processes.

To ensure that environmental issues do not negatively impact new technology transfer to manufacturing, this research focuses mainly on evaluating the gas emission and consumption during the course of chip manufacturing for 300mm tools and comparing the environmental performance of copper/lowk and aluminum/SiO₂ interconnect modules.

The first chapter introduces the source of gas emission from semiconductor tools, as well as the methodologies adopted by the semiconductor industry. The second chapter is a literature review related to the Perfluorocompounds (PFC) and hazardous air pollutant (HAPS) reduction strategies. Chapter 3 introduces the process flow for each module and discusses the purpose of this research. Chapter 4 discusses the theory of the two analytical

instruments used to characterize different processes, Fourier transform infrared (FTIR), and quadrupole mass spectroscopy (QMS). Chapter 5 describes the experimental methodology used to analyze the gas emissions. Chapter 6 discusses a comparison of copper and aluminum interconnects module, and a model of gas emission and consumption per wafer basis. Chapters 7 discuss the overall conclusions and future work.

1.2 Background

The rapid growth of the semiconductor industry has resulted in an increase of PFC emissions from semiconductor industry fabs worldwide that may have significant environmental impact. In response to this rapid expansion, the United States Environmental Protection Agency (EPA) and the semiconductor industry have instituted a program to measure and reduce global warming emissions from the fabs. The program is especially important for the transition to 300-mm generations of tools since an ambitious reduction target has been specified by the industrial protocol I300I. In addition to PFCs, gas emission from the semiconductor industry also includes HAPs and VOCs.

The PFCs are considered high global warming gases (GWG) with high global warming potential (GWP). They are many times more effective than CO₂ in contributing to global warming. The GWP for a given gas depends on its atmospheric lifetime to destruction and its infrared absorption coefficient. Table 1 reports the GWP100 (calculated over 100years), and The GWP (calculated over an infinite time horizon) for different gases. Generally these gases are used as process gases in oxide etch processes, in CVD and Etch chamber clean processes, or formed as byproducts. The memorandum of

understanding (MOU) signed between EPA and semiconductor industry target five gases (CF₄, CHF₃, C₂F₆, C₃F₈, and SF₆) as belonging to these category.

Formula	Lifetime(years)	GWP(100 years)	GWP(infinite)
CO ₂	50-200	1	1
CH ₂ F ₂	5.6	560	
C ₃ H ₃ F ₅	2600	7000	130.000
CF ₄	50000	6300	850.000
C ₄ F ₈	32000	8700	
CHF ₃	250	12100	11.000
C ₂ F ₆	10000	12500	230.000
C ₃ F ₆	<1	Low	
NF ₃	740	8000	18.000

Table 1: PFC Characteristics

The HAPs are generally used as process gases in silicon and metal etch processes, or formed as byproducts in CVD clean processes. They are compounds that are hazardous to humans if released into the atmosphere. The EPA has identified some 189 HAP, examples of which are Hydrofluoric acid (HF), fluorine (F₂), Hydrochloric Acid (HCl), and Chlorine (Cl₂). Since elevated levels of these compounds in air are immediately

dangerous to life and health, the EPA has established strict concentration levels for each compound.

Volatile Organic Compounds (VOC) are defined as chemical based on carbon chains or rings (and also containing hydrogen) with a vapor pressure greater than 0.27 kPa at 25°C. These compounds may also contain oxygen, nitrogen and other elements, excluding carbon monoxide, carbon dioxide, carbonic acid, metallic carbides and carbonate salt. Generally these chemicals are used in tool and wafer cleaning processes or as coolant in heat exchangers. The industrial sites are required to limit the air emissions of VOCs. These compounds are also harmful to human health if released to the atmosphere.

1.3 Emission Reduction Strategies:

In 1999, the World Semiconductor Council set a voluntary goal of reducing PFC emissions to 10 percent below 1995 levels by 2010. PFC emission reduction can be divided in four technology areas listed below in order of preference.

Process optimization:

Certain processes use no more than 15 to 20 percent of the incoming gas, emitting 80 to 85 percent. Recent optimization studies conducted by tool manufacturers have shown increased efficiencies, as reported by “%conversion.” This practice involves the use of end-point detectors and process parameter variations to find the minimum level of PFC utilization to reduce excess emissions. In studies of the C₂F₆ CVD chamber cleaning

application (Algood 2000), it was found that greatest increase in efficiency was made by optimizing both the system operating pressure and the cleaning gas flow rate.

Alternative Chemistries:

These strategies required a search for an environmental friendly alternative for PFCs in CVD and etch applications. These options may require a radical modification of the process, gas and hardware, in order to improve the clean process performance and reduce emissions. Applied Materials have launched a new process technology, which employs remote plasma source (RPS) to yield minimum PFC emission.

Capture and Recycle:

This technology separates unreacted and process-generated PFCs from the other gases for further processing. This effluent treatment process allows for the possibility of some recycling or reuse of the captured PFC gas (Mocella, 1998). These systems can either repurify the PFC for reuse or they can concentrate the gas for subsequent offsite disposal.

Abatement:

This solution consists on reducing the amount of undesirable species emitted into atmosphere by destroying unreacted PFC molecules by means of plasma abatement, thermal destruction, or catalytic destruction. The plasma system dissociates PFC molecules, which reacts with an additive gas such as H_2 , O_2 , H_2O , or CH_4 in order to produce low molecular weight by products such as HF with no GWP. Wet scrubbers can then remove these product molecules.

Chapter 2

Literature Review

2.1 Semiconductor Process Emission Measurement

The ability to quantitatively characterize the effluent emission from the CVD and Etch tools is important to evaluate the environmental impact of semiconductor fabrication process, and the measurements have to be carried out using an approved methodology. The PFC leadership group developed industrial protocol for performing effluent emissions characterization (The Equipment Environmental Characterization Guidelines, (Rev.3.0)), which defines the role of semiconductor equipment suppliers in minimizing chemical consumption and production of waste emissions. The main requirements specified in this protocol are as follow:

1. Equipment: All gas emissions must be measured by mass spectroscopy and fourrier transform infrared (FTIR), downstream of the tool process pump.
2. Calibration: All quantification of signals should be accompanied by an in-situ calibration method.
3. Chemical mass balance: A chemical mass balance engineering analysis must be presented to show the composition and quantity of each chemical used in the process and each waste stream discharge from the tool. The mass balance must be on a per wafer basis, include chemical used and discharged during maintenance and wet clean,

and be based on actual measurement. The mass balance must account for >90% of fluorine, chlorine, and bromine used by the tool.

4. Reporting: The results have to be reported in a standard format that highlights the chemical mass balance. For the quantified compounds a calibration curve and quantitative analysis should be attached. For the compounds not quantified, an absolute intensity needs to be reported. Each data point should have associated statistical error (+/-10) generated either by repeating the process 5 times or deduced through a design of experiment methodology. An utilization efficiency of the chemical during the processes must also be reported.

2.2 Emission Reduction Approach

To ensure that new technology transfer to manufacturing do not impact the environmental performance of the semiconductor industry, Alaoui (2000) studied the process performance of the remote plasma source (RPS) for silicon carbide film (Blok) deposition on Applied Materials PECVD tool. Blok was introduced as an interlayer dielectric for copper damascene, to provide a barrier against copper diffusion, moisture, and impurities. RPS uses NF_3 clean gas, which dissociates to fluorine radicals that are very active and effectively etch the residues and clean the chamber. The QMS and FTIR were used to provide quantitative information on the process behavior, clean end point, clean rate, plasma behavior, and PFC emission. It was found that removing the carbon residues after the Blok deposition from the chamber walls using NF_3 chemistry forms CF_4 as byproduct. CF_4 is considered as high GWP PFC gas. Alaoui conducted a design of an

experiment to determine the effect of several variables (RF power, pressure, O₂ flow, and NF₃ flow) on the PFC (CF₄) emission, and to optimize the process. These variables were varied +/- 10% from the baseline values of 700 scc NF₃, 500scc O₂, 450W, 3.15Torr). The first result showed that RF power has the most effect on PFC emission. Increasing the power helps cleaning the chamber from carbon residues, and make CF₄ as byproduct. Increasing the NF₃ flow significantly improved the chamber clean time due to higher fluorine radicals available to clean the chamber. Alaoui also found that addition of Ar prevents the recombination of fluorine radicals to molecular fluorine and improve the clean time. The third result was the addition of oxygen minimizing the formation of the global warming CF₄ and instead forming COF₂, which is water scrubber.

Based on the DOE the optimum clean time was achieved with 2300sccm NF₃ diluted with 2300sccm Ar, 500sccm O₂, and 450W (Radio Frequency) RF power. This optimized recipe for Blok film emitted 2400KgCE per 10000 wafer of PFCs, which is not significant amount. This study showed the advantage of NF₃ remote clean for the new technology (Low k materials Blok) over the C₂F₆ in-situ clean (Raoux et al 1999) for oxide or nitride film deposition which emit 25 times more the amount of kgCE of PFC than RPS clean.

Using an alternative chemistry approach Chen et al. (2000) investigated the chemical vapor deposition (CVD) chamber clean using C₃F₈/O₂/NF₃ in situ plasma as an alternative to C₂F₆/O₂/NF₃ plasma clean. They found that an 85% reduction in PFC emission can be achieved and 76% mass reduction of gas usage. This was due to the fact that C₃F₈ has a lower global warming potential and shorter lifetime in the atmosphere.

Chen found also that the switching from 900 sccm $C_2F_6/O_2/NF_3$ to the optimized 150 sccm $C_3F_8/O_2/NF_3$ can reduce the clean time with 3% and increase the total deposition removal by 9%.

Algood et al (2000) reported the performance of four perfluorocarbon compound-based clean process (C_2F_6 , C_3F_8 , c- C_4F_8) and NF_3 - based clean process. The different chemistries were analyzed in terms of cleaning times, PFC emission, and gas costs. Oxygen was added to the Perfluorocompounds based process to avoid the formation of CF_4 as byproduct. His work showed (Figure 1) that the optimum SiO_2 etch rates occurred at different oxygen concentrations for C_2F_6 , C_3F_8 , and c- C_4F_8 when all other factors were held constant.

Figure 1: Oxide Etch Rates as a Function of Oxygen Content for C_2F_6 , C_3F_8 , and c- C_4F_8 (Allgood et al 2000).

The $c\text{-C}_4\text{F}_8$ has its highest etching rate at large (70-80%) oxygen content. The high O_2 content, favored the formation of COF_2 as a by-product, as opposed to the high GWP compounds CF_4 . Based on this initial result with $c\text{-C}_4\text{F}_8$, a DOE study was conducted. Figure 2 summarizes the data from the current DOE study for $c\text{-C}_4\text{F}_8$, along with those for several other gases that have been evaluated in the same tool.

Figure 2: Comparison of Various Clean Gases on a Novellus PECVD Tool
(Allgood et al 2000).

The DOE result showed that $c\text{-C}_4\text{F}_8$ can offer significant advantages in reducing PFC emissions (>85%), gas usage (>80% by weight), and clean time (~20%) as compared to a standard (non-optimized) C_2F_6 -based clean. The largest benefit was found with the NF_3 in terms of PFC emission reduction. However, NF_3 -based processes present other concerns such as the high level of F_2 emitted, which is considered a HAP. While considerable

progress has been achieved in reducing PFC emission from the CVD processes, the etch process remains more problematic to emission reduction strategies due to severe process requirements of dielectric etch. The requirements include the need to attain high etch rates, high aspect ratio and high selectivity to the oxide layer compared to the mask layer.

Doe et al (1999) conducted a study to model emission from Lam Research Corporations, for dielectric etch using, the new Excelan reactor. In this study, a contact etch process region was mapped by changing total flow and RF power for $C_4F_8/O_2/N_2/Ar$ chemistry using two factor experimental design. QMS and FTIR were used to determine the absolute concentration of unreacted process gases and reaction by product. In this study the main variables were C_4F_8 flow and power. The flow and RF power were varied by +/- 33% and +/- 28%, respectively from baseline ($6.5 C_4F_8/6.5 O_2/200Ar/ 20 N_2 / 1000W(27MHz) /2200W(2MHz)$), while other parameters of the process were fixed (Ar flow, 2MHz power, pressure, He backside pressure, and chuck temperature). The particular responses measured in these experiment designs were unreacted C_4F_8 , and the detected by product: PFCs (CF_4 , C_2F_6) and HAPs (SiF_4 , HF, F_2 , CO). To account for all species a mass balance was calculated. The fluorine closure percentages 85+/-3% was detected which indicates that all major F-species have been detected. The missing fluorine was accounted for in the fluorocarbon polymer deposition in the reactor and on the wafer. Through experimentation and statistical design techniques, a model had been developed that predicted emission in terms of PFCs and HAPs over a wide range of process parameters for this reactor. The model was in form of emission equation for the

reactor process. The equation used all the required steps for stabilization, process, dechuck and wafer transfer.

The model was used to evaluate adjustments in process and stabilization times, gas flow and power. The output was converted to the equivalent amount of CO₂ that was produced from each wafer. The result per wafer in terms of sccm output of PFCs are shown in Table 2, and clearly demonstrate the difference between the older system Rainbow 4520 with poor PFC process combination versus the newer Excelan efficient tool using optimized process.

Rainbow 4520 (old system)		Excelan (new system)	
CF ₄ Emission	37sccm	CF ₄ Emission	1-2sccm
CHF ₃ Emission	67sccm	C ₄ F ₈ Emission	1-2sccm
C ₂ F ₆ Emission	4sccm	C ₂ F ₄ Emission	3-7sccm
Total PFC Emission	108sccm	Total PFC Emission	9-11sccm

Table 2: Comparison of PFC Emission from Older to Newer Contact Etch Technologies
(Doe et al 1999)

The HAPs outputs, HF, SiF₄, CO and F₂, had also been modeled for the Excelan. Five runs within and outside the DOE fitted parameter space were also completed. The results of these 5 runs are shown in Table 3 along with the DOE predicted ones.

Wafer	Predicted COF2 (%)	Experiment COF2 (%)	Predicted HF (%)	Experiment HF (%)	Predicted SiF4 (%)	Experiment SiF4 (%)
A	30.5	31.4	36.8	15.7	33.2	27.1
B	22.1	23.7	17.4	24.6	32.6	21.9
C	22.5	22.8	22.1	22.8	35.6	35.8
D	18.0	18.2	24.8	25.0	37.9	37.5
E	22.2	22.8	22.0	22.8	34.7	34.2

Table 3: HAPs Predicted and Actual Measurements (Doe et al 1999)

Through this experimentation a dramatic PFCs and HAPs reduction had occurred for the new Lam Excelan process. The use of this model may allow an optimization of processes in terms of gas stabilization time, etch time, power levels gas ratios, and flows so as to reduce the environmental impact.

Another study was conducted by Sparks et al (2000) on the performance of the three isomers of C_4F_6 , hexafluoro-2-butyne, hexafluoro-1, 3-butadiene, and hexafluorocyclobuten, as an alternative to a global warming gas C_3F_8 based process for an inductively coupled high density plasma etch chamber. Their work showed that the hexafluoro-2butyne and hexafluoro-1, 3-butadiene reduce the emission for 80%, while the hexafluorocyclobuten exhibit emission reductions greater then 75%. This is due to the greater formation of C_2F_4 , which is not a global warming gas instead of CF_4 . The process

performance was assessed by cross-sectional scanning electron microscopy (SEM), based on the photoresist erosion, etch rate, via profile, gas emission, and utilization efficiency. It was found that all three of the isomers of C_4F_6 were capable of etch performance comparable to C_3F_8 process. There was no photoresist erosion, a good etch rate, and no indications of etch stop. The resulting emission was 0.0628 KgCE, which corresponds to a reduction of 82 %, compared to C_3F_8 process. The destruction efficiency was 99.5 %, indicating a near complete destruction.

2.3 Literature Review Summary:

The major conclusion from this literature review is that the ability to effectively measure and model individual tools is key to reduce air emission, and develop special treatment to these gases. The applicability of different PFC reduction technologies depends on several factors. Process optimization may be the best solutions to reduce PFC because of space constraint and low cost. The second favorable technology is alternative chemistry, which gives emission reduction 50% more than process optimization, but its required time and money to develop, and qualify the new processes. However, the affective way to further this improvement on the fab level is to design a model of emission, and consumption during the course of chip manufacturing.

Chapter 3

Purpose of Study

3.1 Process Performance:

The purpose of this study is to establish a model of gas consumption and emission on per wafer basis. At this point, global evaluation of the chip is extremely difficult because of the wide variety of new technologies (Al/W versus Cu. damascene, organic versus inorganic dielectrics). However in order to narrow the problem for this study, three assumptions were employed. First the characterization is made for individual module such as shallow trench isolation module (STI), gate module, via module, and interconnect module (Al/SiO₂, Cu/Low K materials). Second, the environmental impact will scale with number of layers used (Equation 1).

$$\text{Chip Emission} = \text{Shallow trench} + \text{Gate} + \text{Via} + N * \text{Interconnect} \quad (1)$$

Where N is the number of interconnecting level in chip (Figure 3). Third for the purpose of this research, we will limit ourselves to processes that present gaseous emissions that are of concerns for environmental impact. The next section defines the process sequence integration for every module studied.

Figure 3: A Cross Section of 5 Level Interconnects Structure

3.2 Module Process Sequence Integration

3.2.1 Shallow Trench Isolation Module:

A variety of techniques has been developed to isolate devices in integrated circuits. The first isolation technique proposed was Local oxidation of silicon (LOCOS). In the LOCOS, the oxide is selectively grown over the field regions (while the active area is protect by layer of silicon nitride.). LOCOS has been found inadequate for submicron chips because of the non-planar surface that prevent the deposition of uniform films above it, and effect the properties of the device. Bird's beak encroachment is also one of the negative aspect of LOCOS. Since oxidation occurs in two dimensions, some oxidant diffuses under the edges of the nitride where unwanted oxide grows. The oxide grown under the nitride can lift the nitride edge. The shape of the field oxide as it penetrates under the nitride has been given the name of bird's beak. The bird's beak is a lateral extension of the filed oxide into the active area of the device). To accommodate bird's beak it is necessary to make the active region larger. This uses extra chip real estate and is inefficient for ULSI circuit. A new process has been developed to eliminate bird's beak, shallow trench isolation (Figure 4). In STI, a shallow trench is etched into the silicon and the trench is oxidized and filled with deposited oxide to make it nonconducting. The device is built on the plateaus of silicon between trenches. Table 4 summarizes the process flow for STI.

Figure 4: Shallow Trench Isolation Module

Process Step	Process Condition	Process	Purpose
Pad Oxide	400Å	RTP	Etch stop layer
Nitride Deposition	1500-2000Å	LPCVD/HDPCVD	Polish stop layer
Nitride/Oxide Etch	1500-2000 Å	Dielectric Etch	Open the trench
Si Etch	8000-10000Å	Si Etch	Etch the trench
Thermal Oxidation	100-200Å	RTP	Prevent the damage caused by Etch
Trench Fill	8000Å	HDPCVD	Fill the trench
Corner Oxidation	1100C, dry O ₂	RTO	Minimize stress to the silicon lattice upon oxide fill

Table 4: Shallow Trench Isolation Module Process Flow.

3.2.2 Gate Module

The building block in VLSI devices is the metal-oxide-semiconductor field-effect transistor (MOSFET); usually this is implemented through the complementary metal oxide semiconductor (CMOS) transistor. The heart of a MOSFET is the gate, which serves as an insulator, gate metal from the channel electrically, so a voltage on the gate electrode can induce carriers in the channel to conduct current without leakage through the gate dielectric. In order to achieve good electrical properties, this gate dielectric should also be almost defect free and uniform for the current to pass through the channel. The process flow for the gate module is described in Table 5.

Figure 5: Gate Module.

Process Steps	Process Condition	Process Tool	Purpose
Thin oxide	55 A	RTP	Gate oxide
Doped Poly Si	2000 A	LPCVD	Gate Metal
SiN deposition	400A	LPCVD	Etch Stop Layer
ARC (TiN)	50 A	CVD	Anti reflective coating layer
Etch ARC/SiN/ Poly etch	500A	Dielectric etch	Gate Etch
Thin Oxide	100A	RTP	Oxidation
SiN deposition	1100 A	LPCVD	Spacer Formation
SiN/Oxide etch	Spacer Etch	Dielectric etch	Spacer Etch

Table 5: Gate Module Process Flow.

3.2.3 Via/Contact Module

The W-plug has been extensively used in production of advanced devices. At the contact level, the process flow for W plug formation is nowadays pretty much standardized, as is shown in Figure 6 and Table 6.

Figure 6: Via/ Contact Module.

Process Step	Process Condition	Process Tool	Purpose
Contact Etch	5000 A	Dielectric Etch	Etch the Via
Ti/TiN	TDMAT/TiCl ₄ , NH ₃	MOCVD	Barrier layer
W Deposition	WF ₆ /300 Torr	LPCVD	Fill the via

Table 6: Via/Contact Module Process Flow.

3.2.4 Al/SiO₂ Interconnect Module:

The interconnect module (Figure 7) is a metalization process that connects individual devices together by means of microscopic wires to form circuits. These wires are necessary for the circuit to function. Today nearly all integrated circuits use Al wiring with two to five levels. Multilevel metalization offers greater flexibility in circuit design and, even more importantly, a substantial reduction in die size, and thus, chip cost. The Al metals are deposited by a variety of techniques, but principally by physical vapor deposition (PVD) or by chemical vapor deposition (CVD). The processes flow for interconnect module is summarized in Table 7.

Figure 7: Al/SiO₂ Interconnect Module.

Process Step	Process Condition	Process Tool	Purpose
Ti/TiN Deposition	300A	TxZ Centura	Barrier layer
Al/0.5-1%Cu	8000A	PVD Endura	Metal deposition
Al Etch	8000A	DPS Centura	Metal Etch
1 st Oxide Deposition	8000-10000 A	Ultima HDPCVD	Intermetallic dielectric layer
2 nd Oxide Deposition (Cap Layer)	10000 A	Producer PE	Intermetallic dielectric layer (Cap Layer)

Table 7: Al/SiO₂ Interconnect Module Process Flow.

3.2.5 Cu/low k Interconnect Module:

The migration from Al-Alloy metallization to Cu and the push towards low-k materials has been driven by the need to improve the RC delay, power dissipation, and electromigration of advanced interconnects. Cu doesn't form volatile copper fluoride and chloride. Thus, instead of patterning and etching Cu films, it is more advantageous to blanket-deposit Cu films into recesses in dielectric layers, and then polish them away by CMP in flat areas above. This is the basis of the damascene interconnect structure. Several methods of forming dual damascene are available. These methods can begin by either patterning the interconnects or via first. In this study the via first approach was used.

Figure 8: Cu/lowK Interconnect Module.

Process Name	Description	Process condition	Process tool
Via Dielectric	BD/FSG	8000A	HDPCVD
Via Etch Stop	SiN	600A	PECVD
Trench Dielectric	BD/FSG	6000A	HDPCVD
Via Lithography	PR	PR	Photolithography
Via Etch	Oxide Etch	0.5 um	EMaxP+
Trench Lithography	PR	PR	Photolithography
Trench Etch	Oxide Etch	L/S=0.84/0.64	EmaxP+
Post Etch Clean			Wet Clean
Barrier Layer	TiSiN	250A	CVD
Cap layer	SiN	350-1000A	PECVD

Table 8: Cu/lowK Interconnect Module Process Flow.

Chapter 4

Experimental Instrument

4.1 Introduction

The experiments were done at Applied Materials. As one of the semiconductor equipment companies, Applied Materials is working on achieving a high standard of environmental quality. Following the industry protocol, FTIR and QMS has been used for evaluation and measurement of effluent emission of CVD and Etch tools. This chapter focuses on the description of QMS and FTIR and the theory behind these instruments.

4.2 Theory of Quadrupole Mass Spectrometer

Several different analytical techniques are used to determine component gases in mixtures. In this study a quadrupole mass spectrometry is used. Quadrupole mass spectrometers are the most common type of gas analyzer for vacuum applications. They are often used in vacuum systems where it is useful to know both the partial pressure of component gases, and the total pressure of the system. Partial pressures are determined by ionizing atoms and molecules, mass filtering ions, then detecting these ions. Atoms and molecules are first ionized to provide an electronic handle by which ions can be separated and subsequently detected. After ionization, the quadrupole rods serve as sets of tunable high and low band pass filters, allowing only the ion species of interest to reach the detector.

The detector measures the ion current directly or, using an electron multiplier detector measures an amplified signal proportional to the ion current. Through the use of well-designed electronics circuitry, it is possible to quickly and efficiently determine the partial pressures of gases in the system (MKS Orion Compact 2000).

Figure 9: Mass spectrometer Component

Ionization

During ionization, a steady stream of positively charged ions is created for subsequent separation by the quadrupole rod set. A resistively heated filament that emits electrons begins the ionization process. These electrons are drawn toward a positively charged ion cage. Inside the ion cage, a few of the electron collide with the atoms or molecules, causing the removal of one or more electrons from them, thereby creating positive ions. These ions are then drawn toward the lower potential of focus plate. From this focus plate, the positive ions are injected into the quadrupole rod set. The ionization rate of gases species depends in part on the stability of the atom or molecule. The ionization rate also depends on the ionization energy of the ion source.

Quadrupole Mass filter

The quadrupole mass filter separates ions by molecular weight (more specifically by mass/charge ratio). The filter consists of four rods, with opposite rod pair interconnects. One-rod pair is connected to a positive DC voltage upon which a sinusoidal RF voltage is superimposed. The other rod pair is connected to a negative DC voltage upon which a sinusoidal RF voltage is superimposed, 180° out of phase with the RF voltage on the first set of rods.

The net result is that the rod sets act as high-and low-band passes filters. Through precise construction and proper electronic tuning, these rod sets can separate all but the desired mass species of interest. One of the rod sets neutralizes lighter ion, and the other set neutralizes heavier ions. The mass species of interest continues toward the detector. By simultaneously varying the amplitude of the DC and RF voltages, an entire mass spectrum can be scanned quickly (MKS Orion Compact 2000).

Detection

The ion detector consists on an electron multiplier (EM) and a Faraday cap (FC). Faraday cup is a simplest detector, a small metal bucket at one end of the quadrupole rod sets. At the Faraday cup, an electrometer amplifier measures the ion current as electrons are given up to the ions that contact its surface.

The electron multiplier detector can be used to enhance the spectrometer sensitivity. The EM consists of a conductive glass tube with a cone mounted on its front end. Positive ions strike the cone and the secondary electron emission produces electrons. These secondary electrons subsequently are accelerated down the channel of the EM and

produce cascades of more secondary electrons. For each ion entering the cone of the EM, 1000 to 1,000,000 electrons are collected at the exit. An electrometer amplifier then measures the electron current (MKS Orion Compact 2000).

4.3 Theory of Fourier Transform Infrared

Absorption in the infrared region results in changes in vibrational and rotational status of the molecules. The absorption frequency depends on the vibrational frequency of the molecules, whereas its intensity depends on how effectively the infrared photon energy can be transferred to the molecule. This is due to a change in the dipole moment that occurs as a result of molecular vibration. A molecule will absorb infrared light only if the absorption causes a change in the dipole moment. Therefore all elemental diatomic gases (such as N_2 , H_2 and O_2) are not detectable by FTIR. Other components present in flue gas can be analyzed by their characteristic infrared absorption.

If only one species is to be analyzed, a species-specific instrument can be used. However in this research a mixture of different gases is characterized so a Fourier transform infrared (FTIR) spectrometer is used because it is faster and has better signal to noise ratio. The interferometer used in the FTIR instrument is based on the same principal as interferometer originally designed by Michelson in 1891.

The Michelson interferometer is a device that can divide a beam of radiation into two paths and then recombine the two beams after a path difference has been introduced. A condition is thereby created under which interference between the beams can occur.

The intensity variations of the beam emerging from the interferometer can be measured as a function of the path difference by the detector. A form of the Michelson interferometer is shown in Figure 10. It consists of two mutually perpendicular plane mirrors, one, which can move along an axis that is perpendicular to its plane. The movable mirror is either moved at a constant velocity or is held at equally spaced points for fixed short time periods and rapidly stepped between these points. Between fixed mirror and the movable mirror is a beamsplitter where a beam of radiation from an external source can be partially reflected to the fixed mirror and partially transmitted to the movable mirror. After the beams return to the beamsplitter, they interfere and are again partially reflected and partially transmitted. Because of the effect of interference, the intensity of each beam passing to the detector and returning to the source depends on the difference in path of the beams in the two arms of interferometer. The variation in the intensity of the beams passing to the detector and returning to the source as a function of the path difference ultimately yields the spectral information in Fourier transform spectrometer.

Figure 10: FTIR Spectrometer (Nicolet Instrument Corporation <http://www.ftir.cz> 2001).

EXPERIMENTAL METHODOLOGY

QMS and FTIR spectroscopy is used for all sampling. The sampling scheme for analysis is shown in Figure 11. Samples are drawn through 0.125" stainless steel tubing from 0.25" stainless steel VCR fittings which are connected directly to the process exhaust lines. Samples are drawn through both instruments using separate mechanical pumps. The pumping speed is controlled by a throttle valve located on the exit of the instrument to yield a sampling pressure to 740 Torr for the FTIR and the QMS. The pressure is monitored with capacitance nanometers located immediately downstream of the FTIR gas cell. The sample lines are heated to about 110⁰ C to eliminate the water vapor from the lines. The exhausts from both instruments are safely vented back to the scrubber exhaust.

Figure 11: Schematic of Experimental Set up (EM&T Applied Materials)

5.2 Instrumentation

5.2.1 Quadrupole Mass Spectrometer

The total pressure in the QMS is adjusted to 10^{-6} Torr by adjusting the electron multiplier voltage. Analyses are accomplished in static mode (0-200 AMU) and in selected peaks mode (up to 10 monitored ion species). The response time of the QMS (time between the beginning of injection of the gas in the process chamber and the detection in the QMS) is less than 25 seconds.

5.2.2 Fourier Transform Infrared Spectroscopy

FTIR measurements are performed using a Nicolet NexusTM spectrometer with a 5-cm gas cell. The FTIR spectral series are recorded with an 8 cm^{-1} resolution with each spectrum being an average of 16 scans.

5.2.3 Calibration

The instrument calibrations are performed after each experiment using a dynamic calibration system. The calibration curves were obtained by dynamic dilution of gas standards (1 vol% in N₂ carrier) with pure N₂ gas, and by plotting the intensity versus the concentration of each compound. The concentration can be calculated by the equation:

$$C_{\text{ppm}} = 10^6 V_a / (V_d + V_a) \quad 2$$

Where V_d, and V_a are the volume of the diluent (N₂), and the desired compound. (Refer to Appendix A for examples on calibration curves obtained during this research)

5.2.4 PUMP PURGE

During this study, the measurements are made downstream of the process pump; the process byproducts are diluted with the nitrogen pump purge. To determine the actual

volumetric emissions, it is necessary to calculate the pump purge dilution factor. The pump purge is determined by flowing NF_3 gas from the CVD tool, without igniting the plasma, at different flow rates (from 0.5 to 0.05 liter/minute) and then by measuring its concentration using the QMS, which had been previously calibrated for NF_3 . The pump purge is determined by Equation (1).

$$N_2 = (\text{NF}_3_{\text{slm}} \times 10^6) / [\text{NF}_3_{\text{ppm}}] - \text{NF}_3_{\text{slm}} \quad (3)$$

5.3 EXPERIMENTAL PROCEDURE

5.3.1 Mass Balance

From the equivalent halide inlet and outlet amounts, a mass balance closure on the halogen fluorine, bromine, and chlorine is performed. Equivalent halide out (E.H.O) is calculated by equation (4):

$$\text{E.H.O. (x)} = \text{Volume emitted of Compound X} * \text{number of halides in compound X} \quad (4)$$

Similarly the Equivalent halide in (E.H.I) is calculated by equation (5):

$$\text{E.H.I.(x)} = \text{Volume of process compound used for compound X (from recipe)} * \text{number of halides present in compound X} \quad (5)$$

The mass closure is then calculated by equation (6):

$$\text{Mass closure} = (\text{total amount of E.H.O} / \text{Total amount of E.H.I}) * 100 \quad (6)$$

If the experimental errors are taken into account, a mass balance closure of >90% is acceptable. However, if the mass balance did not close further experiments will be conducted. (Refer to Appendix B for an example of process study during this research.)

5.4 Experimental Plan

The fabrication of an entire chip can involve as many as 300 distinct manufacturing steps, although many of these processes are just repeated in a cycled fashion (dep, etch, lithography...). In order to build a model of emissions on a per wafer basis, we characterized 25 processes from Applied Materials' equipment set, for each process the utilization efficiency of the reaction precursors was evaluated, the formation byproduct was quantified and a mass balance closure is performed. Then we build models of chemical consumption and emissions on a per module basis. We established the process flow and emissions for five major modules: a Shallow Trench Isolation (STI) module, a Gate module, a Via module, and two Interconnect modules (standard interconnecting and dual damascene). After each module has been characterized, a model of chemical consumption and emission can be built, based on generic chip processes flow, by just adding the contribution of each module. In this study a five level interconnect structure is characterized. A flow chart of experimental plan is shown in Figure 12.

Figure 12: Flow Diagram of the Experimental Plan.

Chapter 6

RESULTS AND DISCUSSION

6.1 Shallow Trench Isolation and Gate Modules

In these modules a total of 11 processes were characterized where 7 are CVD processes, and 4 are etch processes. Figures 13 and 14 show the consumption and emission of gases during the fabrication of the STI and gate modules.

SiH_4 , NH_3 , and PH_3 are process gases used for CVD, and they represent 55 percent of the total gas consumption. The highest consumption is NH_3 , 14.92-g/ wafer; which correspond to 53 percent of the total. NH_3 is used with SiH_4 in deposition of silicon nitride (Si_xN_y) which is used as sidewall spacer in gate module and etch stop layer in STI module. The high level of ammonia consumed is due to the poor utilization efficiency during the process. The second major gas consumed is NF_3 , 29 percent. This gas is used in all CVD processes to clean the chamber walls from the residues after the deposition processes. PH_3 (1 %) is used as doping gas to the CVD reactant gases. In this case it is used with SiH_4 to deposit a doped polysilicon film for the gate module. The last 16 percent are from etch processes. CF_4 , 5 percent, CHF_3 , 1 percent, Cl_2 , 1 percent, SF_6 , 1 percent, Cl_2 , 1 percent, and HBr , 8 percent. The gases selected for the etch are either inherently reactive (such Cl_2), or can be dissociated into molecular fragments (that are then reactive- for example, CF_4 , a molecule that can be dissociated into such reactive species as F , CF_3 , CF_3^+ , etc).

Overall, it was observed that 84 percent of the consumption gases are from the CVD, and 16 percent are from the etch processes.

The major emission also come from the CVD (83 percent) and 17 percent from the etch processes. As shown in Figure14, NH_3 is the largest portion of the emission (42 percent). This is due to the low destruction efficiency of this gas, which points out the need to optimize the silicon nitride LPCVD process. The second challenge is the high emission of fluorine molecule (F_2), 35 percent. F_2 is a hazardous air pollutant. The fluorine is due to recombination of atomic fluorine during the remote clean process. On one hand remote clean technology helped to eliminate the PFC emission from the CVD processes, on the other hand, it contributed to increase of hazardous air emission by generating F_2 as byproduct. The rest of the gases are etch byproducts and represent 17 percent of total emissions.

Figure 13: Gas Consumption for STI and Gate Module for 300mm Tools.

Figure 14: Gas Emission for STI and Gate Module for 300mm Tools.

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
NF ₃	GWG	8.21	10.02
CF ₄		1.35	
CHF ₃		0.31	
SF ₆		0.15	
PH ₃	HAPs	0.25	17.87
HBr		2.31	
Cl ₂		0.39	
NH ₃		14.92	
TDMAT	VOC	0.016	0.016
SiH ₄	FLAM	0.28	0.28

Table 9: Gas Consumption for STI and Gate Module.

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
NF ₃	GWG	0.06	1.15
CF ₄		0.812	
CHF ₃		0.22	
SF ₆		0.059	
NH ₃	HAPs	7.53	16.46
F ₂		6.24	
Cl ₂		0.007	
HBr		0.33	
SiF ₄		0.793	
HF		0.066	
COF ₂		0.02	
HCl		0.155	
SiCl ₄		0.193	
SiBr ₄		0.037	
Br ₂		1.094	
MMA	VOC	0.13	0.13
DMA		0.0010	
SiH ₄	FLAM	0.126	0.126

Table 10: Gas Emission for STI and Gate Module.

6.2 Interconnect Module

Copper is replacing the tungsten and aluminum metalization for chip manufacturing. Also low k materials for interconnect ILD are replacing the SiO₂ such as, Fluorosilicate glass (FSG) (with a k between 3.0 to 3.6) and carbon doped silica glass (Black diamond, BD) which has a k value of about 2.8.

In this section, the environmental performances of three different interconnect modules were studied: standard Al/SiO₂ interconnect module, Cu/ FSG dual damascene

interconnect module, and Cu/BD dual damascene interconnect. These analyses give some indication about the challenges coming ahead and how the shift to low k materials and dual damascene interconnect structures effect emissions of PFCs, Volatile organic compounds (VOCs), and Hazardous Air pollutant (HAPs).

6.2.1 Via and Al/SiO₂ Interconnect Module

Figures 15 and 16 show the consumption and emission of gases during manufacturing of the interconnect module on a 300mm tool set. In Figure 15, SiH₄, TEB, TEOS, and WF₆ are the gases used for CVD film deposition, and they represent 27 percent of the total gases. NF₃ is used for CVD chamber cleaning and represents 62 percent of the overall gas consumption. The rest of the gases (C₄F₆, BCl₃, Cl₂, CHF₃) are etch process gases and represent only 11 percent of the total consumption, due to the relatively low flows used for these applications. One can observe from this data that greater amounts of chamber clean gas are used, compared to process gases. This highlights the need to optimize CVD chamber cleaning processes.

Figure 16 illustrates the emitted gases from interconnects module tool set. PFC represent 64 percent of the total gas consumption but only 6 percent of the PFC gas emission, this drop indicates a good utilization efficiency of these gases during the processes. The large PFC emission reduction (97 percent) has been achieved at the cost of increasing the emission of hazardous air pollutants, which is regulated and must be abated. In this module, HAPs represent 90 percent of the overall emissions (80 % is from CVD processes and 10 % from the etch processes). Sixty percent of the HAPs emissions originate from CVD chamber cleaning due to the high concentration of fluorine generated

during this process. Only 20 percent of the fluorine atoms from the initial NF_3 feedstock contribute to the cleaning reaction to form SiF_4 and the remainder is emitted in the form of F_2 . The VOCs consumed are used for CVD (TEOS, TDMAT, TEB, and TEP) and relatively high destruction efficiency is achieved for this compounds.

Figure 15: Gas Consumption for Standard Al/SiO₂ Interconnect Module

Figure 16: Gas Emission for Standard Al/SiO₂ Interconnect Module

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
hNF ₃	GWG	16.71	17.303
CHF ₃		0.593	
Cl ₂	HAPs	0.757	5.01
BCl ₃		1.063	
C ₄ F ₆		0.55	
WF ₆		2.64	
TEOS	VOC	3.44	4.029
TDMAT		0.032	
TEB		0.456	
TEPO		0.101	
SiH ₄	FLAM	0.626	0.626

Table 11: Gas Consumption for Standard Al/Oxide Interconnect Module

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
NF ₃ CF ₄ CHF ₃ C ₂ F ₆	GWG	0.248 0.305 0.412 0.168	1.13
F ₂ SiF ₄ HF CO C ₄ F ₆ COF ₂ WF ₆ Cl ₂ BCl ₃ SiCl ₄ AlCl ₃ HCl	HAPs	10.61 1.303 0.0395 0.506 0.05 0.475 1.7 0.42 0.762 0.044 0.286 0.136	16.32
TEOS MMA DMA	VOC	0.008 0.26 0.0032	0.27
SiH ₄	FLAM	0	0

Table 11: Gas Emission for Al/SiO₂ Interconnect Module

6.2.2 Cu/FSG Interconnect Module

For Damascene FSG, the low dielectric constant is the key factor for being compatible with copper. The fluorine concentration has to be above 5 %, which exceeds the upper limit for stability of the conventional film. HDP-CVD fluorine doped silicon oxide (FSG) thin film is an attractive solution to replace the conventional silicon dioxide as intermetal dielectrics for Cu damascene device technology. The main advantages with this material are: a) It can be deposited in a conventional HDP-CVD system which has

been widely used for the USG and FSG gap fill application. b) It has a better process scheme in terms of reliability, stability and throughput than the other candidates.

c) Electrical performance should be significantly improved by the dielectric constant reduction from 4.2 to 3.5.

It is also important to identify the environmental performance of the Cu/FSG dual damascene module. A model of emission and consumption was put together.

The processes characterized are FSG HDPCVD, and Blok PECVD each used twice in the model, for the via, and trench dielectric layers and via trench etch stop layers.

Figure 17 and table 13 illustrates the total gas consumption for this module.

NF₃ is consumed in the largest amount (78 percent of the total). Again this result shows the high clean gas used compared to process gas. The process gases (SiF₄, SiH₄, TDMAT, TMS) signify 14% of the whole consumption, silicon tetrafluoride (SiF₄) is 6%, and silane SiH₄ is 2%. SiF₄ and SiH₄ are constituent gases for FSG film.

TDMAT 1% is a precursor for TiN, which is used as barrier layer in dual damascene. Trimethyl silane (TMS) is 3% of the total consumption and is a process gas for Block which acts as an etch stop layer, and also barrier layer to prevent copper, moisture, and impurities diffusion.

Figure 18 shows the gas emission from this module. The major byproduct formed is fluorine (F₂), which is due to recombination of atomic fluorine generated by the decomposition of NF₃. Once again, CVD processes are a big challenge in gas emission from the semiconductor industry. Even with the transfer to new technology and implementation of new materials, they still represent 96% of the total emissions.

The Etch gases are only 4% in the damascene structure. Comparing NF_3 emitted to consume, it is clear that the remote clean technology ensures near-complete dissociation of the cleaning gas. SiF_4 gas represents somehow a significant amount in the total emission, because it is formed when silicon based films are etched with fluorine atoms. The rest of the gases are etch byproducts.

Figure 17: Gas Consumption for Dual Damascene Cu/FSG Interconnect Module for 300mm Tool

Figure 18: Gas Emission for Dual Damascene Cu/FSG Interconnect Module for 300mm

Tool

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
NF3	GWG	21.98	23.016
CHF3		1.04	
C4F6	HAPs	1.10	2.75
SiF4		1.65	
TDMAT	VOC	0.02	2.35
TMS		1.71	
SiH4	FLAM	0.63	0.63

Table 13: Gas Consumption for Dual Damascene Cu/FSG Interconnect Module
for 300-mm tools

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
NF3	GWG	0.254	0.82
CF4		0.195	
CH4		0.00034	
CHF3		0.128	
C2F6		0.198	
CO2		0.046	
COF2	HAPs	0.099	14.17
F2		10.47	
SiF4		3.15	
HF		0.275	
CO		0.12	
C4F6		0.05	
MMA	VOC	0.13	0.61
TMS		0.48	
DMA		0.0010	

Table 14: Gas Emission for Dual Damascene Cu/FSG Interconnect Module
for 300-mm Tools

6.2.3 Cu/BD Interconnect Module

In order to reduce the interconnect capacitance and increase the speed for sub-0.25 mm devices, a low k interlayer dielectric (< 3.0) is required. One promising candidates of is Black Diamond (BD), which is a trademark low k product from Applied Materials, Inc.

BD is used with copper dual damascene. Copper metalization brings four new technologies to a fab: barrier deposition, copper seed layer, fill copper deposition, CMP (chemical mechanical polishing). With the implementation of BD, the total PFC emission increased due to the formation of CF_4 as a byproduct of the removal of the C-containing residues. Another challenge for Cu/ BD dual damascene structure is the increase of VOCs

emissions after BD and Blok deposition, due to the low utilization efficiency of Trimethyl silane (TMS). This brings the necessity of BD, and Blok process optimization.

Figure 19 and Table 15 describe the gas consumption and emission from the Cu/BD interconnect module. The major gases consumed are NF_3 (53 percent), which is used to clean the chamber after the deposition of Blok and BD, and TMS 43% which is one of the CVD precursors. The etch processes represent 4% of the consumption gases: 2% is C_4F_6 , 2% is CHF_3 .

The major byproduct is fluorine (39 %), again originated from the NF_3 remote clean. Finally TMS represents 23% of the total emission.

Figure 19: Gas Consumption for Dual Damascene Cu/BD Interconnect Module
for 300-mm Tools

Figure 20: Gas Emission for Cu/BD Module for 300-mm Tools

Chemical	Category	Mass (g/wafer)	Total (g/wafer)
NF3	GWG	22.94	23.97
CHF3		1.036	
C4F6	HAPs	1.1	1.1
TDMAT	VOC	0.016	19.12
TMS		19.11	

Table 15: Gas Consumption for Dual Damascene Cu/BD Interconnect Module
for 300-mm Tools

Chemical	Category	Mass(g/wafer)	Total (g/wafer)
NF3	GWG	0.20	3.38
CF4		2.24	
CHF3		0.56	
C2F6		0.13	
CO2		0.20	
		0.05	
COF2	HAPs	1.08	17.50
F2		8.04	
SiF4		5.15	
HF		3.06	
CO		0.12	
C4F6		0.05	
MMA	VOC	0.13	8.57
TMS		8.44	

Table 16: Gas Emission for Dual Damascene Cu/BD Interconnect Module
for 300-mm Tools

6.3 Model of Gas Consumption and Emission for Different Chip

In this section a model of chemical consumption and emission for three different generic chips was built. The first one uses one STI and gate module and five via and Al/SiO₂ interconnect module. The second chip has one STI and gate modules, one Al/SiO₂ interconnect module, and four Cu/FSG dual damascene interconnect modules. The third one uses one STI and gate modules, one Al/SiO₂ interconnect module, and four Cu/BD dual damascene interconnect module. By comparing these models of emission on a per wafer basis, we can evaluate the air emission related to the transfer to new technology Cu/low K dual damascene structure.

Figure 21 presents the gaseous consumption and emissions for a logic process flow using a 5 level Al/SiO₂ interconnect module. In this model, the interconnect portion represented 47% of all the gases consumed, the via modules accounted for 41%, the STI for 7% and the gate module for 5%. The majority of the gases consumed were global warming compounds (96.54g/wafer) out of which 96% were used to clean the CVD chambers. The remaining 4% were being consumed by etch processes. VOCs represented the second most important category of precursors, dominated by TEOS and TDMAT. HAPs consumption (42g/wafer) comes third with WF₆, NH₃, BCl₃ and Cl₂ being the major ones. In terms of emissions, one can observe that most of the precursors have been transformed into HAPs (92% of all emissions). Once again, the CVD chamber cleaning method is the major source of HAPs (58%), due to high F₂ emissions. Regarding global warming emissions, the overall PFC conversion is good (93%) because of the good performance of the remote clean to destroy NF₃. From the 8g of global warming gases emitted during the process, 64% originated from the etch processes, indicating the need for PFC abatement from these processes. Overall, one can conclude that the number one problem in terms of gas consumption is the NF₃ consumed during CVD chamber cleaning and the number one emission problem is fluorine from this same step.

Figure 21: Gas Consumption (left) and Emissions (right) from a 0.25 μm Generic Logic Device using Al/SiO₂ Interconnect Materials.

Figure 22 presents the gaseous consumption and emissions for a similar chip at the 0.25 μm technology node, but using FSG/Cu Dual damascene. In terms of consumption, one can observe that the consumption of GWG increased from 96.5g/wfr to 123 g/wafer. This due to additional steps used in dual damascene structure. However the destruction efficiency of PFC is similar to the previous chip with an overall conversion of 95%. The total mass of chemicals used and emitted during the process has increased from figure 21, but this is due to the fact that we are using a dual damascene structure where 2 additional steps have been added. The overall efficiency of the processes did not improve by moving to the Cu/FSG interconnect scheme. The same challenges are facing the Cu/FSG technology: the fact the CVD chamber cleaning is the biggest contributor both in terms of gas consumption and emissions.

Figure 22: Gas Consumption (left) and Emissions (right) from a 0.25 μ m Generic Logic Device using Cu/FSG Dual Damascene Interconnect Module.

Figure 23: Gas Consumption (left) and Emissions (right) from a 0.25 μ m Generic Logic Device using Cu/BD Dual Damascene as Interconnect Module.

Figure 23 is a model of consumption and emissions using Cu and Black Diamond. Similar Remarks can be made as in the previous examples. First, one can observe that the GWG gas conversion as dropped from 95% to 90% which is due to the fact that CF₄ is generated as a byproduct of the Black Diamond cleaning process. Further optimization of this clean process should be pursued to minimize CF₄ emissions. For example O₂ can be added to the process and generate COF₂ and CO₂ as byproducts of the carbon-containing

residues. Second, one can observe that the VOC consumption has greatly increased due to the use of trimethylsilane (TMS) as a precursor for Black Diamond. Volatile Organic Compounds also represent an increased portion of the emissions (28%) due to the relatively low utilization efficiency of TMS during the low k deposition process. Other VOC emissions originate from the Ti/TiN deposition and the decomposition of TDMAT into methylamine and dimethylamine byproducts. These results point out the need of a proper VOC abatement solution to be integrated into the tool.

Chapter 7

Conclusion & Future Research

7.1 Conclusion

A total of 25 processes were characterized, and a model of consumption and emission on a per chip basis was built. The model includes all type of air emission PFCs, VOC, HAPs. This module highlights the environmental issues coming with the migration to new technology Cu/Low K structures. From the data presented in this study, it can be concluded that:

- 1) Overall the major emission is coming from the CVD processes which represent 80% of the total emission.
- 2) Greater amount of chamber clean gas is used, compared to process gases.
- 3) Large PFC emission has been achieved around 97 percent in CVD processes with the introduction of NF₃ Remote cleanTM technology.
- 4) The NF₃ remote cleanTM technology introduce an ancillary challenge is emission of Fluorine F₂, hazardous air pollutant.
- 5) The VOC emission is going to become an increasingly important issue with the implementation of low k materials.
- 6) The migration to Cu/Low k dual damascene structure increase the total gas emission and consumption, due to additional steps used in Cu damascene, barrier deposition

7.2 Future Research

The model of consumption and emission shows that a great improvement has been made in reduction of PFC emissions. However, a destruction of PFC introduces an ancillary challenge because they generally result in an increase in HAPs emission, which are regulated by EPA. Therefore, an optimization is required to reduce the HAPs emission. The second issue is the high consumption of the cleaning gas NF_3 , which caused a gas shortage, and inflated the price of the gas, and gave rise to high gas cost per wafer. Studies should be carried out to optimize the cleaning processes and find alternative lower cost gas. Another issue with the switch to Cu/Low k is the increase of VOCs emission, which will require usage of proper abatement solution.

APPENDIX A

Calibration

The calibration curves used in the emission characterization of these processes CF_4 , HF , F_2 , NF_3 , TEOS , CH_4 , $\text{C}_2\text{H}_6\text{O}$ and SiF_4 were obtained by dynamic dilution of gas standards (1 vol% in N_2 carrier) with pure N_2 gas. Table A .1 summarizes the IR absorption bands or selected AMUs for the different species detected during the measurements. The methods used to quantify emissions are also indicated.

Species	NF_3	CF_4	SiF_4	F_2	CO	$\text{C}_2\text{H}_6\text{O}$	CH_4
IR region (cm^{-1})	909	1280	1028		2209.5-2149.7	1062-1069	~3016
QMS(amu)	52	69	85	38			
Quant. method	FTIR	FTIR	FTIR	QMS	FTIR	FTIR	FTIR

Table A.1: Summary of effluent species and detection methodology.

CO Calibration:

Figure A.1: Carbon Monoxide Calibration Curve obtained with FTIR.

NF₃ Calibration:

Figure A.2: Nitrogen Trifluoride Calibration Curve obtained with FTIR.

F₂ Calibration (AMU 38):

Figure A.3: Fluorine Calibration Curve obtained with QMS (AMU 38).

SiF₄ Calibration (AMU 85):

Figure A.4: Silicontetrafluoride Calibration Curve obtained with QMS (AMU 85).

CH₄ Calibration (3080-3089)

Figure A.5: Methane Calibration Curve obtained with FTIR (3080-3089).

CF₄ Calibarion

Figure A.6: Carbon Tetrafluoride Calibration Curve obtained with FTIR (1267-1258).

APPENDIX B

Mass Balance

A fluorine mass balance was evaluated for this process in order to estimate the destruction efficiency of NF_3 , and to quantify the PFC emitted from the processes. Typical FTIR Spectra and time resolved QMS spectra are shown in Figures B.1 and B.2 respectively for the cleaning process.

Figure B.1: Typical FTIR spectrum recorded during the clean process

Figure B.2 : Time resolved QMS response during clean process.

The quantitative analysis, utilization efficiencies and kg of carbon equivalent (kgCE) recorded during the clean processes for is summarized in Table B.1

Emission Compounds	Vol.Out (sl/Cln)	Equiv.O ut Halide	Mass.Out (g/Cln)	util.Eff (%)	KgCE (10Kwfr/100yrs)	F.Vol Clos(%)
NF3 In	2.69	8.07	8.53		58727.13	81
NF3 Out	0.02	0.06	0.07	99		
F2	1.37	2.73	2.32			
SiF4	0.89	3.58	4.15			
CF4	0.02	0.08	0.08		350.11	
HF	0.11	0.11	0.10			
CO2	0.45	-	0.89		5436.24	
Overall	2.87	6.57	7.61		5786.35	

Table B.1: Averaged Emissions During Cleaning Process.

It was observed that the utilization removal efficiency of NF_3 was better than 99%. The Remote CleanTM technology ensures near-complete dissociation of the clean gas, and greatly reduces global warming emissions from the process, compared to classical *in-situ* clean processes. It must be noted that the major byproducts of the clean process is Silicon Tetrafluoride (SiF_4) and Fluorine (F_2). These indicate the efficiency of the clean and the high utilization efficiency of the fluorine atoms generated in the remote clean. It must also be noted that the overall fluorine mass balance was closed only to 81% suggesting that some fluorine containing residues might have been formed in the foreline.

APPENDIX C

GLOSSARY

- BD:** Carbon doped silica glass (Black Diamond), trade mark of low k materials from Applied Materials.
- Blok:** Barrier low k is a silicon carbide film used as barrier layer to prevent copper diffusion.
- BPSG:** Boron- and Phosphorous-Doped Silicon Glass.
- CMOS:** Complementary Metal Oxide Semiconductor. Any MOS device that incorporates both p-channel and n-channel structures within the same silicon substrate.
- Contact:** Regions of exposed silicon, covered with metal material in the metallization process, that provide electrical access to the device.
- CVD:** Chemical Vapor Deposition is the formation of solid thin film on a substrate by the reaction of vapor phase chemicals that contain the required constituents.
- Damascene:** A way of making metal lines, which involves depositing an insulator (oxide), etching a trench in the oxide, depositing metal everywhere and then polishing back with CMP so there is just metal left in the trench.
- Dielectric:** The nonconducting material used to separate the plates of a capacitor or to separate metal lines.
- FSG:** Fluorine Silicate Glass, dielectric film with dielectric constant between

3.0 to 3.6.

FTIR: Fourier Transform Infrared is an instrument that measures the interaction of matter with infrared radiation.

GWP: Global Warming Potential represents how much a given mass of chemical contributes to global warming compared to the same mass of carbon dioxide.

HAP: Hazardous Air Pollutant.

HDPCVD: High Density Plasma Chemical Vapor Deposition.

Interconnects: Electrical conducting paths that are formed during the metallization process.

ILD: Interlayer dielectric, insulating films between the wafer surface and the first metal layer.

IMD: Intermetal dielectric, insulating films between two conductive layers.

KgCE: Kilogram of carbon equivalent is measured of the equivalent mass of CO₂ Emitted into the atmosphere in kilograms.

LOCOS: Selective thermal oxidation of silicon where the oxidation takes place only in exposed holes in a SiN masking layer.

LPCVD: Low Pressure Chemical Vapor Deposition.

MOCVD: Metal Organic CVD, method of depositing metal into contact holes.

PECVD: Plasma Enhanced CVD.

PFC: Perfluorocompounds include all molecules that contains carbon and fluorine plus NF₃ and SF₆.

QMS:	Quadruple Mass Spectrometer is an analytical instrument that identifies ions by way of measuring their mass to charge ratio.
RTP:	Rapid Thermal Processing.
RTO:	Rapid Thermal Oxidation.
SACVD:	Sub-Atmospheric CVD.
TEB:	Triethylborate.
TEOS:	(Si(OC ₂ H ₅) ₄), an organic silicon source that can provide the vapor for CVD oxides. Since TEOS is a liquid at room temperature, the vapor is usually delivered by bubbling an inert carrier gas (helium) through the liquid.
TEPO:	Triethylphosphate.
TMS:	Trimethyl silane.
USG:	Undoped Silicate Glass.
VOC:	Volatile Organic Compound.