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Design of Bluetooth frequency synthesizer

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DESIGN OF BLUETOOTH FREQUENCY SYNTHESIZER

A Thesis

Presented to

The Faculty of the Department of Engineering

San Jose State University

In Partial Fulfillment

Of the Requirements for the Degree

Master of Science

By

Shridevi Vijayakumar Jade

August 2005

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ABSTRACT

DESIGN OF BLUETOOTH FREQUENCY SYNTHESIZER

by Shridevi V. Jade

A 2.5V CMOS Bluetooth frequency synthesizer with low phase noise and power is presented. Low power consumption and phase noise is achieved by using a Colpitts oscillator. An accumulation varactor is used with 14% variation synthesizing frequencies from 2.4G Hz to 2.48G Hz. The divider network is designed using dynamic true single-phase logic (TSPC) for low power operation. Verilog-AMS modules are used as a high level simulation and validation model. The Bluetooth frequency synthesizer is designed using 0.25um technology and occupies an active area of 0.3mm X 0.17mm. Power consumption at 2.4G Hz is 8m W. Simulated phase noise varies between -50dBc/Hz to -10dBc/Hz and spurious tones vary between -90dBc/Hz to -7-dBc/Hz at 2.4G Hz.

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Chapter 1

INTRODUCTION

1.1 Motivation

The popularity of wireless technology in the area of communications and growth in very large-scale system integration (VLSI) low cost technology has opened doors for a variety of phase-locked loop (PLL) based complementary metal-oxide semiconductor (CMOS) frequency synthesizers. One of the key elements of the PLL frequency synthesizers is the voltage-controlled oscillator (VCO). The inductor-capacitor (LC) based oscillators are preferred over conventional ring oscillators for monolithic integration of frequency synthesizers used in radio frequency (RF) applications. The Colpitts oscillator achieves important VCO criteria of low phase noise, power dissipation, and a large tuning range. The accumulation mode metal oxide semiconductor (MOS) varactor provides a larger tuning range. True single-phase clock (TSPC) dynamic logic divider circuit, has the advantages of fast operation, low area, and power dissipation.

The synthesizer design and circuit implementation was performed for a Bluetooth frequency synthesizer used in wireless applications, cell phones, personal computers, small hand held devices, etc.

1.2 Purpose

The proposed design generates 2.38G Hz to 2.5G Hz signals wireless applications. It is targeted for Bluetooth transceivers in the industrial, scientific and medical (ISM) radio frequency band of 2.4G Hz to 2.483G Hz.

1.3 Scope

The frequency synthesizer generates 2.38G Hz to 2.5G Hz signals for Bluetooth wireless transceiver applications. The Taiwan semiconductor manufacturing company (TSMC) 0.25u CMOS technology is used. The design goals are low phase noise, small area, and low power consumption. MOS varactors provide a large tuning range. The phase frequency detector (PFD) is dead zone free for improved performance.

The design parameters were initially tested and verified for convergence using Verilog-AMS modules. The schematics and layouts for Colpitts oscillator, MOS varactor, TSPC divider, PFD, charge pump (CP), and low pass filter (LPF) were simulated using Cadence tools. The frequency synthesizer was not fabricated. Phase noise analysis was performed using the Cadence SpectreS simulator, and plotted using MathCAD software.

1.4 Thesis Organization

This thesis presents the design and implementation of a 2.4G Hz frequency synthesizer for Bluetooth transceiver applications. The contents of this document have been organized in a logical sequence. A brief description of the contents of each chapter is given below.

Chapter 2 gives an overview of RF frequency synthesizers. It also defines the terms used with frequency synthesizers. Chapter 3 illustrates the current state of the art, in the area of RF frequency synthesizers. Bluetooth frequency synthesizer is described in detail. Few examples of related products, by various vendors, currently used in wireless

applications are listed. Chapter 4 gives an overview of the 0.25 μ process used for the design and discusses deep sub-micron challenges. Chapter 5 presents the proposed design in detail and illustrates the benefits of the proposed design and its trade-offs. It also discusses how Verilog-AMS modules are used to arrive at the final converging solution. Implementation of the proposed design is described in detail in Chapter 6. Chapter 7 discusses the layout considerations of the proposed design. Chapter 8 describes how parameters are measured and discusses the simulation results in detail. Chapter 9 concludes the thesis with possible further study in this area.

1.5 Summary of Results

A summary of Bluetooth specifications and design performance is presented in Table 1. All aspects of specifications have been met except for the phase noise requirement by this design. The low pass filter and inductor are considered off-chip for this design to be cost effective. To reduce the spurious tones, a third order loop filter is implemented. Good settling time can be achieved by narrow loop bandwidth. This increases the loop filter capacitance and hence the cost of the chip. There is a trade-off between settling time and area.

Parameter	Specification	Measurement
Technology	0.25u m	0.25u m
Supply Voltage	2.5 V	2.5 V
Frequency range	2.4G Hz – 2.48G Hz	2.36G Hz – 2.5G Hz
Frequency Resolution	1M Hz	1M Hz
Tuning range	~3%	~14%
Phase noise	-89 dBc / Hz	-50dBc/Hz to -10dBc/Hz
Spur	-49 dBc / Hz	-90dBc/Hz to -70dBc/Hz
Settling time	< 62.5u S	50u S
Power	< 70m W	8m W
Area	1 mm X 1mm	0.3mm X 0.17mm
Cost	\$2.1 - \$3.0	\$0.2 - \$0.3

Table 1: Summary of Bluetooth Frequency Synthesizer Performance

Chapter 2

OVERVIEW OF FREQUENCY SYNTHESIZERS

2.1 Introduction

In this chapter different frequency synthesizer architectures are discussed. The role of radio frequency (RF) communication frequency synthesizers is highlighted. The general terms and considerations used in RF frequency synthesizers are discussed with an emphasis on critical parameters, such as phase noise, chip area, and power dissipation.

2.2 Synthesizer Architectures

There are many ways to implement frequency synthesizers. The desired frequency synthesizer used for Bluetooth RF communication should be able to generate giga hertz frequencies with low phase noise, low power, and minimum chip area. The frequency synthesizer design architecture is selected based on application. The direct digital frequency synthesizer (DDFS) is used for the applications where fast frequency switching is required. It is suitable for the low frequency applications. It has no off-chip components and hence meets minimum chip area constraints. But the power requirements are very large due to the requirement for a RF frequency DAC and not feasible for 2.4G Hz frequency applications.

PLL based frequency synthesizers are most commonly used. They generate high frequencies with low phase noise and low power requirements meeting two of the main

constraints for RF Frequency synthesizers [1]. Most of the PLL frequency synthesizers use high quality factor (Q-factor) components and these are usually off-chip components due to chip area constraint. PLL frequency synthesizers have narrow loop bandwidth and good tunable frequencies with low phase noise, which makes them popular over other frequency synthesizer architectures.

2.3 Direct Digital Frequency Synthesizers

The direct digital frequency synthesizer consists of a digital phase accumulator, read-only memory (ROM) containing a look-up table, and digital to analog converter (DAC). The digital phase accumulator accumulates phase at every clock cycle until its maximum count is reached. Depending on the accumulated phase, a word is set at the end of every clock cycle. This word is then translated into a corresponding frequency by the look-up table stored in the ROM. This digital word is then fed to the digital to analog converter, which gives the desired output frequency [2]. In this architecture, digital to analog converter consumes very large power and hence DDFS is not used for Bluetooth RF synthesizer applications. The clock is typically three times greater than the output frequency. The block diagram is shown in Figure 1.

Figure 1: Direct Digital Frequency Synthesizer

2.4 PLL Based Frequency Synthesizers

PLL based RF frequency synthesizers consist of a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a voltage controlled oscillator (VCO), and a divider. The feedback loop usually contains a divider. The VCO output is a high frequency analog signal and the phase frequency detector compares low frequency digital signals. The block diagram is given below.

Figure 2: Basic PLL Model

The front-end of the PLL based frequency synthesizer is a phase frequency detector. The PFD compares the reference signal with the divided VCO signal in the feedback loop. Depending on whether the reference is leading or lagging the VCO signal, the PFD outputs an up or down signal. The charge pump consists of two switched current sources. If the reference signal leads the VCO signal, the UP signal turns on the upper current source of the charge pump. This puts charge on the capacitor, which is converted into a voltage and filtered by the low-pass filter. It is then fed to the voltage-controlled

oscillator. If the reference signal lags the VCO signal, the lower current source of the charge pump is turned on. This removes the charge on the capacitor and is converted into voltage. This voltage is filtered by the low-pass filter removing high frequency components, and given as an input to the voltage-controlled oscillator.

The voltage-controlled oscillator usually consists of an inductor and capacitor tank circuit. The capacitor is implemented using a varactor. The input control voltage varies the capacitance of the varactor. The tank circuit generates a high frequency output analog signal corresponding to the input control voltage. This signal is divided in the feed back loop, and converted into a low frequency digital signal to be compared with the reference signal at the input of the phase frequency detector. This mechanism has a loop settling time, and once the loop settles, it can synthesize accurate frequencies.

2.5 Delay Locked Loop Frequency Synthesizers

Delay locked loop (DLL) is a type of PLL where, the voltage controlled oscillator is replaced by a voltage controlled delay line. The voltage controlled delay line has N -delay stages. When the delay line is locked, the output is delayed by a clock cycle. The edge accumulator is used to accumulate edges at the end of every clock cycle. The N -stage delay line delays the reference clock by a multiple of N [3]. It is not recommended for variable frequencies since N -stage delay line fixes the output frequency. The block diagram of a DLL is given in Figure 3.

Figure 3: Delay Locked Loop

2.6 General Terms and Considerations of PLL Frequency Synthesizers

Loop stability is very important for PLL based frequency synthesizers. The PLL must maintain the phase locked state, in order to generate accurate frequencies. To attain a phase locked state, PLL frequency synthesizers depend on phase noise and loop settling time. The other considerations are chip area and PLL power.

2.6.1 Phase Noise

Phase noise is rapid, short-term, random fluctuations in the phase of a frequency synthesizer output, caused by time domain instabilities. The output of the phase locked loop in the locked state is a series of impulse functions, taken at the output of the phase

frequency detector. In reality, it has some random short-term fluctuations known as phase noise. Phase noise appears as short-term skirt shaped tone rather than a sharp impulse. It is shown in Figure 4. In the figure, ω_0 represents the center frequency. Phase noise is measured in dBc. The dBc is defined as,

$$\text{dBc} = 10 * \text{Log} [\text{Power of fluctuation} / \text{Power of the Carrier}]$$

Figure 4: Phase Noise of Frequency Synthesizer

High phase noise is the result of an unstable PLL. High phase noise means, the control voltage signal moves faster and overshoots. If this happens, it is difficult to sustain the locked state. If the phase noise is low, the loop is stable and the PLL can remain in the locked condition.

The importance of phase noise in RF receivers [4] is shown in Figure 5. The noisy signal of the oscillator down converts the RF signal with a strong unwanted signal. Both the signals have overlapping spectra, and due to this, RF signal suffers severely. Hence it is very much desired by RF frequency synthesizers to have low phase noise.

Figure 5: Effect of Phase Noise in RF Receivers

2.6.2 Capture Time or Settling Time

The capture time or the settling time of a PLL is defined as the time taken by the PLL to lock new frequency or changed frequency and be stable again. A lower capture time implies the switching time between channels is lower. This increases efficiency of the radio signal using the frequency synthesizer.

Lower phase noise requires a more stable loop. This increases the capture time or the settling time. Higher phase noise means, the signal moves faster and overshoots, which in turn decreases the settling time. A low-pass filter is used to filter out the high frequency noise. As frequency decreases, the loop becomes slower and stable. In contrast, as frequency increases the loop becomes faster, overshoots, and results in high

frequency noise or phase noise. Hence, in the design of PLL frequency synthesizers, there is always a tradeoff between phase noise, settling time, and loop stability, depending on their application. Slower settling is a problem in fast frequency hopped systems [5]. Figure 6 shows the graph of settling time versus control voltage.

Figure 6: Settling Time of Frequency Synthesizer

2.6.3 Chip Area and Cost

Another important factor the designers consider is the chip area. The chip area is directly proportional to the cost of the final product. Hence, it is highly desirable to keep silicon real estate as low as possible. The low-pass filter is usually designed using static components. Generally, to achieve higher stability, frequency synthesizers require low phase noise. Low phase noise can be achieved if the loop bandwidth is narrow. However, it requires a larger capacitor during the loop filter design. This capacitor takes a larger area during silicon implementation and increases the cost dramatically. Smaller capacitance is required to minimize area and cost.

2.6.4 Power

The main blocks of a PLL frequency synthesizers are phase frequency detector, charge pump with low-pass filter, voltage-controlled oscillator, and divider. Usually, PLL frequency synthesizers follow a mixed-signal design approach. The digital section of a PLL consists of a phase frequency detector and divider. The charge pumps and voltage-controlled oscillators constitute the analog section. The dividers are generally designed using dynamic logic or true single-phase logic (TSPC), which results in zero static power consumption. The phase frequency detectors are implemented using minimal number of gates, which lowers power dissipation. The charge pumps and voltage-controlled oscillators should be designed for low power consumption. The current switches of the charge pump are designed using small currents to achieve low power consumption. Usually inductor-capacitor tuned oscillators are designed to meet the power requirements of the frequency synthesizers.

2.6.5 Spurs

The phase frequency detector and charge pump operate at the reference frequency. The noise from these blocks modulates the control voltage, as the loop filter attenuation is finite. This noise appears at upper and lower sidebands of reference frequency of the oscillator as illustrated in Figure 7.

Figure 7: Spurious Tones at Upper and Lower Sidebands of Reference Frequency

Chapter 3

BLUETOOTH FREQUENCY SYNTHESIZER AND MARKET EXAMPLES

3.1 Introduction

Frequency synthesis is a mechanism, where a phase locked loop is used to generate the desired frequencies. Frequency synthesizers are used for clock synchronization, carrier detection, frequency translation, and in many other communication applications. The growth in wireless communications has opened up a new chapter in the design of frequency synthesizers. This chapter discusses Bluetooth frequency synthesizers in detail, including specifications, and design considerations.

3.2 Bluetooth Wireless Technology

Bluetooth wireless technology has revolutionized the world of wired connections. Bluetooth connects the devices using short-range radio links. Electronic devices such as, cell phones, hand-held portable devices, global positioning systems, medical equipments, computers, and many others can be linked without any wires. Bluetooth technology has simplified the interconnection of common electronic devices in office and home alike. The popularity of the Bluetooth technology is due to its low power, cost, complexity, and robustness.

Bluetooth operates in the 2.4G Hz industrial scientific medicine (ISM) band. It uses 2.4G Hz – 2.4835G Hz frequency range. The lower guard band is 2M Hz and the upper guard band is 3.5M Hz [6]. It uses frequency hopping from 2.402G Hz to 2.48G Hz at 1M Hz intervals resulting in 79 channels. The signal hop rate is 1600 hops/s. The Bluetooth frequency allocation is illustrated in Figure 8. Bluetooth uses Gaussian

Frequency Shift Keying (GFSK) modulation scheme, which makes it robust in noisy environments. Bluetooth systems avoid interference by hopping to a new frequency after transmitting or receiving a packet.

Figure 8: Bluetooth Frequency Allocation of 79M Hz Range

In Figure 8, LGB refers to the 2M Hz lower guard band, UGB refers to the 3.5M Hz upper guard band, and CH1, CH2... CH79 refer to the 79 channels spaced at 1M Hz intervals in the range 2.402G Hz to 2.48G Hz [6].

Bluetooth system operates at two frequency ranges, the most popular being 79M Hz range and the other is 23M Hz range [6]. Both of these ranges use ISM band. Bluetooth with 23MHz range is used in countries like Spain, Japan, and France, where there are limitations over the available frequencies that can be used for communications. They use special frequency hopping algorithms to adhere to their allocated frequencies.

3.3 Bluetooth Design Specifications

Bluetooth frequency synthesizers are designed for low cost and complexity. At the receiving end of a Bluetooth transceiver, the synthesizer is characterized by phase noise, settling time, and spurs.

3.3.1 Phase Noise

Phase noise of frequency synthesizer is the ratio of noise power of phase locked loop and offset frequency. The minimum noise power of radio signals can be as low as -70 dBm [1]. Within the loop bandwidth, the phase frequency detector dominates the phase noise of the PLL closer to the carrier, and voltage-controlled oscillator at the farther end. Outside the loop bandwidth, the noise power is considered to be zero, if the loop filter provides high attenuation to the out of band signals. The phase noise requirement for the Bluetooth frequency synthesizer is -80dBc/Hz [6].

3.3.2 Settling Time

Bluetooth uses frequency hopping to avoid interference and signal fading. In the 79M Hz range Bluetooth system; frequency hop rate is 1600hops/s [6]. Minimum settling time of the loop depends on the time it takes to settle from the first channel to the last channel in the frequency range. Settling time is usually a percentage of 1/hop rate. If it is 10% of the hop rate, then settling time has to be smaller than 62.5us.

3.3.3 Spurs

The loop filter is designed to filter the high frequency noise entering into the voltage-controlled oscillator. The noise from phase frequency detector and charge-pump modulates the control voltage of the voltage-controlled oscillator. This appears at the upper side band and the lower side band of the reference frequency as spurs. These spurious tones have to be minimized, to keep better signal-to-noise ratio. For a Bluetooth frequency synthesizer, spurious tone specification is -49dBc/Hz [6].

The Specifications used for the design of Bluetooth frequency synthesizer are given in Table 2.

Parameters	Specification
Technology	TSMC 0.25um
Frequency range	2.402G Hz - 2.48G Hz
Number of channels	79
Frequency resolution	1M Hz
Hop rate	1600 Hops/S
Phase noise	-89 dBc/Hz
Spurs	-49 dBc
Settling time	62.5u S
Voltage Supply	2.5 V
Power consumption	< 70m W

Table 2: Bluetooth Frequency Synthesizer Design Specifications

3.4 Advantages of Bluetooth Technology

Bluetooth is different from some other technologies since it does not require the devices to be in the line of sight to establish a connection. It supports both voice and data communications. Bluetooth uses 2.4-to 2.48G Hz radio band with spread-spectrum frequency hopping technology. This frequency hopping technique minimizes interference, even if two devices are using same exact frequency, by randomly changing the frequency within its frequency band.

Bluetooth is used to connect the devices within a short range of 30 to 40 foot. Bluetooth enabled devices can also communicate with each other without human intervention. Bluetooth supports simultaneous transmission of voice and data at a rate of 1M bits/s.

3.5 Market Examples

Bluetooth frequency synthesizers are used in various short-range wireless communication applications. Its popularity is due to easy and cost effective integration of Bluetooth chips and Bluetooth silicon capabilities into mobile handsets, personal computers, computer mouse and keyboard devices, personal digital assistants (PDAs), game controllers, automobiles, and industrial equipment.

Industry giants like Nokia, Ericsson, Sony, Samsung, and Motorola have developed Bluetooth enabled cell phones, which are very popular. These phones are being used for e-mail, internet access, mobile commerce, general packet and radio service (GPRS) applications, and sharing digital images.

Wireless application protocol (WAP) over Bluetooth is becoming increasingly popular. Using integrated Bluetooth chips along with WAP services avoids expensive and time-consuming cellular connections. It offers localized and more interactive WAP services. Nokia and Ericsson have developed phones using WAP over Bluetooth. They are being used in airports, cafes, and shopping centers.

Wireless local area networking (LAN) using Bluetooth has revolutionized network connections at office and home environments. Bluetooth enabled wireless LAN cards are being used for providing broadband speeds without wires. Toshiba, Nokia, SMC, and many other companies are also bringing Bluetooth enabled personal computer (PC) wireless LAN cards into the market.

Intensive research is being done by companies like IBM and Intel on, how to construct a network at any place, any time, and with anybody by means of the Bluetooth technology.

3.6 Market Study of Wireless Frequency Synthesizers

The cost of the fabricated chip depends on type of packaging, production volume, and the active area of the chip. The Table 3 gives examples of 2.5G Hz wireless frequency synthesizer chips available in the market and their cost estimation.

Synthesizer Chip	Packaging	Volume	Cost	Area
ADF4212LBCP Analog Devices	LFCSP	100-499	\$2.1	4mm X 4mm
ADF4212LBRU Analog Devices	TSSOP	100-499	\$2.1	6.6 mm X 6.4 mm
TRF3750IPW Texas Instruments	TSSOP	90	\$2.7	4mm X 4mm
TRF3750IRGPR Texas Instruments	QFN	1000	S3	4mm X 4mm

Table 3: Market Examples of 2.5G Hz Wireless Frequency Synthesizers

The types of packages are given as follows.

TSSOP - Thin Shrink Small Outline Package

LFCSP - Lead Frame Chip Scale Package

QFN - Quality Flat Pack No-lead

Chapter 4

0.25 μ m TSMC CMOS TECHNOLOGY

4.1 Introduction

For the design, 0.25 μ m complementary metal oxide semiconductor (CMOS) technology is used. The CMOS technology offers very large scale integration capabilities in a cost effective manner and is ideal for implementing single chip solutions. In analog circuit design, gain and noise characteristics of active devices are very important. Although silicon (Si) bipolar technology offers better performance, its cost is higher than CMOS. Hence, CMOS technology is popular.

4.2 Challenges in the Deep Sub-Micron Technology

In the area of radio frequency (RF) and mixed signal design the main challenges are, low supply voltage, trans-conductance of active devices, flicker noise, substrate coupling, and sub-threshold leakage [7].

4.2.1 Low Supply Voltage

In deep sub-micron, the supply voltage is decreased to avoid junction breakdown. Usually, analog designs require larger swings compared to digital designs. Transistor scaling is done mainly to improve the speed of digital designs. The threshold voltage V_{th} of the transistors is not properly scaled. This limits the usage of cascoded structures, which are used for reducing Miller capacitances and to achieve low impedance effects for

matched current mirrors. Due to low supply voltage, the maximum voltage swing available for logic realization is tremendously reduced.

4.2.2 Trans-conductance (G_m) of Active Devices

The trans-conductance of an active device is the linear approximation of the square law curve. It is defined as the ratio of small change in the drain to source current to the small change in the gate to source voltage of the active devices. The G_m of active devices changes constantly and designs done with G_m are valid over a small range.

4.2.3 Flicker Noise

It is associated with crystal surface defects in semiconductors. Flicker noise is inversely proportional to frequency and hence, also known as $1/f$ noise [8]. Its effects are seen at low frequencies. It is very important while designing RF circuits like oscillators and mixers.

4.2.4 Substrate Coupling

In deep sub-micron technologies, the substrate is highly doped. This reduces insulation between devices and results in degradation of noise characteristics of the active devices.

4.2.5 Sub-threshold Leakage

As we move from one generation to another, the supply voltage is reduced to achieve low power dissipation. This causes lower threshold voltage of the transistor, but increases the sub-threshold current exponentially [9].

4.3 The TSMC 0.25u Process

The 0.25u Taiwan semiconductor manufacturing company (TSMC) process uses five layers of metal and one layer of poly. The supply voltage used in this process is 2.5V. This technology is most popular for today's telecommunication integrated products because of high stability, good performance, and reliability. This is ideal for mixed signal RF applications because of improved spice models, compatibility with CMOS logic, good trans-conductance values, improvement in 1/f noise, and sub-threshold leakage [10]. The substrate noise coupling is reduced by the deep n-well implantation. The n-wells can be used around the n+ regions for isolation with p-regions on the substrate. The metal insulator metal capacitor, also known as MiM, offers a capacitance of $1\text{fF}/\mu\text{m}^2$ [10]. The mixed signal process uses non-epitaxial wafers. Other features of TSMC 0.25u, suitable for mixed signal and RF designs are, high precision poly resistors, good quality varactors, and high quality factor inductors [10]. The detailed data sheet of 0.25u TSMC run T39S is included in Appendix A [11].

Chapter 5

DESIGN

5.1 Introduction

Frequency synthesizer is an important building block in the generation of reference frequencies used for wireless communications. To realize high-speed communication systems, frequency synthesizers would have to generate higher frequencies. This section also describes how the proposed design parameters are first tested and verified using Verilog-AMS software tool to arrive at the converging solution.

5.2 Frequency Synthesizer Architecture

The proposed frequency synthesizer architecture is shown in Figure 9. It consists of a phase frequency detector (PFD), a charge pump with third order loop filter, a voltage controlled oscillator (VCO), and a high-frequency divider.

Figure 9: Frequency Synthesizer Architecture

The VCO has to generate radio frequencies (RF) in the range of 2.4GHz to 2.5GHz. It is implemented using a Colpitts oscillator, which uses an inductor and a capacitor in its resonance tank. Since Colpitts oscillator uses capacitive feedback, there is no phase inversion. The output frequency of the oscillator is controlled by the values of inductor and capacitor. The capacitor part of the resonance tank consists of a metal oxide semiconductor (MOS) varactor, which varies the capacitance proportional to the voltage generated by the charge pump and low-pass filter circuit. The reason for using Colpitts oscillator is, it gives good frequency stability and is easy to tune over a wide range of frequencies. It also has low phase noise, which is highly desirable in RF frequency synthesizers.

The divider network is designed using true single-phase clock (TSPC) dynamic logic. The advantage of using TSPC dynamic logic is, speed and zero power consumption. The divider output is a digital signal, which is applied at the input of the phase frequency detector, for comparison with the reference frequency.

The phase frequency detector (PFD) is designed using two D flip-flops and an NAND gate. The output of a phase frequency detector is the frequency and phase difference between the reference signal and the divided oscillator signal. The PFD works with a charge pump. The phase PFD determines whether the oscillator output is lagging or leading the input reference.

The charge pump is designed using two current sources. If the oscillator output is lagging the input reference, the charge pump activates the top current source, which deposits the charge on the capacitor. This phenomenon is known as charge pump-up. If

the oscillator output is ahead, lower current source of the charge pump is activated. This discharges the capacitor, which is known as charge pump-down. The charge pump basically acts as a current switch.

Low-pass filter (LPF) follows the charge pump. LPF is used to remove unwanted high frequency noise from the output voltage of the charge pump. This voltage is then applied as a control voltage to the oscillator. Control voltage is also known as tune-in voltage. Tune-in voltage or control voltage is proportional to the phase/frequency difference between two input signals entering the phase frequency detector. When the tune-in voltage settles, it reduces the phase/frequency difference between the two input signals. The output frequency of the oscillator is pulled towards the frequency of the reference. The phase change between the two signals contributes to the frequency difference. When the tune-in voltage reaches a steady state, it is proportional to the phase difference between the two signals and it remains constant. Since the phase difference is constant, when the loop is locked, the oscillator frequency is exactly equal to the reference frequency. Different reference frequencies at the input of phase frequency detector produce corresponding tune-in voltages. Hence the loop gets locked at different frequencies as defined by the tune-in range of the VCO.

5.3 Colpitts Oscillator Architecture

The main design considerations of a high frequency RF oscillator are, low power dissipation, phase noise, good stability, and higher tuning range. The advantages of Colpitts oscillator are, good frequency stability, ease of tuning, low phase noise, low power consumption, and usage over wide range of frequencies [12]. The large value of

split capacitance is in parallel with the junctions and minimizes effect on frequency stability. Hence, Colpitts oscillator is an ideal choice for the Bluetooth frequency synthesizer. The basic architecture of the Colpitts oscillator is depicted in Figure 10.

Figure 10: Basic Architecture of Colpitts Oscillator

The tank circuit of Colpitts oscillator consists of transistor M1, inductor L, capacitors C1, C2, Cvar, and load resistance RL. Here, Cvar is the varactor part of the tank circuit. The capacitances, C1 and C2 are in parallel with Cvar and form a capacitive voltage divider. The voltage drop across RL is reduced by the capacitive voltage divider. The total capacitance C is computed as, $C = \left[\frac{C_1 \cdot C_2}{C_1 + C_2} \right] + C_{var}$. The capacitive divider ratio is given by $N = C_1 / (C_1 + C_2)$. The oscillation frequency is given by $f = 1 / [(2 \cdot \pi) (\text{Sqrt}(L \cdot C))]$. The capacitive divider formed by C1 and C2 reduces

load on the tank circuit. The capacitive divider ratio N can be set to achieve optimal noise performance. Best noise performance can be obtained with the N value of $(1/5)$ [18].

The parameters used to design the basic Colpitts oscillator are given in Table 4.

Resistor values in Ohms							
R1	18.6 K	R2	15 K	R3	200	RL	20 K
Capacitor values in Farads							
C1	3.85 p	C2	150 p	C3	10 u		
Transistor Values in um							
(W/L) M1	40 / 0.3	(W/L) M2	15 / 15	(W/L) M3	15 / 15		
Inductor Value in Henry							
L	1n						

Table 4: Parameters of Basic Colpitts Oscillator

5.4 Advantages of the Architecture

The designed architecture is an example of mixed-signal phase locked loop (PLL), which involves both analog and digital components. Digital PLLs are not tightly coupled to the underlying fabrication technology. The absence of off-chip components makes them highly cost effective. In reality, digital PLLs require tens of thousands of gates and exhibit poor locking times. Although the architecture is process dependent and uses off-chip components such as inductor and capacitor, it exhibits good locking times and low phase noise.

The architecture uses a charge pump implemented using two switched current sources. The charge pump is designed using cascode current mirrors. Cascode style provides high output impedance, which is highly desirable for current mirrors to keep a constant current. It uses small number of transistors and allows the synthesis of desired loop filter with less complexity, low power consumption, and smaller area [13].

The architecture uses a third order loop filter consisting of static components. To achieve efficient area criterion, capacitors must be as small as possible. By making the charge-pump current low, lower capacitance can be achieved. However, a very low capacitance increases the phase noise. So, in the design, there is a trade-off between noise and area [14].

Colpitts oscillator is used to generate desired frequencies; since it is single ended and can achieve negative resistance with only one transistor. Therefore, it is simple to design compared to other negative resistance oscillators. Colpitts oscillator exhibits low phase noise and low power consumption, both critical to the RF frequency synthesizers.

The divider circuit uses TSPC dynamic logic. These dividers are reasonably fast, compact in size, and have no static power dissipation. The dynamic TSPC circuit achieves higher clock frequencies, by simplifying the clock distribution and eliminating phase overlapping problems [15].

5.5 Disadvantages of the Architecture

The main disadvantage of this architecture is its use of an LC oscillator. It uses many off-chip components and is not area efficient. The layout of the inductor is process dependent and even minor inaccuracies may result in different synthesized frequencies.

5.6 Verilog-AMS Simulation Model of the Design

The design is first tested using Verilog-AMS software tool, to know the best possible converging solution of PLL. Then the circuit implementation is done using TSMC 0.25u process. The parameters of the proposed design are summarized in Table 5.

Parameters	Specification
Frequency range	2.402G Hz - 2.48G Hz
Number of channels	79
Frequency resolution	1M Hz
Settling time	62.5u S
Voltage supply	2.5 V
Charge pump current	100u A
Kvco - Oscillator sensitivity	55M Hz / V
Kpfd – PFD sensitivity	15.92u A / Radians
Klpf – Loop filter sensitivity	1
Loop bandwidth	5M Hz

Table 5: Parameters of the Design

The integrated schematic of Verilog-AMS PLL is shown in Figure 11 below.

Figure 11: Schematics of Verilog-AMS PLL

The Verilog-AMS routines are written for phase frequency detector, charge pump, oscillator, and divider. These routines use the parameters given in Table 5. Each module is tested for the whole range of frequency synthesizer. Using Verilog-AMS routines final solution of frequency synthesizer is achieved for the entire range of frequency synthesizer. These modules test and verify the correct parameters that could be used for circuit implementation. All the routines used to arrive at the converging solution of Bluetooth frequency synthesizer are given in Appendix B.

Figure 12 shows the variation of control voltage for Verilog-AMS module of PLL and the PLL is in unlocked state. Figure 13 shows the variation of control voltage and its stabilization near the locking state. Figure 14 shows the stabilized control voltage for the locked PLL.

Figure 12: Verilog-AMS PLL in Unlocked State

Figure 13: Verilog-AMS PLL Approaching Locking State

Figure 14: Verilog-AMS PLL in Locked State

From the Verilog-AMS simulation of PLL, it is verified that the parameters used for the Bluetooth frequency synthesizers can achieve lock over the entire desired range of frequencies. From Figure 14, it gives a lock time of 13.5u S. While implementing the Bluetooth frequency synthesizer by TSMC 0.25u process, the lock time of PLL could be different, as it uses different capacitance model.

Chapter 6

CIRCUIT IMPLEMENTATION

6.1 Introduction

The design is implemented using Taiwan semiconductor manufacturing company (TSMC) 0.25u technology. The specification of Bluetooth frequency synthesizer is discussed in chapter 3. In this chapter, design and implementation of dead-zone free phase frequency detector (PFD), charge-pump, low-pass filter (LPF), Colpitts oscillator, and true single-phase clock (TSPC) divider are discussed in detail.

6.2 Phase Frequency Detector Design

Phase-frequency detectors are used to determine frequency differences, when the loop is unlocked and determine phase differences, when the loop is locked. The common problem with phase-frequency detectors is its dead-zone. It occurs when both input signals of phase-frequency detector are in phase and both edges occur simultaneously. Then, one of the outputs is an infinitely thin pulse. As the digital circuits have finite rise and fall times, gain of the phase-frequency detector will be in the undesirable, nonlinear low-gain region [16]. To avoid this dead-zone problem, the phase frequency detector is designed, using two edge-triggered D-flip flops and a NAND gate. When both the signals are turned on simultaneously, to avoid the dead-zone problem, the delay gates reset the flip-flops [13]. The gate level schematic of phase-frequency detector implementation is shown in Figure 15.

Figure 15: Dead-zone Free Phase Frequency Detector

When the loop is in phase-locked state, pulse width of the D-flip flop should be about 1.65ns. In this way, the up and down signals, are long enough to reach a valid logic level and turn on the switches in the charge-pump. A large pulse width introduces jitter. Jitter is a result of unmatched up and down currents of the charge-pump.

Simulation results of PFD are shown in the Figure 16.

Figure 16: Phase Frequency Detector Output Without a Dead-zone

The phase frequency detector operates by comparing the two input signals, the oscillator feedback signal and the reference signal. The output of PFD is either an up or a down pulse, depending on the input signals. The output is an up pulse, if the oscillator signal is lagging the input reference signal and a down pulse, if the oscillator signal leads the reference signal. The simulation results for these two instances are illustrated in Figure 17 and 18 respectively.

Figure 17: Oscillator Signal Lags Input Reference Signal

Figure 18: Oscillator Signal Leads Input Reference Signal

The edge-triggered D-flip flop is designed using NAND gates. The schematic of the D-flip flop is shown in Figure 19.

Figure 19: Edge Triggered D-Flip Flop

The schematics of the NAND cell, used to implement the edge triggered D-flip flop is shown in Figure 20.

Figure 20: Schematics of NAND Gate Used in D-Flip Flop

6.3 Charge Pump Design

Charge-pumps are used in conjunction with the phase-frequency detector. It converts up or down pulses of a phase-frequency detector output into current, which is proportional to the phase difference. The charge-pump consists of two switched current sources, which pump charge into or out of the loop filter, depending on logical outputs of the phase-frequency detector [14]. The schematics of the charge-pump, along with second order loop filter are shown in the Figure 21.

Figure 21: Charge-pump Schematics

The charge pump in Figure 21 is a tri-state charge pump. The “UP” or “DN” signals of the phase-frequency detector control current sources of the charge-pump. The net current delivered to the loop filter is proportional to the difference between the pulse widths. In Figure 21, the transistors P1 and P2 form the upper current source and transistors M1, M2, and M3 form the lower current source. The current source is designed to be a cascode, using transistors M4 and M5. The cascode style offers high output impedance, which helps to maintain a constant current through the current sources. Transistors P3 and M6 are used as up and down current switches respectively. The parameters used in the design of charge pump are summarized in Table 6.

Transistor Values in μm					
(W/L) M1	8.85 / 1.2	(W/L) M2	8.85 / 1.2	(W/L) M3	8.85 / 1.2
(W/L) M4	8.85 / 1.2	(W/L) M5	8.85 / 1.2	(W/L) M6	20 / 0.3
(W/L) P1	21 / 0.6	(W/L) P2	21 / 0.6	(W/L) P3	50 / 0.3
Low Pass Filter Values					
R1 in Ohms	12 K	C1 in Farads	3.6 p	C2 in Farads	36 p
R2 in Ohms	20 K	C3 in Farads	2.7 p		

Table 6: Parameters of Charge Pump

The test-bench used to test the phase-frequency detector and the charge-pump is shown in the Figure 22.

Figure 22: Phase-Frequency Detector and Charge-pump Test-bench

The charge-pump can be in one of the three following states, depending on the output of the phase-frequency detector.

- a. When UP is high and DN is high

This means both the UP and DN current sources are off and there is ideally no leakage current. The output of the loop filter is a constant voltage, called control voltage. The simulated output is shown in the Figure 23.

Figure 23: Both UP and DN Switches are OFF

- b. When UP is high and DN is low

This implies the UP switch is on and the charge-pump charges capacitor C1. This indicates the reference signal leads the oscillator signal and the control voltage increases steadily. The simulated output is shown in the Figure 24.

Figure 24: Reference Signal Leads Oscillator Signal

- c. When UP is low and DN is high

This means the DN switch is on and the charge-pump discharges through capacitor C1. This indicates the reference signal lags the oscillator signal and the control voltage would steadily decrease. The simulated output is shown in Figure 25.

Figure 25: Reference Signal Lags Oscillator Signal

The performance of charge pumps is limited by the mismatch between two current sources and leakage currents [17]. The current mismatch can occur due to non-ideal current mirrors, or varying output voltages along with finite output resistance. Usually, third order filters are used to remove high-frequency current spikes.

The charge pump is balanced at 100uA. The currents from up and down current sources under the balanced condition are shown in Figure 26.

Figure 26: Balanced Charge Pump Currents at 100uA

6.4 Low-pass Filter Design

The filtered output of the charge-pump is known as the control voltage. This voltage is fed to the VCO. The control voltage determines the frequency generated by the VCO. Output of the PFD, UP or DN, consists of direct current (DC) component and undesirable high frequency components. The control voltage must remain constant for the loop to achieve a locked state. Hence, high frequency components from the output of the charge-pump must be filtered out. A low-pass filter is used to remove the high frequency components of the control voltage. The third order loop-filter is shown in the Figure 27.

Figure 27: Third Order Low-pass Filter

Third order low-pass filter contains three poles and two zeros. When both the poles are at origin, the system becomes unstable because, the poles at the origin form two integrators and the system oscillates at the gain cross over frequency. In order to stabilize the system, phase shift must be less than 180 degrees at the gain cross over frequency. This is accomplished by adding a resistor R2 in series with capacitor C2. The components R2 and C2 represent the core of the filter. The added pole C3 and low pass network R1, C1 provides higher order attenuation. Whenever current is injected into the charge-pump, the output control voltage experiences a large jump. This leads to current mismatch in the locked state and the oscillator output signal is disturbed. The additional pole, C3 is added in parallel with R1 and C1 in order to overcome high-frequency jumps or spikes and provides good spurious tone filtering.

Third order loop filter provides good stability and filters the high-frequency noise, which is also known as phase noise. Always, there is a trade-off between loop stability, settling time, and phase noise. Lower phase noise results in a more stable the loop, but increases settling time. Higher phase noise means, the signal moves faster and overshoots, but lowers settling time. By using efficiently designed low-pass filter, high frequency components can be removed and as the frequency decreases, the loop becomes slower and stable.

Bandwidth of a low-pass filter is known as the loop bandwidth. It is the frequency range that can be passed through a low-pass filter. This is an important factor in the loop stability design. The 3-dB bandwidth of the PLL is shown in Figure 28 below. It is measured to be 4.89M Hz.

Figure 28: 3-dB Bandwidth of Low-pass Filter

6.5 Colpitts Oscillator Design

A high frequency RF synthesizer should generate a reference, which is stable, has low phase noise, has wide tuning range, and has accurate frequency [18]. Colpitts oscillators can provide such a reference. The schematic of Colpitts oscillator is shown in Figure 29. Colpitts oscillator is designed for low power dissipation, low phase noise, and accurate frequency. Colpitts oscillator is also known as voltage-controlled oscillator because; the voltage output from the charge pump controls the output frequency of the oscillator.

Figure 29: Colpitts Oscillator Schematics

Figure 29 shows common-source configuration of the Colpitts oscillator. Regenerative feedback is obtained from the tank circuit. The tank circuit consists of transistor M1, inductor L, Capacitors C1, C2, and MOS varactor formed by transistors

M9 and M10. The voltage developed across capacitor C2 is the feedback voltage. In common-source configuration, there is no phase difference between signals at drain and source of transistor M1. Hence, there is no need for phase inversion. The MOS varactor Cvar is in parallel with C1 and C2.

In the common-source configuration of Colpitts oscillator, when the source of transistor M1 becomes negative, the drain of M1 also turns negative. Capacitor C2 charges negatively at the junction of C1 and C2. This makes transistor M1 reverse biased. This negative charging of C2 continues and the reverse bias across M1 increases until the drain of M1 is unable to charge negatively. Now, the inductor L acts as a source and collapses the electric field. The tank potential reverses and the capacitors C1 and C2 begin to discharge. This decreases the reverse bias across M1 and the drain voltage of M1 swings in the positive direction. Capacitors C1 and C2 continue to discharge and then charge in the positive direction. This positive voltage across C2 is fed back to the source of M1 as a re-generative feedback. This continues until the field around inductor L collapses. Then, capacitors C1 and C2 begin to discharge and the cycle repeats. This generates the desired sinusoidal signal at the drain of transistor M1.

The control voltage of the charge-pump and the low-pass filter output, determines the exact frequency. The total capacitance C is given by, $C = [(C1 * C2) / (C1 + C2)] + Cvar$. The frequency of the oscillation is given by $f = 1 / [(2 * \pi) (\text{Sqrt}(L * C))]$.

P and N diodes formed by transistors, P3 and M6 in Figure 29; act as resistors and bias the Colpitts oscillator M1 at 1.8V. These back-to-back diodes are used as level

shifters. The P-diode provides one V_{gs} drop and operates in the deep triode region to bias the Colpitts oscillator.

The primary current of 29.3 μ A is designed using transistors M2 and M3, and is mirrored accordingly in the entire circuit, as depicted in Figure 29. The current source is designed to be cascode by using transistors M4 and M5. The cascode configuration provides high output impedance, which is desirable to keep the current through the current mirror constant. This constant current is mirrored in relative multiples by transistors M7, M8, M11, M12, M13, P1, and P2.

The capacitors C5, C6, C3, and C7 act as bypass capacitors and are used to prevent noise from entering the circuit through the power line. Output of the Colpitts oscillator is a sinusoidal waveform, which is a pure analog signal. Output of the oscillator is fed to the high frequency divider. The frequency divider requires digital input. Hence, the analog signal must be converted into a digital signal.

The common-source amplifier is designed at the output of the oscillator with a high gain. This is done, so that the amplified voltage can trip the inverter chain to convert the analog signal into a digital signal. In Figure 29, transistor M14 denotes the common source amplifier.

The isolation of DC current is done using capacitor C4 and resistor R4 at the input of the common source amplifier. The combination of R4 and C4 forms a high-pass network, which blocks DC, but allows AC to pass through it. The common source amplifier is biased by resistors R3 and R4, which are also part of the high-pass network. The cascode style current source designed using transistors P4 and P5 acts as an active

load to the common source amplifier and also provides high output resistance. This cascode current source also biases the common source amplifier along with resistors R3 and R4.

The output of the common source amplifier is fed to the inverter chain. In Figure 29, the inverters are shown by transistors P6, M15 and P7, M16. These inverters are designed at mid-point voltage, V_M . The inverter chain is designed such that, the V_{trip} is sufficient to keep the common source amplifier in saturation. Transistors P4 and P5 form an active load to the common source amplifier and keeps it in saturation. When both the conditions are satisfied, the AC signal coming into the common source amplifier trips the inverters and consequently, the sinusoidal signal is converted into a digital signal. The output of the Colpitts oscillator is shown in Figure 30, when the input control voltage is set at 1.47V.

Figure 30: Output Waveform of Colpitts Oscillator

The parameters used to design the Colpitts oscillator are summarized in Table 7.

Transistor Values in μm					
(W/L) M1	3.975/0.3	(W/L) M2	9.975/0.975	(W/L) M3	9.975/0.975
(W/L) M4	9.975/0.975	(W/L) M5	9.975/0.975	(W/L) M6	9.975/0.975
(W/L) M7	9.975/0.975	(W/L) M8	10.05/1.5	(W/L) M9	15/15
(W/L) M10	15/15	(W/L) M11	9.975/0.975	(W/L) M12	9.975/0.975
(W/L) M13	9.975/0.975	(W/L) M14	3.975/0.3	(W/L) M15	1.8/0.3
(W/L) M16	2.025				
(W/L) P1	30/0.975	(W/L) P2	30/0.975	(W/L) P3	30/0.975
(W/L) P4	3/0.3	(W/L) P5	3/0.3	(W/L) P6	2.4/0.3
(W/L) P7	3.97/0.3				
Inductor Value in Henry					
L	1n				
Capacitor values in Farads					
C1	4 p	C2	22 p	C3	4 p
C4	200 f	C5	10 u	C6	1 u
C7	1 u				
Resistor values in Ohms					
R1	40 K	R2	40 K	R3	20 K
R4	20 K				

Table 7: Parameters of Colpitts Oscillator

The gain of an oscillator is represented by $[(f_{\max} - f_{\min}) / (v_{\max} - v_{\min})]$. It is measured in MHz/V where, $f_{\max}$ and $f_{\min}$ are the maximum and minimum frequencies of the oscillator. Voltage $v_{\max}$ is the maximum control voltage input required to generate $f_{\max}$, and $v_{\min}$ is the minimum control voltage required to generate $f_{\min}$. K_{vco} denotes the gain of the oscillator. The plot of K_{vco} is given in the Figure 31.

Figure 31: K_{vco} Plot of Colpitts Oscillator

The phase and frequency changes, as the control voltage varies is depicted in Figure 32.

Figure 32: Phase and Frequency Variation of Colpitts Oscillator

From the Kvco plot of Colpitts oscillator designed for Bluetooth application, the voltage and frequency readings are noted as follows. When $v_{min} = 0.45V$, $f_{min} = 2.4G$ Hz and when $v_{max} = 1.86V$, $f_{max} = 2.48G$ Hz. The Kvco is defined as, $[(f_{max}-f_{min}) / (v_{max}-v_{min})]$. The Kvco is 56M Hz/V for this implementation of the Colpitts oscillator.

The accumulation mode varactor is designed using two NMOS transistors with their drains and sources shorted, as shown in Figure 33. One of the gates is grounded and the other is connected to the re-generative feedback path of Colpitts oscillator. In the accumulation mode varactor, as the control voltage increases, the output frequency of the oscillator increases and consequently decreases the varactor capacitance [19]. The total capacitance C is given by, $C = [(C1 * C2) / (C1 + C2)] + Cvar$.

Since the required frequency range is from 2.4G Hz to 2.48G Hz, the capacitor has to be varied from 4.118p F to 4.39p F. The accumulation mode varactor actually varies from 4.08p F for 2.5G Hz at 2.5V to 4.47p F for 2.389G Hz at 0.1V. Hence, actual variation of varactor is from 4.08p F to 4.47p F. This varactor provides 14% variation. The test-bench used to plot capacitance versus frequency is shown in Figure 34.

Figure 34: Test-bench of the Varactor

The varactor capacitance variation with respect to frequency is shown in Figure 35.

Figure 35: Capacitance Vs. Frequency Plot of Varactor

The varactor capacitance variation with respect to control voltage is shown in Figure 36.

Figure 36: Varactor Capacitance Vs. Control Voltage

6.7 Frequency Divider Design

The output frequency of Colpitts oscillator is in the range, 2.4G Hz to 2.5G Hz. The PFD can compare signals in the mega Hz range. Hence, the VCO output has to be divided before giving it as input to the PFD. The divider is designed using dynamic TSPC logic. Pulse skipper is the first stage of the divider. It operates only once at a high frequency of 2.4G Hz. Pulse skipper skips every other pulse from the VCO output. A chain of TSPC divide-by-two circuits follows the pulse skipper.

Divide-by-128 is a circuit used in fixed frequency synthesizers. Frequency divider is made variable by using a Verilog-AMS module. Divide-by-80 in the feedback loop provides eighty channels used by Bluetooth, each between 1M Hz interval.

Divider is one of the main sources of phase noise. To achieve better phase noise performance, it is desirable to reduce rise and fall times. Low rise and fall times increases the transistor size dramatically. Therefore, as a compromise, the rise and fall times are set at 10% of the output period.

6.7.1 TSPC Pulse Skipper Design

The pulse skipper is designed using TSPC D-flip flop. The output Q\ of the D-flip flop is fed as an input. It skips every other pulse from VCO output. The pulse skipper output is a full swing signal and its frequency is relaxed to 1.2G Hz. The TSPC pulse skipper is shown in Figure 37. A chain of divide-by-two circuits also designed using TSPC dynamic logic follows it. TSPC logic can construct D-flip flops using only nine transistors. Reduced parasitic capacitance enhances the high-speed and low-power operation of the divider. The TSPC divide-by-two circuit is shown in Figure 38.

Figure 37: TSPC Pulse Skipper

The parameters used to design the TSPC pulse skipper are given in Table 8.

Transistor Values in um					
(W/L) P1A	1.8 / 0.3	(W/L) P1B	1.8 / 0.3	(W/L) P2	2.1 / 0.3
(W/L) P3	2.25 / 0.3	(W/L) P4	2.25 / 0.3		
(W/L) M1	0.6 / 0.3	(W/L) M2A	3.375 / 0.3	(W/L) M2B	3.375 / 0.3
(W/L) M3A	0.45 / 0.3	(W/L) M3B	0.45 / 0.3	(W/L) M4	0.9 / 0.3

Table 8: Parameters of TSPC Pulse Skipper

The output of VCO has a voltage of 1.9V peak-to-peak and a frequency of 2.4G Hz. The operation of D-flip flop is described below.

- a. When $Q=0$ and $D=1$

When clock becomes low, the node Out1 in Figure 37 becomes low and Out2 becomes high. The output Q remains unchanged. When the clock becomes high, the node Out1 remains low, and Out2 high. The output Q becomes high.

- b. When $Q=1$ and $D=0$

When the clock becomes low, the node Out1 in Figure 37 becomes high and Out2 becomes high. This makes the output Q remain unchanged. When the clock becomes high, the node Out1 remains high, and Out2 becomes low. The output Q becomes low.

6.7.2 TSPC Divide-by-two Circuit Design

Figure 38: TSPC Divide-by-two Circuit

The parameters used to design the TSPC divide-by-two are given in Table 9.

Transistor Values in μm					
(W/L) P1A	1.8 / 0.3	(W/L) P1B	1.8 / 0.3	(W/L) P2	2.1 / 0.3
(W/L) P3	2.25 / 0.3				
(W/L) M1	0.75 / 0.3	(W/L) M2A	0.975 / 0.3	(W/L) M2B	0.975 / 0.3
(W/L) M3A	0.975 / 0.3	(W/L) M3B	0.975 / 0.3		

Table 9: Parameters of TSPC Divide-by-two

The input of divide-by-two circuit has full swing amplitude and the frequency is relaxed in half by the pulse skipper. TSPC dynamic logic has two modes, precharge and evaluate. During precharge phase, the node1 is precharged depending on the input signal and node2 is precharged to Vdd. The transistors P3 and M3B are off. In the evaluation phase, if node1 is precharged to Vdd, the node2 is discharged, and the transistor P3 pulls up node3. If node1 is precharged to zero, the node2 is not discharged, and transistors M3A and M3B pull down node3. The TSPC D-flip flop are designed with rise and fall times of 10% of the output period. A chain of divide-by-two circuits is cascaded to get the desired output frequency. The test bench used for TSPC skipper and TSPC divide-by-two is shown in Figure 39. The simulation results of TSPC skip and divide-by-two circuits are shown in Figure 40.

Figure 39: Test Bench for TSPC Skipper and TSPC Divide-by-Two Circuit

Figure 40: Simulation Results of TSPC Skip and TSPC Divide-by-Two Circuit

The test bench used to divide the Colpitts oscillator output by the TSPC divider is shown in Figure 41. The TSPC divider consists of TSPC pulse skipper followed by six stages of TSPC divide-by-two circuits, to achieve division ratio of 128 in the feed back loop of PLL. The simulation results are shown in Figure 42.

Figure 41: Test Bench for Colpitts Oscillator and TSPC Divide-by-128 Circuit

Figure 42: Simulation Results of Colpitts Oscillator and TSPC Divide-by-128 Circuit

6.8 Phase Locked Loop Integration

The implemented Bluetooth frequency synthesizer has a dead zone free phase frequency detector, cascode charge pump with third order low pass filter, Colpitts oscillator, and TSPC divide-by-128 circuits. The integration of all these modules is shown in Figure 43.

Figure 43: PLL Integration

The reference frequency range required to generate frequencies between 2.4G Hz to 2.48GHz is 18.75MHz to 19.38MHz. The cascode charge pump is designed for 100uA. The settling time of the loop is measured to be 50us. The plot of control voltage under locked condition is shown in Figure 44.

Figure 44: Plot of Control Voltage under Locked Condition

The up and down signals of the PFD are impulses, when the divided oscillator frequency equals the reference frequency under locked condition. These waveforms are shown in Figure 45.

Figure 45: Output Waveforms of Frequency Synthesizer under Locked Condition

Chapter 7

LAYOUT CONSIDERATIONS

7.1 Introduction

The design of a Bluetooth frequency synthesizer is an example of analog and mixed signal circuit. Special considerations have to be made during layout, as it includes analog components. The Colpitts oscillator and charge pump (CP) form the analog components, while phase frequency detector (PFD) and true single-phase (TSPC) dividers form the digital components of the frequency synthesizer. For the layout of the design, 0.25um technology with single poly is used. It is cost effective to consider the passive loop filter elements and the inductor to be off-chip.

7.2 Layout of Phase Frequency Detector

The PFD of the design uses two edge triggered D-flip flops and a NAND gate. The edge triggered D-flip flop is designed using three input NAND gates. The layouts of three input NAND gate, D-flip flop, and PFD are shown in Figure 46, 47, and 48 respectively. The space between NMOS and PMOS are selected to be adequate to make the internal connections of the PFD gates. The completed layout of PFD is enclosed in a guard ring for noise isolation. The area of the PFD is 0.173mm X 0.034mm.

Figure 46: Layout of Three Input NAND Gate

Figure 47: Layout of D-Flip Flop

Figure 48: Layout of Phase Frequency Detector

7.3 Layout of TSPC Divider

The TSPC divider consists of a pulse skipper followed by six divide-by-two circuits. The layouts of TSPC pulse skipper, TSPC divide-by-two circuits, and complete TSPC divide-by-128 are shown in Figure 49, 50, and 51 respectively. The area taken by the divider network is 0.118mm X 0.038mm.

Figure 49: Layout of TSPC Pulse Skipper

Figure 50: Layout of TSPC Divide-by-two Circuit

Figure 51: Layout of TSPC Divide-by-128 Circuit

7.4 Layout of Charge pump

The design has cascode charge pump. It uses 30K ohms of resistor and it is a thin film resistor. The layout of the charge pump is shown in Figure 52. The area of the charge pump is 0.112mm X 0.046mm. The resistor and the entire charge pump layouts are placed within guard rings for noise isolation.

Figure 52: Layout of Charge Pump

7.5 Layout of Varactor

The varactor is very sensitive to adjacent noise. To overcome noise, it is placed in a guard ring. The layout of varactor is shown in Figure 53.

Figure 53: Layout of Varactor

7.6 Layout of Colpitts Oscillator

The Colpitts layout has passive elements like capacitors and resistors, which results in larger area requirements compared to other segments of the design. These passive elements are placed in the guard rings for noise isolation. The inductor is considered to be off-chip because of area constraint and its cost effectiveness. The capacitors used in the layout are metal-insulator-metal (MIM) capacitors and resistors are of the thin film type. The layout of the Colpitts oscillator is shown in Figure 54. The area of the Colpitts oscillator is 0.24mm X 0.14mm.

Figure 54: Layout of the Colpitts Oscillator

7.7 Layout of Resistors

The resistors are diffusion resistors. They use a thin metal layer with a given resistivity to form a resistor. Advantages are high precision, low sensitivity to voltage variations and the ability to handle high currents. The resistance is calculated using the equation,

$R = r * (L / W)$; where r , is known as the resistivity given in Ohms/square, W is the width in μm , and L is the length in μm . The value of resistivity is dependent on the process.

The layout of 40K resistor is shown in Figure 55.

Figure 55: Layout of 40K Ohms Resistor

7.8 Layout of Capacitors

The capacitors can be layed out as MIM capacitors or as diode capacitors. MIM capacitors are used in the design, as they have high quality factor (Q) required for radio frequency design and low sensitivity to process variations. In MIM capacitors, a thin dielectric layer is placed between two metals. The capacitance is calculated using

the equation, $C = C_{sd} * (W*L) + C_p * 2 * (W+L)$

Where C, is the total capacitance in f Farads.

C_{sd} is the source-drain parameter dependent on the process and C_p is the perimeter parameter dependent on the process.

The layout of 100fF capacitor designed using metal1 and metal2 is shown in Figure 56.

Figure 56: Layout of 100fF MIM Capacitor

7.9 Layout of Bluetooth Frequency Synthesizer

The Bluetooth frequency synthesizer is an example of mixed signal. The analog components are very sensitive to noise. The noise also enters from power and ground lines. To avoid this noise from entering into the circuit, guard rings are used. Guard

rings short the energy. They also have high resistance. To lower the resistance, lot of metal contacts are put around it.

The complete layout of frequency synthesizer is shown in Figure 57. The total area measured is 0.3mm X 0.17mm.

Figure 57: Layout of Bluetooth Frequency Synthesizer

Chapter 8

SIMULATION RESULTS AND PARAMETER MEASUREMENTS

8.1 Introduction

The design uses 0.25 μ m technology. A Colpitts oscillator is used for low phase noise and power. The inductor and loop filter are considered to be off-chip components.

8.2 Phase Noise Measurement

Phase noise of the architecture is measured using Mathcad. The simulation is run until the loop settles and becomes stable. The transient response of Colpitts oscillator output is windowed in the desired time interval. The data is collected and processed using MathCAD. The raw data points plotted using MathCAD and the phase noise plots are shown in Figure 58 and 59 respectively. The transient response data points under locked condition are collected between 60 μ s to 65 μ s with a step size of 50ps.

Figure 58: Raw Data Used to Plot the Phase Noise

The plot of phase noise is shown in Figure 23. From the graph, it is found that phase noise actually varies from -50dBc/Hz to -10dBc/Hz . The spurious tones are

between -90dBc/Hz to -70dBc/Hz . This could be due to, the windowing of the data points might be incorrect or due to the fact that the data points are collected up to 5-digit precision and 50p s step size requires higher precision to be used.

Figure 59: Phase Noise Plot of the Design

The phase noise specification of Bluetooth frequency synthesizer is -89 dBc/Hz . The spurious tone specification is -49 dBc/ Hz . The phase noise of the Bluetooth frequency synthesizer is between -50dBc/Hz to -10DBc/Hz . This is because the software failed to generate accurate time stamps needed for plotting the phase noise. The noise emanating from the divider chain degrades the phase noise performance. There is a design trade-off between phase noise and settling time. Higher the settling time, slower and more stable the loop is. If the settling time is lower, the loop is faster; the signal overshoots, and results into high phase noise. Table 10 summarizes the phase noise performance of the design.

Parameter	Measurement
Phase noise	-50dBc/Hz to -10dBc/Hz
Spurious tone	-90dBc/Hz to -70dBc/Hz

Table 10: Phase Noise Measurement of Design

8.3 Power

The power requirement of Bluetooth frequency synthesizer is to be less than 70mW. The design has only 8mW of power consumption. Table 11 summarizes the power consumption of every element of Bluetooth frequency synthesizer.

Parameter	Measurement
Colpitts oscillator	5.153m W
Charge pump	0.21m W
Phase frequency detector	0.5m W
TSPC pulse skipper	0.4m W
TSPC divide-by-two	0.3m W
TSPC divide-by-128	2.2m W
Bluetooth Frequency synthesizer	8.063m W

Table 11: Power Consumption of Bluetooth Frequency Synthesizer

8.4 Settling Time

The settling time of the frequency synthesizer is 50u s. The settling time depends on whether the loop is faster or slower. The settling time can be improved by making the

loop bandwidth narrow, but it increases the loop capacitor. This means an increase in the area of the chip. The design of settling time always involves a trade-off between phase noise and area.

8.5 Area

The area requirement for 0.25 μ m technology Bluetooth frequency synthesizer is 1mm X 1mm. The area of the Bluetooth frequency synthesizer is 0.3mm X 0.17mm. It meets the design specification very well. Table 12 summarizes the area of every element of the Bluetooth frequency synthesizer.

Parameter	Measurement
Colpitts oscillator	0.24mm X 0.14mm
Charge pump	0.112mm X 0.046mm
Phase frequency detector	0.173mm X 0.034mm
TSPC divide-by-128	0.118mm X 0.038mm
Bluetooth frequency synthesizer	0.3mm X 0.17mm

Table 12: Area of Bluetooth Frequency Synthesizer

8.6 Performance of Bluetooth Frequency Synthesizer

The comparison of the performance of the design with the Bluetooth frequency synthesizer specification is summarized in Table 13. It is found that settling time, area, and power parameters of the frequency synthesizer meets the design specifications very well. The phase noise performance can be improved, but it's a trade-off between settling time and area.

Parameter	Specification	Measurement
Technology	0.25u m	0.25u m
Supply Voltage	2.5 V	2.5 V
Frequency range	2.4G Hz – 2.48G Hz	2.36G Hz – 2.5G Hz
Frequency Resolution	1M Hz	1M Hz
Tuning range	~3%	~14%
Phase noise	-89 dBc / Hz	-50dBc/Hz to -10dBc/Hz
Spur	-49 dBc / Hz	-90dBc/Hz to -70dBc/Hz
Settling time	< 62.5u S	50u S
Power	< 70m W	8m W
Area	1 mm X 1mm	0.3mm X 0.17mm
Cost	\$2.1 - \$3.0	\$0.2 - \$0.3

Table 13: Summary of Specifications and Measured Results

Chapter 9

CONCLUSIONS

The design and implementation of the Bluetooth frequency synthesizer using 0.25 μ m technology has been presented. The Colpitts oscillator provides good phase noise and consumes low power. The measured phase noise is between -50dBc/Hz to -10dBc/Hz and spurious tone is between -90dBc/Hz to -70dBc/Hz . Although the output is a smooth sine wave, the phase noise and spurious tones does not meet the standard specifications, because the software failed to generate the accurate time stamps. It consumes about 8 mW of power, which is 88% improvement over the design specifications. The settling time of the loop is 50 μ s, which is 20% better than design specifications. The area with off-chip loop filter and inductor is 0.3mm X 0.17mm, which is cost effective.

Faster settling time can be achieved by using on-chip passive discrete low pass filter, rather than a third order loop filter. Using dual path loop filter can reduce the loop filter component sizes. For monolithic design, the inductor can be made on-chip by using a bond-wire, which has high Q required for the RF designs. A better loop filter can be designed for filtering high frequency components and spurious tones to achieve better phase noise.

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Appendix A

TSMC 0.25u TSMC Run T39S Data Sheet

MOSIS PARAMETRIC TEST RESULTS

RUN: T39S (MM_NON-EPI)
TECHNOLOGY: SCN025

VENDOR: TSMC
FEATURE SIZE: 0.25 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: TSMC 0251P5M

TRANSISTOR PARAMETERS W/L N-CHANNEL P-CHANNEL UNITS

MINIMUM	0.36/0.24		
Vth	0.47	-0.50	volts
SHORT	20.0/0.24		
Idss	562	-248	uA/um
Vth	0.48	-0.54	volts
Vpt	7.6	-7.2	volts
WIDE	20.0/0.24		
Ids0	7.6	< 2.5	pA/um
LARGE	50/50		
Vth	0.41	-0.58	volts
Vjbkd	4.8	-5.0	volts
Ijlk	<50.0	<50.0	pA
Gamma	0.44	0.61	V ^{0.5}
K' (Uo*Cox/2)	125.6	-24.9	uA/V ²
Low-field Mobility	414.66	82.21	cm ² /V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPICE model card.

Design Technology	XL (um)	XW (um)
SCN5M_DEEP (lambda=0.12)	0.00	-0.04
thick oxide, NMOS	-0.01	-0.04
thick oxide, PMOS	-0.06	
SCN6M_SUBN (lambda=0.15)	-0.06	0.00
thick oxide, NMOS	-0.10	0.00
thick oxide, PMOS	-0.15	

FOX TRANSISTORS GATE N+ACTIVE P+ACTIVE UNITS
 Vth Poly >6.6 <-6.6 volts

PROCESS PARAMETERS N+ P+ POLY N+BLK PLY+BLK MTL1 MTL2 UNITS
 Sheet Resistance 4.1 3.0 3.7 60.3 176.7 0.07 0.07 ohms/sq
 Contact Resistance 6.0 5.1 5.1 2.35 ohms
 Gate Oxide Thickness 57 angstrom

PROCESS PARAMETERS MTL3 MTL4 MTL5 N_W UNITS
 Sheet Resistance 0.07 0.07 0.03 975 ohms/sq
 Contact Resistance 5.18 7.38 10.02 ohms

COMMENTS: BLK is silicide block.

CAPACITANCE PARAMETERS N+ P+ POLY M1 M2 M3 M4 M5 R_W D_N_W M4P N_W
 UNITS
 Area (substrate) 1748 1906 108 34 15 9 5 4 121 116 aF/um^2
 Area (N+active) 6103 50 20 13 11 9 aF/um^2
 Area (P+active) 5841 aF/um^2
 Area (poly) 58 17 10 7 6 aF/um^2
 Area (metal1) 38 14 9 7 aF/um^2
 Area (metal2) 34 14 9 aF/um^2
 Area (metal3) 37 15 aF/um^2
 Area (metal4) 42 982 aF/um^2
 Area (r well) 1751 aF/um^2
 Area (d well) 526 aF/um^2
 Area (no well) 1591 aF/um^2
 Fringe (substrate) 407 347 42 36 22 aF/um
 Fringe (poly) 72 43 31 24 21 aF/um
 Fringe (metal1) 62 37 24 aF/um
 Fringe (metal2) 53 37 29 aF/um
 Fringe (metal3) 58 38 aF/um
 Fringe (metal4) 68 aF/um
 Overlap (N+active) 579 aF/um
 Overlap (P+active) 684 aF/um

CIRCUIT PARAMETERS UNITS
 Inverters K
 Vinv 1.0 0.98 volts
 Vinv 1.5 1.06 volts
 Vol (100 uA) 2.0 0.12 volts
 Voh (100 uA) 2.0 2.24 volts
 Vinv 2.0 1.12 volts
 Gain 2.0 -18.94
 Ring Oscillator Freq.
 D1024_THK (31-stg,3.3V) 190.60 MHz
 DIV1024 (31-stg,2.5V) 250.22 MHz

Ring Oscillator Power
 D1024_THK (31-stg,3.3V) 0.10 uW/MHz/gate
 DIV1024 (31-stg,2.5V) 0.06 uW/MHz/gate

COMMENTS: DEEP_SUBMICRON

T39S SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

```
* DATE: Nov 14/03
* LOT: T39S          WAF: 6005
* Temperature_parameters = Default
.MODEL CMOSN NMOS (          LEVEL = 49
+VERSION = 3.1      TNOM = 27      TOX = 5.7E-9
+XJ = 1E-7          NCH = 2.3549E17 VTH0 = 0.3541717
+K1 = 0.4730605     K2 = 3.690193E-5 K3 = 1E-3
+K3B = 3.6085943    W0 = 1E-7      NLX = 1.859848E-7
+DVT0W = 0          DVT1W = 0      DVT2W = 0
+DVT0 = 0.3689274   DVT1 = 0.5135528 DVT2 = -0.5
+U0 = 272.8655753   UA = -1.604422E-9 UB = 2.759541E-18
+UC = 3.303343E-11 VSAT = 1.33276E5  A0 = 1.8058967
+AGS = 0.3236498    B0 = -4.831642E-8 B1 = 1.608348E-8
+KETA = -8.917383E-3 A1 = 1.569503E-4 A2 = 0.4679635
+RDSW = 200         PRWG = 0.3216259 PRWB = -0.1423427
+WR = 1             WINT = 0        LINT = 0
+XL = 0             XW = -4E-8      DWG = -1.692362E-8
+DWB = 4.413808E-9 VOFF = -0.0871132 NFACTOR = 1.4575308
+CIT = 0            CDSC = 2.4E-4   CDSCD = 0
+CDSCB = 0          ETA0 = 3.734602E-3 ETAB = 1.282082E-4
+DSUB = 0.020612    PCLM = 1.9751054 PDIBLC1 = 1
+PDIBLC2 = 2.379099E-3 PDIBLCB = 0.0715542 DROUT = 1
+PSCBE1 = 3.031354E8 PSCBE2 = 1.315546E-7 PVAG = 0
+DELTA = 0.01       RSH = 4.1      MOBMOD = 1
+PRT = 0            UTE = -1.5      KT1 = -0.11
+KT1L = 0           KT2 = 0.022     UA1 = 4.31E-9
+UB1 = -7.61E-18    UC1 = -5.6E-11  AT = 3.3E4
+WL = 0             WLN = 1         WW = 0
+WWN = 1            WWL = 0         LL = 0
+LLN = 1            LW = 0          LWN = 1
+LWL = 0            CAPMOD = 2      XPART = 0.5
+CGDO = 5.79E-10    CGSO = 5.79E-10 CGBO = 1E-12
+CJ = 1.738242E-3   PB = 0.99      MJ = 0.4608568
+CJSW = 3.901269E-10 PBSW = 0.99   MJSW = 0.3243988
+CJSWG = 3.29E-10   PBSWG = 0.99   MJSWG = 0.3243988
+CF = 0             PVTH0 = -7.801675E-3 PRDSW = -10
+PK2 = 3.477551E-3  WKETA = 0.0124031 LKETA = 1.114023E-3 )
*
.MODEL CMOSP PMOS (          LEVEL = 49
+VERSION = 3.1      TNOM = 27      TOX = 5.7E-9
+XJ = 1E-7          NCH = 4.1589E17 VTH0 = -0.5537687
+K1 = 0.6428098     K2 = -1.176822E-3 K3 = 0
+K3B = 14.1277692   W0 = 1E-6      NLX = 2.526792E-8
```

```

+DVT0W = 0      DVT1W = 0      DVT2W = 0
+DVT0 = 2.5874047 DVT1 = 1      DVT2 = -0.1343136
+U0 = 100      UA = 9.388591E-10 UB = 1E-21
+UC = -1E-10    VSAT = 1.314478E5 A0 = 1.0391221
+AGS = 0.161067 B0 = 6.180213E-7 B1 = 5E-6
+KETA = 0.0159497 A1 = 0.0284007 A2 = 0.3
+RDSW = 2.015596E3 PRWG = -0.0469299 PRWB = -0.046582
+WR = 1      WINT = 0      LINT = 3.724045E-8
+XL = 0      XW = -4E-8    DWG = -4.032385E-8
+DWB = 3.497457E-9 VOFF = -0.1311201 NFACTOR = 1.1438388
+CIT = 0      CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0     ETA0 = 0.1728158 ETAB = -0.0187082
+DSUB = 1.0886163 PCLM = 1.359894 PDIBLC1 = 4.289016E-3
+PDIBLC2 = -1.185323E-9 PDIBLCB = -2.132891E-4 DROUT = 0.0783642
+PSCBE1 = 3.104525E10 PSCBE2 = 3.423805E-9 PVAG = 9.025521E-3
+DELTA = 0.01    RSH = 3      MOBMOD = 1
+PRT = 0      UTE = -1.5     KT1 = -0.11
+KT1L = 0      KT2 = 0.022    UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0      WLN = 1      WW = 0
+WWN = 1      WWL = 0      LL = 0
+LLN = 1      LW = 0      LWN = 1
+LWL = 0      CAPMOD = 2      XPART = 0.5
+CGDO = 6.84E-10 CGSO = 6.84E-10 CGBO = 1E-12
+CJ = 1.893734E-3 PB = 0.9889579 MJ = 0.4705132
+CJSW = 3.124347E-10 PBSW = 0.8 MJSW = 0.2786992
+CJSWG = 2.5E-10 PBSWG = 0.8 MJSWG = 0.2786992
+CF = 0      PVTH0 = 4.241515E-3 PRDSW = -0.8425843
+PK2 = 2.37439E-3 WKETA = 0.029515 LKETA = -7.186867E-3

```


Appendix B

Verilog-AMS Simulation Source Code

// Phase-Frequency Detector with Charge Pump

```

`include "disciplines.vams"
`include "constants.vams"
// This model exhibits no jitter
module pfd_cp (out, ref, vco);
output out; electrical out;          // current output
input ref; voltage ref;              // positive input (edge
triggered)
input vco; voltage vco;              // inverting input (edge
triggered)
parameter real iout=100u;            // maximum output current
parameter real vh=+1;               // output voltage in high state
parameter real vl=-1;               // output voltage in low state
parameter real vth=(vh+vl)/2;       // threshold voltage at
input
parameter integer dir=1 from [-1:1] exclude 0;
                                     // dir=1 for positive edge trigger
                                     // dir=-1 for negative edge trigger

parameter real tt=1n from (0:inf); // transition time
of output signal
parameter real td=0 from (0:inf); // average delay
from input to output
integer state;
analog begin
    @(cross(V(ref)-vth, dir))
        if (state > -1) state = state - 1;
    @(cross(V(vco)-vth, dir))
        if (state < 1) state = state + 1;
    I(out) <+ transition(iout*state, td, tt);
end
endmodule

```

```
// VerilogA for 0.25UTSMC, Oscillator_VA, veriloga
```

```
`include "constants.vams"
`include "disciplines.vams"
module Oscillator_VA(out, in);
    parameter real Vin_min=0.435;
    parameter real Vin_max=1.8;
    parameter real Fmax=2.498E9;
    parameter real Fmin=2.389E9;
    parameter real Vout_offset=0.8;
    parameter real amp=0.85;
    input in; output out;
    voltage out, in;
    real freq, phase;
    analog begin
        freq= (V(in) - Vin_min)*(Fmax - Fmin) / (Vin_max - Vin_min) + Fmin;
        if (freq > Fmax) freq = Fmax;
        if (freq < Fmin) freq = Fmin;
        phase = 2*M_PI*idtmod(freq, 0.0, 1.0, -0.5);
        V(out) <+ Vout_offset+amp*sin(phase);
    end
endmodule
```

```
// VerilogA for 0.25UTSMC, divider, veriloga
```

```
`include "constants.h"
`include "discipline.h"
module divider (out, in);
    output out; voltage out;          // output
    input in; voltage in;             // input (edge triggered)
    parameter real vh=2.5;             // output voltage in high state
    parameter real vl=0;               // output voltage in low state
    parameter real vth=1.08;           // threshold voltage at input
    parameter integer ratio=2 from [2:inf]; // divide ratio
    parameter integer dir=1 from [-1:1] exclude 0;
        // dir=1 for positive edge trigger
        // dir=-1 for negative edge trigger
    parameter real tt=417p from (0:inf); // transition time of output signal
    parameter real td=417p*6 from (0:inf); // average delay from input to output
    integer count, n;
    analog begin
        @(cross(V(in) - vth, dir)) begin
            count = count + 1; // count input transitions
            if (count >= ratio)
                count = 0;
            n = (2*count >= ratio);
        end
        V(out) <+ transition(n ? vh : vl, td, tt);
    end
endmodule
```

Appendix C

“C” Program to Find PLL Loop Parameters

// shri.cpp : Defines the entry point for the console application

```
#include "stdafx.h"
#include "math.h"
#define _USE_MATH_DEFINES
const double PI = 3.1415926535;
int main(int argc, char* argv[])
{
    double Ip = 1.0e-5;
    double Cp = 1.0e-13;
    FILE *fResultFile;
    fResultFile = fopen("c:\\result.txt", "wt+");
    if(fResultFile == NULL)
    {
        printf("file could not be opened for writing");
        return 0;
    }
    fputs("Ip,\t\tCp,\t\tWn,\t\tFn,\t\tRp,\t\tR2,\t\tC2,\t\tV2,\t\tC3,\t\tV3,\t\tKpd2,\t\tKpd3,\t\tH2,\t\tH3,\t\tX,\t\tY2,\t\tY3,\t\tG2,\t\tG3,\t\tYg2,\t\tYg3\n", fResultFile);
    for(double IpLoop = Ip; IpLoop < 1.0e-3; IpLoop = IpLoop+1.0e-5)
    {
        for(double CpLoop = Cp; CpLoop < 1.0e-10; CpLoop = CpLoop+1.0e-13)
        {
            long double WnSquare = (14.16*1.0e+6*IpLoop)/(CpLoop*4);
            long double Wn = sqrt(WnSquare);
            long double Fn = (1/(2*PI))*Wn;
            long double RpSquare = 1.416*1.0e-7/(IpLoop*CpLoop);
            long double Rp = sqrt(RpSquare);
            long double R2 = 3*Rp;
            long double C2 = CpLoop/10;
            long double V2 = (833.33*1.0e-12)*(IpLoop/C2);
            long double C3 = CpLoop/5;
            long double V3 = (833.33*1.0e-12)*(IpLoop/C3);
            long double Kpd2 = V2/PI;
            long double Kpd3 = V3/PI;
            long double H2 = 22.25*1.0e6*Kpd2;
            long double H3 = 22.25*1.0e6*Kpd3;
            long double Y2 = 20*log10(H2);
            long double Y3 = 20*log10(H3);
            long double X = log10(Wn);
            long double G2 = 14.16*1.0e6*Kpd2;
            long double G3 = 14.16*1.0e6*Kpd3;
            long double Yg2 = 20*log10(G2);
            long double Yg3 = 20*log10(G3);

            char buffer[1024];
```


Appendix D

Abbreviations

AC	Alternating Current
AMS	Analog Mixed Signal
CP	Charge Pump
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DC	Direct Current
DDFS	Direct Digital Frequency Synthesis
DLL	Delay Locked Loop
FFT	Fast Fourier Transform
GFSK	Gaussian Frequency Shift Keying
GPRS	General Packet Radio Service
ISM	Industrial Scientific and Medicine
LAN	Local Area Networking
LC	Inductor-Capacitor
LFCSP	Lead Frame Chip Scale Package
LPF	Low Pass Filter
MOS	Metal Oxide Semiconductor
MIM	Metal Insulator Metal
PC	Personal Computer
PDA	Personal Digital Assistant
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
QFN	Quality Flatpack No-lead
RF	Radio Frequency
ROM	Read Only Memory
TSMC	Taiwan Semiconductor Manufacturing Company
TSPC	True Single Phase Logic
TSSOP	Thin Shrink Small Outline Package
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
WAP	Wireless Application Protocol