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An NMOS transistor with localized channel and pocket implantations

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AN NMOS TRANSISTOR WITH LOCALIZED CHANNEL AND POCKET
IMPLANTATIONS

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

By

Salih Kilic

August 2005

UMI Number: 1429433

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ABSTRACT

AN NMOS TRANSISTOR WITH LOCALIZED CHANNEL AND POCKET IMPLANTATIONS

by Salih Kilic

Metal Oxide Semiconductor (MOS) technology is the leading technology in fabricating modern integrated circuits due to its lower power dissipation than older bipolar type technologies. However, further steps taken towards minimization bring new challenges in device design and fabrication. As the channel length is reduced, well-known charge sharing effects in the channel and high electric fields at the drain-channel interface become important elements to impact MOS device performance. Digital circuits fabricated with minimal channel lengths do not show significant performance improvement unless other device design issues such as parasitic source/drain capacitance and bulk effect are also resolved during the device design cycle. This thesis, therefore, addresses both, how to improve short channel effect as well as decrease bulk effect and source/drain capacitance as the transistor effective channel length is reduced. Throughout this study, Silvaco's Atlas Device Design Environment was used for design work and optimization.

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CHAPTER 1

INTRODUCTION

1.1 Background

The ease of scalability in gate channel length and width, drain and source junction depths, gate oxide thickness of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) enabled gate lengths to be reduced three orders of magnitude from 10 μm in 1970s to sub-100 nm of today [1]. Currently, most of the research has focused on fabricating 45 nm effective channel lengths [2], however, working 22 nm channel length devices are demonstrated to be fully functional [3]. Therefore, manufacturing the smallest transistor has become the mainstream goal of semiconductor companies targeting high performance and high density integrated circuit fabrication.

As minimization efforts continue, Short Channel Effects (SCE) arise impacting device design. One of the major SCE is the charge sharing effect in the channel [4], which causes the threshold voltage (V_T) to decrease as the effective channel length is reduced. MOS transistors with halo implants around source and drain junctions [5] decreased the charge sharing effect at the expense of generating electron hole pairs at lower drain-source voltages. The other important issue with short gate lengths is the escalating electric field at the drain-channel interface which promotes early impact ionization and the resultant hot electron effect to alter device trans-conductance. Lightly Doped Drain (L_{DD}) [6] was introduced in short channel MOS transistors to decrease high drain fields, but the transistor trans-conductance deteriorated as a result of high parasitic

resistance of the L_{DD} region in the conduction path. Minimization also developed latch-up issues in digital circuits. Silicon-On-Insulator (SOI) [7] and dual-gate type [8] transistors have been developed to improve channel mobility and trans-conductance, transistor isolation and latch-up at the expense of fabrication complexity.

The miniaturization of MOS devices impacts digital circuit performance. Two effects that degrade circuit performance are the parasitic source/drain (S/D) junction capacitance and the bulk effect [9]. Shallow junctions in the order of 20 to 30 nm depth are achieved by elevating the source and drain junctions [10] to reduce S/D junction capacitance. Very low Boron implants between 5 and 10 keV range are administered into the channel to minimize the bulk effect [11].

1.2 Overview of the Thesis

In this thesis, short channel effects as well as the elements to reduce digital circuit performance are eliminated by altering the channel design. The charge sharing effect is reduced by introducing heavy pocket implants adjacent to L_{DD} regions; the circuit performance is enhanced by decreasing source/drain junction capacitances and controlling the bulk effect by localized channel implants.

During this study, various conventional and enhanced NMOS device channel and L_{DD} profiles were compared with each other and a complete device characterization was conducted for both types for effective channel lengths between 0.1 μm and 1 μm . Chapter 2 of this thesis covers to state-of-the art CMOS technology comprising current device structures, processing steps and scaling issues. Chapter 3 explains Silvaco's Atlas

Device Design Environment, and the use of this CAD platform for NMOS transistor simulations. Chapter 4 focuses on the conventional NMOS transistor design, which constitutes the base of this study. Channel lengths which range from 0.1 μm to 1.0 μm and L_{DD} regions between 50 and 90 nm were used to determine an optimum device configuration to yield maximum dc trans-conductance, and minimum bulk effect and S/D parasitic junction capacitance in this chapter. Chapter 5 illustrates the processing steps and the resultant device profile of the enhanced NMOS transistor. The channel length, junction profile and depth, gate material and oxide thickness were unchanged. The channel implant was altered by introducing heavy pocket implants adjacent to L_{DD} regions and a localized channel implant under the physical gate to improve the SCE and decrease source/drain junction capacitances and bulk effect.

CHAPTER 2

CURRENT CMOS TECHNOLOGY

2.1 Current MOS Transistor Structure

CMOS technology has powered a revolution in integrated circuit technology in terms of its capabilities of high device performance and density and low power consumption. The state-of-the-art 90 nm device structure consists of very shallow S/D junctions, silicided poly-silicon gate, a composite thin gate oxide under 3 nm, non-overlapping L_{DD} regions, and a shallow channel implant for adjusting the device threshold as shown in Figure 2.1.

Figure 2.1: Current MOS Transistor Structure (from [12]).

2.2 CMOS Processing Steps

Current CMOS processing steps are illustrated below.

a. N-well Formation on p-substrate

b. Shallow Trench Formation

c. Threshold Implant

d. Gate Oxide Growth and Poly-silicon Formation

e. L_{DD} Implant

f. Oxide Spacer Formation

g. Source Drain Implant

h. Silicide Growth

i. Metal Contact Formation

Via step is not shown in this thesis.

2.3 Scaling Issues

Transistor size scaling has brought physical and performance issues. These are charge sharing effect, higher electric field at the drain, and high off current. Coming sections explain these problems.

2.3.1 Charge Sharing Effect

The primary short channel effect is the charge sharing between the channel and S/D junction implants as shown in Figure 2.2 which causes the threshold voltage to

decrease with decreasing effective channel length in MOS transistors. To improve the fluctuation in V_T roll-off, a halo implant surrounding source and drain junctions has been used [13]. A more practical solution to control charge sharing is the formation of elevated S/D junctions. Junction depths as a result of this technique produce a smaller charge-shared area, and improve V_T roll-off [14].

Figure 2.2: A Simplified Charge Sharing Effect in NMOS Transistor

2.3.2 High Electric Field at the Drain

Another important SCE is the formation of high lateral electric field in the drain-channel interface. Electric fields exceeding 2×10^5 V/cm are known to generate electron-hole pairs in silicon due to impact ionization [15]. The ionization rate increases exponentially with increasing electric field; in NMOS transistors, holes form a substrate current collected at the substrate contact, and electrons form a gate leakage current collected at the gate contact. For gate oxide thicknesses over 5 nm, the electron current that consists of highly energetic electrons (hot electrons) permanently embed inside the

gate oxide layer and create fluctuations in the threshold voltage. To minimize this effect, L_{DD} was used [6]; however, high parasitic resistance of the L_{DD} region in the conduction path reduces the device trans-conductance. For gate oxide thicknesses less than 5 nm, the gate leakage current produces a leakage path in the oxide, which in time, creates gate degradation and produces device reliability problems. To prevent this problem, a composite oxy-nitrate gate oxide was suggested [16]. The resultant gate insulator to maintain field effect function is illustrated in Figure 2.3.

Figure 2.3: Gate Insulator Structure

2.3.3 Off Current

Another important effect as a result of decreasing gate length is the ability of highly energetic electrons (in NMOS transistors) to exceed the potential barrier at the source and travel in the bulk of the channel as minority carriers. This effect basically annihilates the channel modulation by a potential applied at the gate and thereby deteriorates the on/off functionality of the transistor [17].

2.3.4 Threshold Voltage Instabilities due to Channel Doping

The fluctuations in channel doping and threshold voltage become severe as the channel length is reduced. The solution is to design a transistor whose threshold voltage is independent of the charge doping density in the channel but solely determined by the work function of the gate material [18]. Gate materials made out of poly-SiGe and tungsten are the appropriate candidates to accomplish this task [19].

CHAPTER 3

TECHNOLOGY COMPUTER AIDED DESIGN (TCAD)

3.1 Silvaco's TCAD Tools

Process simulator Athena and Device simulator Atlas are used in this study.

The uses of these tools are:

- Semiconductor process modelling
- Device electrical characterization

3.2 Process Simulation Tool Athena

Athena solves the numerical equations for process steps. Defining the inputs in the deck for these specific process steps will create a structure we want. Achieving an accurate process simulation will reduce the design time [20]. Figure 3.1 summarizes the process simulation inputs and outputs.

Figure 3.1: Process Simulation Parameters

3.3 Device Simulation Tool Atlas

Atlas requires an input structure to extract device parameters. This structure can be acquired from process simulation or user can define that in Atlas. This platform generates I_D - V_D and I_D - V_G curves as an output depending on previously defined model and solution methods. Figure 3.2 summarizes the device simulation inputs and outputs.

Figure 3.2: Device Simulation Parameters

3.4 Models and Methods Used in this Thesis

Shockley-Read Hall carrier recombination model, Fermi-Dirac statistics, CVT mobility model and Band Gap Narrowing model are recommended models for MOS device simulations [8]. Due to high carrier concentration we have also implemented Auger [20] three carrier recombination model in our model. Additionally high electric field concern forced us to include Selberrherr's [20] impact ionization model. Newton's numerical method has selected to solve all these models. See Appendix A for all physical models, methods in current TCAD tools.

CHAPTER 4

CONVENTIONAL DEVICE DESIGN

4.1 Conventional Device

The first MOSFET transistor was demonstrated in 1960 [15]. It had a gate length $20\mu\text{m}$ and gate oxide thickness of 100nm . Every three years device dimensions are reduced for new technology. Currently gate length 90nm and gate oxide thickness 2nm devices are being manufacturing by companies. Every technology introduces new process steps to the transistor production. We have defined the conventional device, which has poly-silicon gate, source/drain junctions, lightly doped drain, and terminal electrodes.

In this chapter conventional device analysis will be done. We have selected enhancement type NMOS device for this study. Figure 4.1 illustrates a conventional NMOS device.

Figure 4.1: Conventional Device Cross Section

4.2 Technology Definition

During scaling, device format is limited by the technology definition. The minimum effective gate length for this design is set to $0.1\mu\text{m}$. For this case, power supply voltage (V_{DD}) should be 1.5V to prevent from high electric field at drain. Poly-silicon was used as a gate electrode. It can be created self aligned and is reliable under high temperature.

Gate oxide thickness was set to a 5nm. The minimum gate oxide thickness without tunneling concern can be 1.5nm for sub $0.1\mu\text{m}$ [21]. So 5nm gate oxide thickness is acceptable choice for this design. Gate doping density was chosen 10^{20}cm^{-3} and gate thickness was chosen to be 150nm. Short channel effect increases gate resistance with reducing gate dimensions [22]. Consequently the gate material selection and dimensions of gate become more significant for gate resistance. High gate resistance causes RC delay and reduces the operating speed [22]. The n-type source/drain junctions had a peak doping density of 10^{20}cm^{-3} . The approximate junction depth was 100nm.

4.3 Expected Device Characteristics

Threshold voltage fluctuation, trans-conductance, substrate leakage current, and the standby current are the main transistor parameters to decide the performance of the device. Our specifications for this study were:

$$V_T = 0.3V \text{ (20\% of } V_{DD}) \text{ at } L_{EFF} = 1\mu m$$

$$\Delta V_T \leq 200 \text{ mV due } L_{EFF}$$

$$\Delta V_T \leq 200 \text{ mV due substrate voltage } V_{SUB}$$

$$I_{SUB} \leq 100 \text{ nA } \mu m \text{ at } L_{EFF} = 0.1\mu m$$

$$G_{mSAT} \geq 100 \text{ mS/mm at } L_{EFF} = 0.1\mu m$$

Sub-threshold slope should be less than 80mV/dec for low power device to operate at low supply voltage.

4.4 Top-Down Design Methodology

Six different conventional NMOS device structures were constructed in Atlas platform which have the channel lengths 1 μm , 0.5 μm , 0.4 μm , 0.3 μm , 0.2 μm , and 0.1 μm . The following tasks were done to analyze the devices.

First, threshold doping adjustment was set in 1 μm device. The ideal threshold voltage should be 20 % of the supply voltage (V_{DD}). Second, lightly doped drain (L_{DD}) structure sets were constructed and trans-conductance (G_{mSAT}) versus substrate leakage current (I_{SUB}) analysis was done to select optimum device structure. Third, the V_T difference with changing the effective channel length (L_{EFF}) was investigated which

called V_T roll-off analysis. Fourth, different bias voltages were applied to the substrate. The change in the threshold voltage was investigated. Fifth, the changes in S/D junction capacitances were substantiated with applying different voltages to the substrate. These analyses will be explained in the coming sections.

4.5 V_T Analysis for Long Channel Device

Threshold voltage control is the one of the important parameter for MOSFET transistor.

The threshold voltage is equal to:

$$V_T = V_{FB} + \Psi_s + \frac{Q_c}{C_{ox}} \gamma \quad (4.1)$$

$$\text{Where, } C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad (4.2)$$

There is a flat-band voltage shift due to the effect of the fixed-oxide and the difference in work function. Additionally applied reverse bias voltage to substrate changes the depletion region width thus affecting V_T . Adding all these changes to the V_T the new V_T becomes:

$$V_T = V_{FB} + V_C + 2\Psi_B + \frac{\sqrt{2qN_A\epsilon_{si}(2\Psi_B + V_{CB})}}{C_{ox}} \quad (4.3)$$

The p-type substrate doped to 10^{15} cm^{-3} with boron concentration however this concentration can not provide the threshold voltage of 0.3 V so threshold adjustment implantation has to be done. In $1 \mu\text{m}$ device, peak doping concentration was increased to

$2.85 \times 10^{17} \text{ cm}^{-3}$ and characteristic length was set to a 0.12 to get the Gaussian profile for expected peak concentration.

Figure 4.2 illustrates the conventional device lateral channel doping profile.

Figure 4.2: 1 μm Conventional Device Lateral Doping Profile

During the annealing process the boron tail becomes a problem. This tail needs to be compensated. We have run a few different simulations to find the right boron profile. The best profile was obtained with boron dose $5 \times 10^{12} \text{ cm}^{-2}$ and with 8keV implantation energy. Annealing time was found 30 minutes and the temperature was needed to be set 980 °C.

4.6 Lightly Doped Drain (L_{DD}) Engineering for Conventional Device

Once the channel doping has been determined different lightly doped drain structures were established. The reason creating that many structure was L_{DD} has significant effect on trans-conductance and substrate leakage current. Therefore L_{DD} doping, length, and depth should be optimized. The ideal L_{DD} structure has to provide maximum trans-conductance while maintaining the minimum substrate leakage current. In this study four different doping profiles were matched with three different L_{DD} lengths. All the L_{DD} depths were kept at 50 nm. Table 1 shows the possible L_{DD} configurations.

TABLE 1: L_{DD} PARAMETERS FOR $L_{EFF} = 0.1 \mu\text{M}$ TRANSISTOR

L_{DD} doping (cm^{-3})	L_{DD} depth (nm)	L_{DD} length (nm)
4×10^{17}	50	50, 70, 90
6×10^{17}	50	50, 70, 90
8×10^{17}	50	50, 70, 90
1×10^{18}	50	50, 70, 90

4.7 High Performance Device Selection

Short channel devices provide high trans-conductance but also due to short channel effects they have higher substrate leakage current. Therefore the target device needs to be short channel device. In this study 0.1 μ m device was selected as a shortest device. Maximum drain currents (I_D) for different L_{DD} structures were simulated. Additionally maximum substrate leakage currents were found for same devices. Trans-conductance can be found with maximum drain current ($I_{D_{smax}}$) divided by the supply voltage.

$$G_{mSAT} = \frac{I_{dsmax}}{V_{DD}} \quad (4.4)$$

All the L_{DD} combinations were simulated and the trans-conductance and the substrate leakage current values were extracted. Table 2 shows the results of the simulations.

TABLE 2: SIMULATION RESULTS FOR DIFFERENT L_{DD} STRUCTURES

L_{DD} length 50 (nm)	L_{DD} doping (cm^{-3})	Gm_{SAT} (ms/mm)	I_{DSMAX} (A/ μm)	I_{SUBMAX} (A/ μm)
	4×10^{17}	151.123	2.266×10^{-4}	7.59632×10^{-7}
	6×10^{17}	178.895	2.683×10^{-4}	4.98149×10^{-7}
	8×10^{17}	205.772	3.086×10^{-4}	3.12071×10^{-7}
	1×10^{18}	232.524	3.487×10^{-4}	5.49937×10^{-7}
L_{DD} length 70 (nm)	L_{DD} doping (cm^{-3})	Gm_{SAT} (ms/mm)	I_{DSMAX} (A/ μm)	I_{SUBMAX} (A/ μm)
	4×10^{17}	109.172	1.637×10^{-4}	2.17049×10^{-7}
	6×10^{17}	137.428	2.061×10^{-4}	1.35820×10^{-7}
	8×10^{17}	168.383	2.525×10^{-4}	1.30785×10^{-7}
	1×10^{18}	192.506	2.887×10^{-4}	2.90843×10^{-7}
L_{DD} length 90 (nm)	L_{DD} doping (cm^{-3})	Gm_{SAT} (ms/mm)	I_{DSMAX} (A/ μm)	I_{SUBMAX} (A/ μm)
	4×10^{17}	74.632	1.119×10^{-4}	5.74726×10^{-9}
	6×10^{17}	111.096	1.666×10^{-4}	3.06399×10^{-8}
	8×10^{17}	143.239	2.148×10^{-4}	7.47735×10^{-8}
	1×10^{18}	168.615	2.529×10^{-4}	1.96718×10^{-7}

All the simulation results are drawn on the trans-conductance (G_{mSAT}) versus substrate leakage current (I_{SUBMAX}) graph. Target device has to have low I_{SUBMAX} and high G_{mSAT} . Figure 4.3 illustrates G_{mSAT} versus I_{SUBMAX} .

Figure 4.3: G_{mSAT} versus I_{SUBMAX}

We need to select a device that meets the requirements in the below.

$$I_{SUBMAX} \leq 100 \text{ nA } \mu\text{m at } L_{EFF} = 0.1 \mu\text{m}$$

$$G_{mSAT} \geq 100 \text{ mS/mm at } L_{EFF} = 0.1 \mu\text{m}$$

The L_{DD} configuration with 90nm length, 50nm depth and $8 \times 10^{17} \text{ cm}^{-3}$ doping concentration was found and circled as a better candidate for conventional device.

4.8 Designing Different L_{EFF} Geometries

After deciding the right L_{DD} configuration other device structures have been created. These devices have 0.2 μm , 0.3 μm , 0.4 μm , 0.5 μm and 1 μm effective channel lengths and same doping profiles like 0.1 μm device. Device performance degradation can be seen with scaling the devices.

4.9 V_T Roll-off Analysis

V_T roll-off analysis is the one of the important device performance criteria. Threshold voltage changes by changing device sizes which demonstrates V_T roll-off. We have observed threshold voltage was decreasing by lowering the device size. The reason is charge sharing ratio changes during the decreasing device sizes. Large V_T fluctuations are unwanted behavior for analog circuit designs. Figure 4.4 shows the I_D - V_G curve of the conventional device for V_T . Also see Appendix B for other I_D - V_G curves for V_T .

Figure 4.4: Conventional Device I_D - V_G Curve

Table 3 shows the simulation results of the V_T for different L_{EFF} . Figure 4.5 is the V_T roll-off graph for different device sizes.

TABLE 3: V_T VALUES FOR DIFFERENT L_{EFF}

L_{EFF} (μm)	V_T (V)
0.1	0.175648
0.12	0.201904
0.15	0.222188
0.2	0.236417
0.25	0.253143
0.3	0.264305
0.4	0.276667
0.5	0.283353
1	0.30174

Figure 4.5: Conventional Device V_T Roll-Off

4.10 Bulk Effect Analysis

Substrate biasing causes changes in V_T . Increasing substrate bias voltage increases the V_T , which is called as a bulk effect. Bulk effect is important because of small increase in V_T decreases transistor's current capability or G_{mSAT} . True changes in V_T as a function of substrate bias can be measured more accurately in a long channel device due to the negligible effect imposed by the charge-sharing factor. Table 4 shows the simulation results of the V_T for different L_{EFF} . Figure 4.6 illustrates conventional device bulk effect.

TABLE 4: THE EXTRACTED VALUES FOR V_T UNDER DIFFERENT SUBSTRATE BIASING

VOLTAGE

<i>Bulk Effect of Conventional Device</i>	
$V_{SUB}=-0.5$	$V_T=0.398207$
$V_{SUB}=-1$	$V_T=0.469574$
$V_{SUB}=-1.5$	$V_T=0.527191$
$V_{SUB}=-2$	$V_T=0.567008$
$V_{SUB}=0$	$V_T=0.30174$
$V_{SUB}=0.5$	$V_T=0.158972$

Figure 4.6: Conventional Device Bulk Effect

4.11 On Current (I_{ON}) Analysis

I_D - V_{DD} curves for all transistors were simulated by setting the gate voltages (V_G) to 50mV and 1.5V. On current is the maximum current while the supply voltage and the gate voltage are at their maximum value. Table 5 shows the on current values for all devices.

TABLE 5: I_{ON} FOR DIFFERENT L_{EFF}

L_{EFF} (μm)	I_{ON} (A)
0.1	2.06×10^{-4}
0.12	1.99×10^{-4}
0.15	1.92×10^{-4}
0.2	1.81×10^{-4}
0.25	1.72×10^{-4}
0.3	1.64×10^{-4}
0.4	1.49×10^{-4}
0.5	1.36×10^{-4}
1	0.906×10^{-4}

Also electric field and potential contours were simulated to observe the potential impact ionization problems. See Appendix B for all I_D - V_{DD} curves, electric field, and potential contours.

4.12 Standby Current (I_{OFF}) Analysis

Gate voltage was set to the zero value. Supply voltage was swept from 0 to 1.5V. Off current is an important parameter to decide device's power consumption. If this

value is significantly high, transistor consumes too much power. See Appendix B for I_{OFF} curves.

4.13 Substrate Leakage Current (I_{SUB}) Analysis

Supply voltage was set to $V_{DD}=50mV$ and $V_{DD}=1.5V$ gate voltage V_G was swept from 0 to 1.5 V. See Appendix B for I_{SUB} curves.

4.14 Junction Capacitance (C_J) Analysis

Junction capacitance is another important parameter for devices. Higher junction capacitances increase gate delays and slow output nodes in digital circuits. We extracted small signal capacitance between the source and substrate terminals of a long channel device as a function of substrate bias voltage. Figure 4.7 shows the Tonyplot® output of the Atlas for substrate to source capacitance. Capacitance was simulated for low and high supply voltages. The red curve demonstrates capacitance under low supply voltage and green one stands for under high supply voltage.

Figure 4.7: 1 μ m Conventional Device Substrate-Source Capacitance

See Appendix B for all conventional device simulation results and structure profiles.

CHAPTER 5

ENHANCED DEVICE DESIGN

5.1 Enhanced Device

An enhanced device has some process step differences than the conventional device. Local channel implantation and inside side wall creation are these differences. This chapter explains the process steps of the enhanced device and its simulation results compared with the conventional device. The next section will illustrate enhanced device process steps.

5.2 Enhanced Device Process Steps

Enhance device process steps.

1. Step

Gate oxide was grown; poly, silicon nitride, and photo-resist were deposited on the p⁺ substrate.

2. Step

Mask was applied after lithography then photo-resist and the poly at the top was etched.

3. Step

Local channel implantation (LCI).

Silicon nitride was etched and the resist was removed. Then boron was implanted for channel implantation.

4. Step

Pocket Implantation (PI).

SiO₂ side wall was grown inside the etched region. Arsenic was implanted through the channel. Under the side walls, channel was kept p⁺ concentration however in the middle; channel became p type due to arsenic implant.

5. Step

The side wall oxide was removed and poly was deposited over the poly then chemical mechanical polishing was done.

6. Step

100-200Å oxide was grown with wet oxidation over the poly and silicon nitride, then unnecessary poly was removed.

7. Step

100 Å screen oxide was deposited and arsenic was implanted for LDD.

8. Step

Side wall oxide was grown for n^+ source/drain junction implantation.

Figure 5.1 is the enhanced device structure after simulation.

Figure 5.1: Enhanced Device Structure with Doping Profile

5.3 Technology Definition and Device Characteristics

Technology definition and device characteristics for enhanced device are same as conventional device. The goal is to observe the benefits of enhanced device under same situation as conventional one.

5.4 Design Challenges

Pocket and local channel implantation process steps are illustrated at section 5.2. At the channel two implantations has been done. First p^+ boron was implanted through the entire channel then over this implantation n type arsenic was doped as a part of the channel. 20 nm pockets were created interfacing the L_{DD} by these implantations. The length and the doping concentration of the pockets are very important for this design. If depletion layer of this pockets overlap to the lightly doped drain, channel length increases. So this depletion region length should be minimized by pocket doping concentration, at the same time threshold voltage also should be maintained as 0.3 V with respect to this concentration. Pocket lengths are depends on to the side wall length. Minimum pocket length should be 20 nm to function properly in front of the L_{DD} . Less than 20 nm pockets were not control the charge sharing. Several simulations have been run to find the pocket concentrations and channel concentrations for enhanced device.

5.5 V_T Analysis for Long Channel Device

To design the threshold voltage to be 0.3V, we set the channel doping concentration as same as conventional one which was $2.85 \times 10^{17} \text{ cm}^{-3}$. After simulating this profile we got less threshold voltage. Several simulations were run to find the boron concentration and arsenic concentration for channel implantation. Then the right doping concentration for boron was found as $1.03 \times 10^{18} \text{ cm}^{-3}$; for arsenic concentration it was found to be $5 \times 10^{17} \text{ cm}^{-3}$. The characteristic length for both dopants was found 0.036. This length defines the place of the peak concentration for gaussian profiles. Same profiles should be maintained in real processes. In Athena we have run simulations to get

these profiles to prove they can be achievable. After finding the right doping profile we kept that profile for all the device structures.

Figure 5.2 shows lateral doping profile for enhanced device.

Figure 5.2: 1 μm Enhanced Device Lateral Doping Profile

5.6 L_{DD} Selection for Enhanced Device

For the Enhanced Device, L_{DD} doping, lengths, and depths were chosen same as conventional device. All the L_{DD} combinations were run in the simulation and the trans-

conductance and the substrate leakage current values were extracted. Table 6 shows the simulation results for different L_{DD} structures.

TABLE 6: SIMULATION RESULTS FOR DIFFERENT L_{DD} STRUCTURES

<i>L_{DD} length 50 (nm)</i>	<i>L_{DD} doping (cm^{-3})</i>	<i>G_{mSAT} (ms/mm)</i>	<i>I_{DSMAX} (A/μm)</i>	<i>I_{SUBMAX} (A/μm)</i>
	4×10^{17}	195.23	2.928×10^{-4}	3.71627×10^{-7}
	6×10^{17}	213.24	3.198×10^{-4}	2.81908×10^{-7}
	8×10^{17}	227.81	3.417×10^{-4}	3.13183×10^{-7}
	1×10^{18}	242.82	3.642×10^{-4}	4.76722×10^{-7}
<i>L_{DD} length 70 (nm)</i>	<i>L_{DD} doping (cm^{-3})</i>	<i>G_{mSAT} (ms/mm)</i>	<i>I_{DSMAX} (A/μm)</i>	<i>I_{SUBMAX} (A/μm)</i>
	4×10^{17}	155.74	2.336×10^{-4}	1.09727×10^{-7}
	6×10^{17}	174.79	2.621×10^{-4}	7.36548×10^{-8}
	8×10^{17}	201.76	3.026×10^{-4}	1.87850×10^{-7}
	1×10^{18}	211.70	3.175×10^{-4}	3.11337×10^{-7}
<i>L_{DD} length 90 (nm)</i>	<i>L_{DD} doping (cm^{-3})</i>	<i>G_{mSAT} (ms/mm)</i>	<i>I_{DSMAX} (A/μm)</i>	<i>I_{SUBMAX} (A/μm)</i>
	4×10^{17}	131.38	1.970×10^{-4}	3.52552×10^{-8}
	6×10^{17}	153.80	2.307×10^{-4}	4.47977×10^{-8}
	8×10^{17}	172.60	2.589×10^{-4}	1.18285×10^{-7}
	1×10^{18}	194.59	2.918×10^{-4}	2.93940×10^{-7}

To see the improvements in enhanced device we compare the results with the conventional device. Figure 5.3 shows performance curves for both devices.

Figure 5.3: $G_{m_{SAT}}$ versus I_{SUBMAX} for Both Devices

Better candidates for both devices are circled. We have selected the L_{DD} configuration with 70nm length, 50 nm depths, and 6×10^{17} cm $^{-3}$ doping concentration for enhanced device and the L_{DD} configuration with 90nm length, 50 nm depths, and 8×10^{17} cm $^{-3}$ doping concentration for conventional device.

5.7 Designing Different Channel Length Devices and V_T Roll-off Analysis

Nine different device structures were created and their I_D - V_G curves were simulated to find threshold voltages. The simulation results for V_T are showed in Table 7 for enhanced device. The V_T roll-off curves are illustrated in Figure 5.4.

TABLE 7: V_T RESULTS FOR DIFFERENT L_{EFF}

L_{EFF} (μm)	V_T (V)
0.1	0.234463
0.12	0.240892
0.15	0.249502
0.2	0.259201
0.25	0.266211
0.3	0.271438
0.4	0.278551
0.5	0.286842
1	0.304847

Figure 5.4: V_T Roll-off Curves for Both Devices

We have noticed significant improvements in enhanced device's V_T roll-off due to reducing charge sharing with new design aspect. V_T difference for conventional device between the longest and the shortest one was 126mV, for enhanced device it was 70mV. The built in potential between the L_{DD} and the p^+ pocket was higher than conventional device. The built in potential was:

$$V_{bi} = \Psi_n - \Psi_p = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right) \quad (5.1)$$

For enhanced device $V_{bi} = 0.9472$ V, for conventional device $V_{bi} = 0.9212$ V. The difference was 26mV. The depletion layer width is:

$$W = \sqrt{\frac{2\epsilon_s}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi}} = \sqrt{\frac{2\epsilon_s V_{bi}}{q N_D}} \quad (5.2)$$

For enhanced device depletion width $W=57.3\text{nm}$ and for conventional device $W=76\text{nm}$.

Short channel effect happens when the source/drain depletion region overlaps with the channel depletion region. The charges induced by the field created by the gate bias.

Therefore reducing channel length increases the probability of the overlap of depletion regions. Threshold voltage shift is equal to:

$$\Delta V_T = -\frac{q N_A W_m r_j}{C_o L} \left(\sqrt{1 + \frac{2W_m}{r_j}} - 1 \right) \quad (5.3)$$

Where $C_o = \frac{\epsilon_{ox}}{d}$, W_m is surface depletion and r_j is junction depth.

The depletion layer for enhanced device was less than the conventional device which proves our design reduces charge sharing.

5.8 Bulk Effect Analysis and Sub-threshold Slope

Substrate potential has effect on threshold voltage. The V_T change due to substrate potential is:

$$\Delta V_T = \frac{\sqrt{2\epsilon_s q N_A}}{C_o} \left(\sqrt{(2\Psi_B + V_{BS})} - \sqrt{2\Psi_B} \right) \quad (5.4)$$

The list of the change in V_T with biasing substrate is shown at Table 8.

TABLE 8: THE EXTRACTED VALUES FOR V_T UNDER DIFFERENT SUBSTRATE BIASING VOLTAGES

<i>Bulk Effect of Enhanced Device</i>	
$V_{SUB}=-0.5$	$V_T=0.311261$
$V_{SUB}=-1$	$V_T=0.316617$
$V_{SUB}=-1.5$	$V_T=0.321095$
$V_{SUB}=-2$	$V_T=0.325031$
$V_{SUB}=0$	$V_T=0.304001$
$V_{SUB}=0.5$	$V_T=0.25043$

Significant bulk effect improvements can be seen in Figure 5.5. Conventional and enhanced devices are compared in this figure.

Figure 5.5: Bulk Effect for Both Devices

Local channel implantation has been performed for enhanced device; therefore the channel doping concentration was quite higher than the conventional design to keep both threshold voltages at 0.3 V. Higher doping controls short channel effect but increases V_T fluctuations, however in our design, pockets prevent from this V_T fluctuations due to charge sharing retention.

Drain induced barrier lowering effect causes electron injection from source to drain which causes increase in sub-threshold current. The threshold voltage decreases with increasing the drain bias in short channel devices. To analyze sub-threshold slope we run two simulations with biasing the drain 50 mV and 1.5V. I_D - V_G curve gives the

slope but I_D should be extracted in a log scale. Sub-threshold slopes of both devices are given at Figure 5.6.

Figure 5.6: Sub-threshold Slope for Both Devices

5.9 I_{ON} Analysis

On current simulation results of enhanced device are shown on Table 9. See Appendix B for all I_D - V_D and I_{OFF} curves.

TABLE 9: SIMULATION RESULTS FOR DIFFERENT L_{EFF} DEVICES.

L_{EFF} (μm)	I_{ON} (A)
0.1	0.000262196
0.12	0.000249498
0.15	0.00023201
0.2	0.000207703
0.25	0.000188595
0.3	0.000172572
0.4	0.000146613
0.5	0.000126692
1	7.45702E-05

Also electric field and potential contours were simulated to observe the possible impact ionization problems. See Appendix B for electric field and potential contours.

5.10 Comparison of I_{OFF} between Conventional and Enhanced Design

Enhanced design's off current has increased. The reason for that was, punch through effect between the source and drain. I_{OFF} can be decreased by decreasing substrate concentration or by increasing the depth of the LCI region. I_{OFF} values by changing the L_{EFF} are shown in the Figure 5.7.

Figure 5.7: I_{OFF} versus L_{EFF} for Both Devices

5.11 Junction Capacitance (C_J) Analysis

Substrate potential has been increased 3mV steps while the supply voltages set to 50mV and 1.5V. The junction capacitance change at supply voltages 50mV and 1.5V is shown at Figure 5.8.

Figure 5.8: Junction Capacitance for Both Devices

With this design an 80% capacitance reduction has been obtained. LCI preserves no unnecessary p^+ doping at junctions. This reduces junction capacitance. Halo implantation increases junction capacitance because of all the junction area has been implanted with p^+ dopant but still halo has benefits over the conventional design in terms of better control of short channel effect. With local channel implantation and pocket implantation we have reduced junction capacitance without decreasing other device performances. See Appendix B for all enhanced device simulation results and structure profiles.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusion

The main purpose of this thesis was to show how to improve the short channel effects of an NMOS transistor and eliminate the elements that reduce digital circuit performance. The charge sharing effect is reduced by introducing heavy pocket implants adjacent to L_{DD} regions; the circuit performance is enhanced by decreasing parasitic source/drain junction capacitances and controlling the bulk effect by localized channel implants.

During this study, various channel and L_{DD} profiles were compared in conventional and enhanced NMOS device structures using Silvaco's Device Design Simulation Platform. The optimum conventional and enhanced NMOS transistors are characterized for effective channel lengths between 0.1 μm and 1 μm . The 1.5 V power supply voltage, gate material and dielectric, source and drain doping profiles are kept constant in both device structures.

As a result of this study, the threshold roll-off was improved from 200 mV to 50 mV when effective channel lengths were changed between 0.1 μm and 1.0 μm . The bulk effect was reduced from 200 mV/V to 50 mV/V, S/D parasitic junction capacitance was reduced from 2 fF/ μm to 0.2 fF/ μm , and G_{mSAT} was improved from 100 mS/mm to 150 mS/mm at a channel length of 0.1 μm .

The only drawback was the deterioration of the OFF (stand-by) current. This was resulting from a punch-through effect between the source and drain of the enhanced channel profile. The OFF current gradually decreased as the substrate concentration or the depth of the local channel implant increased. Needless to say, increasing substrate concentration raised the S/D drain capacitance and increasing the local implant depth increased the bulk effect.

6.2 Future Work

Stand-by current reduction should be the primary task for the next study. Higher stand-by current increases the off state power consumption. I_{OFF} reduction can be accomplished by reducing the punch through effect between source and drain. Also instead of double implantation at the channel to create p^+ pocket, new process techniques should be investigated to perform one dopant implantation. This can provide additional improvements at the mobility of electrons and resulted with higher trans-conductance. Also depletion type PMOS transistors can be designed like its NMOS counterpart. After modeling these devices we can implement them in the circuits. The basic circuit for this analysis can be an inverter. If any improvements are seen at the delay time and power consumptions, we can prove the success of these designs.

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APPENDIX A

MOS DEVICE GEOMETRY DEFINITIONS

A.1 Mesh Definition

Sample 2D MOS device mesh definition:

```
# definition of mesh in x-direction #
```

```
x.mesh loc=0      spac=0.05
x.mesh loc=0.155  spac=0.005
x.mesh loc=0.2    spac=0.005
x.mesh loc=0.265  spac=0.005
x.mesh loc=0.32   spac=0.01
x.mesh loc=0.375  spac=0.005
x.mesh loc=0.44   spac=0.005
x.mesh loc=0.485  spac=0.005
x.mesh loc=0.64   spac=0.05
```

```
# definition of mesh in y-direction #
```

```
y.mesh loc=-0.145 spac=0.05
y.mesh loc=-0.105 spac=0.03
y.mesh loc=-0.005 spac=0.0025
y.mesh loc=0      spac=0.0025
y.mesh loc=0.01   spac=0.0025
y.mesh loc=0.25   spac=0.01
y.mesh loc=0.5    spac=0.05
```

x.mesh specifies the location of grid lines along the x-axis.

y.mesh specifies the location of grid lines along the y-axis.

“loc” specifies the location of the grid line.

“spac” specifies the mesh spacing at the mesh location specified by the location parameter.

A.2 Definition of Materials for Regions

Sample 2D MOS device material and region definition:

```
# DEFINITION OF MATERIALS #

# oxide #
region number=1 material=Oxide      x.min=0 x.max=0.64
y.min=-0.145 y.max=0

# poly #
region number=2 material=Poly       x.min=0.265 x.max=0.375
y.min=-0.105 y.max=-0.005

# gate contact #
region number=3 material=aluminum x.min=0.265 x.max=0.375
y.min=-0.145 y.max=-0.105

# drain contact #
region number=4 material=aluminum x.min=0 x.max=0.155
y.min=-0.145 y.max=0.0

# source contact #
region number=4 material=aluminum x.min=0.485 x.max=0.64
y.min=-0.145 y.max=0.0

# substrate #
region number=5 material=Silicon  x.min=0 x.max=0.64
y.min=0 y.max=0.5
```

A.3 Design Geometries for MOSFETs

A.3.1 Mesh Definition

Mesh definition is important for simulation accuracy and time. Fine mesh gives accurate solution but increase simulation time. So optimizing the mesh grid is the important goal for MOSFET structures. Mesh should be refined in the key areas. These areas are:

- Around junctions and depletion regions
- Inversion regions
- Areas of high electric field
- Areas of current flow

Sample 2D MOS device mesh structure is shown in Figure A.1. Mesh is fine in the surface area, channel and junctions.

Figure A.1: MOSFET Mesh Structure

A.3.2 Definition of Materials for Regions

MOS devices have oxide, poly, gate contact, source contact, drain contact and the substrate regions. Region command specifies the location of materials in a previously defined mesh. Every triangle must be defined as a material. Figure A.2 illustrates the MOS structure's regions and the materials.

Figure A.2: Regions and Materials

A.3.3 Definition of Metal Contacts

Command electrode specifies the location and names of electrode in a previously defined mesh.

```
# definitions of metal contacts #
electrode name=gate    x.min=0.265    x.max=0.375 y.min=-
0.145 y.max=-0.105
electrode name=drain   x.min=0         x.max=0.155 y.min=-
0.145 y.max=0.0
```

```
electrode name=source x.min=0.485    x.max=0.64 y.min=-  
0.145 y.max=0.0  
electrode name=substrate bottom
```

Figure A.3 illustrates the contacts on the MOS structure.

Figure A.3: Contacts on Structure

A.3.4 Definitions of Dopings

Command doping specifies doping profiles either analytically or from an input file.

```
DEFINITIONS OF DOPING #
```

```
# poly doping #
```

```
doping uniform conc=1e20 n.type direction=y regions=2
```

```
# background concentration #
```

```
doping uniform p.type direction=y conc=1e15
```

```
# threshold doping #
```

```
doping gaussian p.type direction=y conc=2.85e17 start=0  
char=0.12 ratio.lateral=0.3
```

```
# LDD doping #
```

```
doping gaussian n.type direction=y conc=9e17 start=0  
char=0.041 x.left=0 x.right=0.255 ratio.lateral=0.3  
doping gaussian n.type direction=y conc=9e17 start=0  
char=0.041 x.left=0.385 x.right=0.64 ratio.lateral=0.3
```

```
# S/D doping #
```

```
doping gaussian n.type direction=y conc=1e20 start=0  
char=0.035 x.right=0.155 ratio.lateral=0.5  
doping gaussian n.type direction=y conc=1e20 start=0  
char=0.035 x.left=0.485 ratio.lateral=0.5
```

Figure A.4 illustrates the MOS structure's doping profile.

Figure A.4: Doping Profile

A.4 Solution Models and Methods

Command “models” specifies model flag to indicate the inclusion of various physical mechanisms, models, and other parameters such as the global temperature for the simulation.

A.4.1 Mobility Models

Electric field accelerates electrons and holes. But eventually they lose momentum as a result of various scattering processes. These scattering mechanisms are lattice vibrations (phonons), impurity ions, other carriers, surfaces, and other material imperfections. Therefore mobility is the functions of the local electric field, lattice temperature, doping concentration. Mobility modeling is divided into:

- i. Low field mobility
 - Constant low field mobility
 - Concentration-dependent low field mobility
 - Analytic low field mobility
 - Arora model for low field mobility
 - Carrier-carrier scattering model for low field mobility
 - Klassen’s unified low field mobility
- ii. Inversion layer mobility
 - Lombardi CVT Model
 - Extended CVT Model
 - Yamaguchi Model
 - The Tasch Model
- iii. Perpendicular Electric Field –Dependent Mobility
 - The Watt Model
 - Shirahata’s Mobilty Model
- iv. Parallel Electric Field-Dependent Mobility
- v. Carrier Temperature Dependent Mobility

A.4.2 Carrier Generation-Recombination Models

Carrier generation-recombination is the process through which the semiconductor material attempts to return to equilibrium after being disturbed from it.

The reasons that cause generation-recombination are:

- a. Phonon Transitions
- b. Photon Transitions
- c. Auger Transitions
- d. Surface Recombination
- e. Impact Ionization
- f. Tunneling

Models:

- i. Shockley-Read-Hall(SRH) Recombination Model
- ii. SRH Concentration-Dependent Lifetime Model
- iii. Klaassen's Concentration dependent Lifetime Model
- iv. Trap-Assisted tunneling
- v. Radiative Recombination(Photon generation)
- vi. Auger Recombination
 - 1. Standard Auger Model
 - 2. Klaassen's temperature-Dependent Auger Model
 - 3. Narrow Bandgap Auger model
- vii. Surface Recombination

A.4.3 Impact Ionization Models

In any space charge region with a sufficient high reverse bias, the electric field will be high enough to accelerate free carriers up to a point where they will have acquired sufficient energy to generate more free carriers when in collision with the atoms of the crystal. To acquire sufficient energy these conditions must be met. The electric field must be sufficiently high, and then the distance between the collisions of the free carrier must be enough to allow acceleration to sufficiently high velocity. If the generation rate of these free carriers is sufficiently high this process will eventually lead to avalanche breakdown.

The models are:

- i. Local electric field Models for Impact Ionization
 - 1. Selberherr's Impact Ionization Model
 - 2. Valdinoci Impact Ionization Model
 - 3. Grant's Impact Ionization Model
- ii. Non-Local Carrier Energy Models for Impact Ionization

1. Concannon's Impact Ionization
2. Band-to-Band Tunneling

A.4.4 Gate Current Models

The conductance of the insulating film would ideally be considered as zero. But, for the sub 0.5 μm generation of MOS devices there is now considerable conductance being measured on the gate contacts. The negative side of this gate current is responsible for the degradation in device operating characteristics with the time.

The models are:

- i. Fowler-Nordheim Tunneling
- ii. Lucky Electron Hot Carrier Injection Model
- iii. Concannon's Injection Model

A.4.5 Fermi-Dirac and Boltzmann Statistics

The system includes tremendous number of electrons and it is hopeless task to follow the instantaneous behavior of each electron. Therefore statistical approaches are applied try to determine the average behavior of the system.

A.4.6 Bandgap Narrowing

As the doping level increases, a decrease in the bandgap separation occurs, where the conduction band is lowered by approximately the same amount as the valence band is raised.

A.4.7 Solution Methods

- i. Numerical Methods
 - 1) Newton's method
 - 2) Gummel's Method
 - 3) Discretization
 - 4) Continuation Method
- ii. Electrical analyses
 - 1) Dc Analysis
 - 2) Transient analysis
 - 3) Small-Signal Analysis
 - 4) Impact ionization analysis
 - 5) Gate current analysis

A.4.8 Models Used in This Study

SRH :Shockley-Read Hall two carrier recombination. Based on fixed lifetimes

FERMI: Fermi-Dirac statistics. High concentration effects

CVT: Mobility model. Integrated models

BGN: Band Gap Narrowing. Important in heavily doped regions and critical for bipolar simulation.

AUGER:Auger three carrier recombination. Significant when carrier concentration high

Impact SELBER: Impact ionization Selberrherr's Model. Require for any sort of breakdown voltage simulation

Sample commands for models:

```
# set material models #

MODELS SRH FERMI CVT BGN AUGER
#
impact      selber an1=703000 an2=703000 bn1=1.231e+06
bn2=1.231e+06 \
  ap1=671000 ap2=1.582e+06 bp1=1.693e+06 bp2=2.036e+06
betan=1 betap=1 \
egran=400000
#
mobility  bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000
cp.cvt=884200 \
taun.cvt=0.125 taup.cvt=0.0317 gamn.cvt=2.5 gamp.cvt=2.2 \
mu0n.cvt=52.2 mu0p.cvt=44.9 mu1n.cvt=43.4 mu1p.cvt=29
mumaxn.cvt=1417 \
mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17
csn.cvt=3.43e+20 \
csp.cvt=6.1e+20 alphn.cvt=0.68 alphp.cvt=0.71 betan.cvt=2
betap.cvt=2 \
pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14
delp.cvt=2.0546e+14
```

A.4.9 Major Commands for Solutions and Analysis

Command “solve” instructs Atlas to perform a solution for one or more specified bias points.

Command “load” loads previous solution from files as initial guesses to other bias points.

Command “log” allows all terminal characteristics of a run to be saved to a file.

Command “extract” is used to measure parameters from both log and solution files.

Command “tonyplot” starts the graphical post-processor Tonyplot. In this sample two different solutions are graphed on the same screen.

Sample usage of the solution commands:

```
solve init
SOLVE VGATE=0.05 OUTF=solve_tmp10
SOLVE VGATE=1.5 OUTF=solve_tmp11

LOAD INFILE=solve_tmp10
LOG OUTFILE=CONDEV_1.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1.5 VSTEP=0.03

LOAD INFILE=solve_tmp11
LOG OUTFILE=CONDEV_2.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1.5 VSTEP=0.03

extract name="idsmax" max(abs(i."drain"))

tonyplot -overlay -st CONDEV_1.log CONDEV_2.log -set
CONDEV_1.set
```

APPENDIX B

SIMULATIONS' RESULTS

B.1 Conventional Device Profiles

Figure B.1 illustrates the conventional device channel Gaussian doping profile.

Figure B.1: 1 μ m Conventional Device Vertical Channel Profile

In Athena several simulations are run to find exact channel doping profile.
Sample Athena input deck for boron implantation energy and dose is below.

```
go athena
# Definition of Mesh
line x loc=0.00 spac=0.05
line x loc=0.18 spac=0.005
line x loc=0.35 spac=0.005
line x loc=0.41 spac=0.01
line x loc=0.47 spac=0.005
line x loc=0.64 spac=0.005
line x loc=0.82 spac=0.05

line y loc=0.00 spac=0.0025
line y loc=0.01 spac=0.0025
line y loc=0.25 spac=0.01
line y loc=0.5 spac=0.05

# Substrate definition
init silicon c.boron=1.0e15 orientation=100 two.d

deposit oxide thick=0.02
# P channel doping
implant boron dose=5e12 energy=8 tilt=0 rotation=0 crystal
lat.ratio1=5.0 \
    lat.ratio2=5.0
diffus time=13 temp=800 weto2 press=1.00 hcl.pc=0
# Activation annealing
diffus time=30 temp=980 nitro press=1.00
tonyplot
quit
```

Figure B.2 shows the conventional device channel doping profile.

Figure B.2: 1 μ m Conventional Device Doping Profile

Figure B.3 shows I_D - V_G Curve for V_T Extraction.

Figure B.3: 0.1 μ m Conventional Device I_D - V_G Curve for V_T Extraction

Figure B.4 shows ID-VD curve.

Figure B.4: 0.1 μ m Conventional Device I_D - V_D Curve

Figure B.5 shows electric field contours for conventional device.

Figure B.5: 0.1 μm Conventional Device Electric Field Contour

Figure B.6 shows the potential contours.

Figure B.6: 0.1 μ m Conventional Device Potential Contour

Figure B.7 shows the stand-by current from I_D - V_D curve.

Figure B.7: 0.1 μ m Conventional Device I_{OFF}

Figure B.8 shows I_D - V_G curve for substrate leakage curve.

Figure B.8: 0.1 μm Conventional Device I_{SUB}

B.2 Enhanced Device

Figure B.9 shows enhanced device channel doping profile.

Figure B.9: 1 μm Enhanced Device Vertical Doping Profile

Figure B.10 shows enhanced device doping profile.

Figure B.10: 1μm Enhanced Device Doping Profile

Figure B.11 shows I_D - V_G curve for V_T extraction.

Figure B.11: The V_T for 0.1 μm Device

Sample solution part of bulk effect simulation deck is given below.

```
solve init
SOLVE VDRAIN=0.05
SOLVE Vsubstrate=-1      OUTF=solve_tmp12
LOAD INFILE=solve_tmp12
LOG OUTFILE=lddstr_3.log
SOLVE NAME=gate Vgate=0 VFINAL=1.5 VSTEP=0.03
extract
name="vt"(xintercept(maxslope(curve(abs(v."gate")),abs(i."drain")))) \- abs(ave(v."drain"))/2.0)
```

Sample solution part of sub-threshold slope deck for simulation is given below.

```
solve init
# Bias the drain
solve vdrain=0.05  outfile=solve_t2
# Ramp the gate
load infile=solve_t2
log outf=lddstr_2.log
solve name=gate vgate=0 vstep=0.005 vfinal=1
# plot results
tonyplot  lddstr_2.log  -set lddstr_1.set
```

Sample solution part of Idsmax deck for simulation is given below.

```
solve init
SOLVE VGATE=0.05 OUTF=solve_tmp10
SOLVE VGATE=1.5 OUTF=solve_tmp11
LOAD INFILE=solve_tmp10
LOG OUTFILE=lddstr_1.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1.5 VSTEP=0.03
LOAD INFILE=solve_tmp11
LOG OUTFILE=lddstr_2.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1.5 VSTEP=0.03
```

```
#Show E.FIELD Contour
output      e.field
save outf=lddstr_01.str
tonyplot lddstr_01.str
extract name="idsmax" max(abs(i."drain"))
```

Figure B.12 shows I_D - V_D curve for enhanced device.

Figure B.12: 0.1 μm Enhanced Device I_D - V_D Curve

Figure B.13 shows electric field contours for enhanced device.

Figure B.13: 0.1 μm Enhanced Device Electric Field Contour

Figure B.14 shows potential contours for enhanced device.

Figure B.14: 0.1 μm Enhanced Device Potential Contour

Sample solution part of I_{OFF} deck for simulation is given below.

```
solve init
SOLVE VGATE=0 OUTF=solve_tmp10
LOAD INFILE=solve_tmp10
LOG OUTFILE=lddstr_1.log
SOLVE NAME=drain VDRAIN=0 VFINAL=1.5 VSTEP=0.03
extract name="idsmax" max(abs(i."drain"))
```

Figure B.15 shows stand-by current.

Figure B.15: 0.1 μm Enhanced Device Standby Current

Sample solution part of I_{SUB} deck for simulation is given below.

```
solve init
# Bias the drain
solve vdrain=0.05 outfile=solve_t1
solve vdrain=1.5 outfile=solve_t2
# Ramp the gate
load infile=solve_t1
log outf=lddstr_1.log
solve name=gate vgate=0 vstep=0.1 vfinal=1.5
load infile=solve_t2
log outf=lddstr_2.log
solve name=gate vgate=0 vstep=0.1 vfinal=1.5
extract name="isubmax" max(abs(i."substrate"))
```

Figure B.16 shows substrate leakage current for enhanced device.

Figure B.16: 0.1 um Enhanced Device I_{SUB}

Sample solution part of C_J deck for simulation is given below.

```

solve init
solve vsource=0
solve vgate=1.5
solve vdrain=0.05  OUTF=solve_tmp10
solve vdrain=1.5  OUTF=solve_tmp11
LOAD INFILE=solve_tmp10
LOG OUTFILE=lddstr_1.log
SOLVE NAME=substrate Vsubstrate=0 VFINAL=-1.5 VSTEP=-0.03
ac freq=1e3
LOAD INFILE=solve_tmp11
LOG OUTFILE=lddstr_2.log
SOLVE NAME=substrate Vsubstrate=0 VFINAL=-1.5 VSTEP=-0.03
ac freq=1e3

```

Figure B.17 shows the capacitance change by changing substrate potential.

Figure B.17: Enhanced Device Substrate-Source Capacitance