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Design and analysis of direct-down conversion CMOS mixer

Maithil Pachchigar
San Jose State University

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DESIGN AND ANALYSIS OF DIRECT-DOWN CONVERSION CMOS MIXER

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

By

Maithil Pachchigar

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Maithil Pachchigar

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APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

Advisor

Dr. Sotoudeh Hamed-Hagh

Co-Advisor

Dr. Avtar Singh

Co-Advisor

Dr. Masoud Mostafavi

APPROVED FOR THE UNIVERSITY

Dean I. Williamson

ABSTRACT

DESIGN AND ANALYSIS OF DIRECT-DOWN CONVERSION CMOS MIXER

by Maithil Pachchigar

A nonlinear device that performs the frequency translation in the system is known as the mixer. In the receiver circuits, the mixers carry on the frequency translation by multiplying the high input radio frequency (RF) with a local oscillator (LO) input. This action is called the intermediate frequency (IF) down-conversion of the mixer.

The proposed integrated mixer circuit with wideband input matching network is implemented using Gilbert-cell topology to satisfy the UWB requirement and to achieve the highest overall performance.

The input RF signal frequency from 3.4GHz to 10GHz and the input LO signal frequency from 3.6GHz to 10.2GHz is applied to the mixer in order to achieve the 200MHz of down-converted IF signal frequency, which covers the entire ultra-wideband from 3.1 GHz to 10.6GHz. The simulation results of various mixer parameters are discussed and compared with the previous mixer design works.

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CHAPTER 1. INTRODUCTION

This chapter is about the Ultra-wide band (UWB) standard and its applications in modern era of the wireless communications. Section 1.1 introduces the UWB standard defined by Federal Communications Commission (FCC) and describes the brief summary of the UWB transceiver architecture; Section 1.2 discusses the UWB applications; Section 1.3 provides overview of the modern UWB receiver architecture. Section 1.4 discusses about the best available technology for the UWB mixer. Section 1.5 gives the overview of main objectives of the thesis.

1.1 Definition of UWB Standard

The UWB standard utilizes the unlicensed 3.1 – 10.6 GHz frequency band, as regulated in the United States by the Code of FCC under Title 47, Section 15. Table 1 shows the main five band groups in the UWB spectrum as regulated by FCC in USA and describes how each band group will be utilized. Figure 1 indicates these five band groups and each group are divided in 528MHz bands. The first generation devices for Wireless Personal Area Network (WPAN) applications utilize the first (3.1-4.9GHz) band group. The second (4.9-6 GHz), fourth and fifth (8.1-10.6 G Hz) band groups are for future applications. The third (6-8.1 GHz) band group is designated for the implementation of Wireless Local Area Network (WLAN) applications.

Figure 1: The UWB spectrum: 528 MHz bands – 5 groups of 2/3 bands each
(Modified from A. Silvennoinen (2004, Sept.))

The two fundamental approaches to utilize the UWB spectrum are: the single-band and the multi-band. The single band, high-speed and high-bit rate transmission spectrum utilizes the whole 3.1 to 10.6 GHz band, whereas the multi-band, moderate bit-rate and high-bit rate transmission spectrum breaks into 528MHz bands. The multi-band approach is grouped into the four different bands: band group 1, band group 2, band group 3, band groups 4 and 5 as shown in Table 1; at a limited transmit power of -41dBm/MHz. Consequently, the UWB standard offers an effective channel capacity at short range that limits the interference [1].

Table 1. The UWB band groups as regulated by FCC in USA

	Band Group 2	Band Group 3	Band Group 4, 5
3.1-4.9 GHz	4.9-6 GHz	6-8.1 GHz	8.1-10.6 GHz
First generation devices-WPAN applications	Future Use	WLAN applications	Future Use

The Orthogonal Frequency Division Multiplexing (OFDM) is one of the spread spectrum modulation techniques, which is used by the modern UWB systems to

occupy these extremely wide bandwidths. In the OFDM, the selected signals are amplitude modulated and multiplexed over a large number of orthogonally spaced carriers at precise frequencies. The use of multiple bands in combination with the OFDM modulation can offer significant merits to the traditional UWB systems. The combination of the broad UWB spectrum and low power improves the speed and reduces the interference with other wireless spectra [2].

The block diagram of the UWB transceiver is shown in Figure 2. The UWB transmitter incorporates the OFDM baseband transmission with 128 sub-carriers and the Radio Frequency (RF) section to up-convert the incoming data. The popular OFDM baseband technique in the UWB transceiver offers the flexibility of using the simple DSP algorithms for multi-path transmission in the broadband applications.

The OFDM baseband transmission generates the Inverse Fast Fourier Transform (IFFT) of the incoming data and the Digital-to-Analog Converter (DAC) converts this incoming digital data into the analog domain. The UWB transmitter design has the main challenge of achieving a tunable, flat gain response over a wide bandwidth.

The antennas utilized in the UWB transceiver system must be of small size and omni-directional in order to achieve the best performance. The UWB receiver consists of RF section and the OFDM baseband for the digital back-end processing. A modulated signal is received by the RF section where it is filtered, amplified, and downconverted to a baseband signal. In the OFDM baseband, the high-speed Analog-to-Digital Converter (ADC) samples the output of the RF section. Once

digitized, the demodulator performs the Fast Fourier Transform (FFT) in order to extract the bit stream in the digital domain.

Figure 2. The UWB transceiver block diagram

1.2 The UWB Applications

The UWB applications incorporate Wireless Personal Area Network (WPAN), Wireless Local Area Network (WLAN), and other Wide Area Networks that are intended for prospective short-range radio transmissions. The UWB applications along with various wireless network topologies in terms of their typical network ranges are shown in Figure 3. The UWB standard provides a WPAN with data payload communication capabilities of 53.3, 55, 80, 106.67, 110, 160, 200, 320, and 480 Mb/s.

Figure 3. WPAN and WLAN and their typical ranges
(Modified from A. Silvennoinen (2004, Sept.))

The increasing number of multi-media and entertainment-profound devices in the home such as digital camcorders and cameras, High-Definition TeleVisions (HDTVs), Personal Computers (PCs), and portable gaming devices require a high-resolution-bandwidth wireless solution for easy connectivity and exchange of data as shown in Figure 4. The UWB standard offers the required distinctive cost-effective, power-efficient, and high-resolution-bandwidth wireless solution for the exchange of data within 10 meters of short range.

The UWB standard will probably be the most promising in WPAN applications due to higher data throughput capability, short-range, and lower power dissipation characteristics. The key application areas that will benefit from the UWB standard will be the PC peripherals, portable consumer electronics, and communications.

Figure 4. The typical UWB applications

1.3 The UWB Receiver Front-end Architecture

The UWB receiver interprets the billions of pulses into data by tuning in for an associate pulse sequence sent by the typical UWB transmitter. The popular RF receiver topologies utilized in the communication industry are single super-heterodyne, double super-heterodyne, direct-conversion or Zero Intermediate Frequency (ZIF), low-IF, and digital-IF. There are several criteria that decide which receiver architecture is well suited for the UWB applications. The single and double super-heterodyne receivers require the RF front-end filter for the image rejection although they have good sensitivity and large signal handling capability. In direct-conversion receiver (DCR) architecture, the incoming RF frequency is mixed with an

input Local Oscillator (LO) frequency that is equal to the carrier frequency and thus IF is equal to zero. For this reason, this architecture is known as ZIF or DCR. The DCR architecture offers a number of advantages due to its simplicity, the possibility of a monolithic integration as well as the lack of image related problems, well proven and reliable in terms of sensitivity and selectivity. Superior integration means that no external IF filters are needed. Other resulting qualities are lower power dissipation, lower chip area, and production costs making DCR a suitable choice for the UWB systems. The Low-IF receivers offer almost similar advantages as DCR and they are utilized in the handset applications. The versatile digital-IF receivers are used in the military applications; however they require large chip area and consume high current.

The DCR architecture has also some demerits, apart from the already mentioned merits. First of all, because of direct-conversion, the second order intermodulation (IM) requirement for the receiver is high. Second, the analog modules running at high frequencies suffer from LO leakage and DC offsets. Also, the active filters have to be used, because the low insertion loss passive filters are not available at the baseband and this could create the receiver noise.

The typical UWB receiver front-end, realized by the DCR architecture, block incorporates the Low Noise Amplifier (LNA), the down converted mixer and the IF filter as shown in Figure 5. The LNA amplifies the RF input signal and it is fed to the RF port of the mixer and hence the RF port must exhibit sufficiently high linearity as the LNA also amplifies the nearby interferers and produces the strong intermodulation products.

Figure 5. The typical UWB receiver front-end block diagram

The UWB LNA generally utilizes the two-stage input-matching network with cascade devices to increase the isolation. The UWB LNA should have high voltage gain of about more than 15dB and low noise of about less than 6 dB. The UWB mixer down-converts the RF signal to the IF signal. The UWB mixer must consume low power and should cover the whole UWB range with the highest linearity. The IF filter, which is followed by the UWB mixer, only allows the fundamental IF to pass and filters the other harmonic components. The UWB receiver design simultaneously requires a low noise with a wide bandwidth and a very high linearity because of large amount of interferences may exist close to the used frequency band. The amount of filtering required is determined by the total amount of interference present. This thesis focuses on the design and analysis of the UWB mixer because it is an important and challenging part of the UWB receiver front-end.

1.4 Choice of Technology

The UWB mixer design is done using the 0.18 μm Complementary Metal Oxide Semiconductor (CMOS) by the Taiwan Semiconductor Manufacturing Company (TSMC) technology. This technology is available to the University through Metal Oxide Semiconductor Implementation Service (MOSIS). In general, the RF circuits are implemented either using CMOS or Silicon Germanium (SiGe) processes. The CMOS process is chosen for this thesis because of the low power and the easy availability whereas the SiGe process is more expensive and consumes more power compared to the CMOS process. Some of the TSMC 0.18 μm CMOS technology process parameters from the MOSIS service are provided for the reference in Table 2.

Table 2. The TSMC technology process parameters from MOSIS Service

No. Of Metal Layers	Supply Voltage (V)	f_t of Transistor (GHz)	Metal 6 Thickness (μm)	Substrate to Metal 6 Distance (μm)
6	1.8	40	0.99	5

The transition frequency of the transistor (f_t) shows the frequency ability of the transistor where the gain of the transistor falls to unity when used as an amplifier. The value of f_t can be improved by operating transistor at high values of the difference between the gate-to-source voltage (V_{gs}) and threshold voltage (V_t) of the transistor. The TSMC 0.18 μm CMOS technology has 6 metal layers and 1 polysilicon layer. This process is designed for 1.8V low voltage and high-speed applications. The metal 6 is needed to realize high quality inductors using this

process.

1.5 Objectives

This thesis mainly focuses on the all five band groups (3.432GHz to 10.296GHz) as shown in Figure 1 for the mixer design and its performance. The main challenges in the UWB system design are to realize a wideband mixer to work at the RF and baseband while exhibiting low noise figures and high linearity. This thesis should achieve the specifications listed in Table 3 [3, 4, 5, and 6]. These specifications are based on the past works of mixer design for the UWB receiver.

Table 3. A Typical UWB receiver front-end specification

Operating Frequency (GHz)	Conversion Gain (dB)	Noise Figure (dB)	Input Referred 1-dB Compression Point (dBm)	IIP3 (dBm)
>15	>15	<10	-15 to 5	-10 to 5

Chapter 2 of the thesis starts with mixer theory fundamentals and talks about different mixer types along with important mixer specifications. Chapter 3 starts with the proposed mixer schematic design and simulation results, along with the inductor design analysis, and eventually discusses the layout issues, and the post-layout simulation results achieved using the TSMC 0.18 μ m CMOS technology. Chapter 4 concludes the thesis and summarizes the results and compares them with results reported by the past works.

CHAPTER 2. MIXER THEORY AND SPECIFICATIONS

In this chapter, Section 2.1 describes the mixer theory fundamentals. Section 2.2 explains the various types of mixer and their trade-offs. Section 2.3 leads to the detail description of the mixer specifications. Section 2.4 discusses some performance parameters that the UWB receiver must achieve.

2.1 Mixer Fundamentals

A device that performs the frequency translation in the communication system is called the mixer. The mixers are utilized in almost every wireless system. In the receiver circuits, the basic mixers carry on the frequency translation by multiplying the RF input signal with a LO input signal to produce the IF output signal as shown in Figure 6. The mixer conversion action can also be described by the following equation:

$$O_{IF} = \pm I_{RF} \pm I_{LO} \quad (\text{Eq. 1})$$

Where O_{IF} is the output intermediate frequency signal at the IF port, I_{RF} is the input RF signal at the RF port, and I_{LO} is the input LO signal at the LO port of the mixer [7].

Figure 6. The basic symbol of three-port mixer

The mixer is a linear, time-variant system with respect to RF port and a non-linear, time-variant system with respect to the LO port. Ideally, the amplitude and phase of the mixer output signal should be independent of the LO signal characteristics, and proportional to the amplitude, and phase of the RF input signal. If the RF signals arriving at RF input port have high enough power level, the RF filters preceding the mixer do not need to offer a significant sensitivity to avoid the additional intermodulation products.

2.2 Mixer Types

An integrated RF mixer is a significant block of the modern wireless communication systems. The analysis of an integrated mixer is essential in order to understand the performance tradeoffs and define a figure of merit to fully characterize the performance of the mixers.

The mixer can be grouped into the two categories: a). passive and b). active. The passive diode mixer is commonly available because of low price and easier to design. The passive mixer consumes the lowest power and operates at high linearity. It also has some disadvantages such as relatively high noise figure, sensitivity of each port of the mixer to the reactive terminations, requirement of well-matched diodes, the LO to RF feedthrough, and the requirement of the high LO drive [8]. The double balanced mixer has higher port-to-port isolation, lower spurious outputs, and higher common-mode noise rejection. The generic block diagram of a double balanced passive diode mixer is shown in Figure 7. The diodes operate as high-speed switches in this

configuration, where the LO signal is mixed with the RF signal to produce the IF signal.

Figure 7. Generic double balanced diode mixer

The active mixer includes the transistor-level structure. The most popular active mixer in today's RF industry is Gilbert-cell structure. The Gilbert-cell mixer utilizes the differential pair structure and essentially the transconductance of the mixer helps to transfer the input RF signal to a current signal. The active mixer has some disadvantages such as high power consumption and requirement for the LO buffer. The active mixers can be classified in two categories: 1. single balanced mixer, and 2. double balanced mixer.

2.2.1 The Single Balanced Mixer

The single balanced mixer only requires a single-ended RF input signal for ease of operation and it does not need a balun transformer at the input of the mixer. The differential LO signal applied to switching transistors M1 and M2 mixes with an input RF signal to produce an IF output signal. This type of mixer offers good

voltage conversion gain and low noise. This kind of mixer has the disadvantage of high LO to IF feedthrough. Figure 8 shows that the incoming RF signal mixes with the LO signal to produce an IF output signal waveform. The LO is a large symmetrical signal turning on/off the differential source-coupled transistors. Several harmonics of the LO produces the spurious frequencies by mixing with the input RF signal. Therefore, the differential output is preferred to provide large immunity to the mixer feedthrough and high conversion gain.

Figure 8. The single balanced mixer topology and its waveforms

2.2.2 The Double Balanced Mixer

The double balanced mixer is also known as the Gilbert-cell mixer. This fully differential mixer carries out the voltage to current conversion of the RF input signal that can be modified by the LO input signal as shown in Figure 9. The LO signal is

applied to the switching transistors M1, M2, M3, and M4, and input RF signal is applied to M5 and M6. The IF output signal is taken from the drains of M1 and M4. The merits of this architecture are the good conversion gain without addition of much noise and suppressing unwanted frequency components at the output. Because of the fully differential topology, this type of mixer reduces the amount of even order distortions and provides high isolation between the LO, RF, and IF ports of the mixer.

The conversion gain of this mixer can help to boost the overall UWB receiver gain when the LNA gain is not enough. For this type of mixer, the flicker noise could be significant from the switching action of the LO pair. One possible solution to improve linearity and noise of this mixer is to increase the value of the drain-to-source saturation voltage ($V_{DS(Sat)}$) of the transistor and decrease the channel length of the transistors.

Figure 9. The double balanced Gilbert-Cell mixer topology

2.3 Mixer Specifications

Some important mixer specifications helpful to better characterize the mixer performance include Noise Figure (NF), Third-order Input Intercept Point (IIP3), 1-dB Power compression point (P1-dB), voltage conversion gain, and RF port-to-IF port isolation.

2.3.1 Noise

In general, the noise is defined as any unwanted signal intervenes with the lucidity and intelligibility of desired signals. From the mixer point of view, there are two main frequencies that contribute to the IF output signal, the desired RF signal, and the undesired image (IM) signal. The noise figure is referred to as the single-sideband noise Figure (SSB NF) if one only considers the desired RF signal information. As the SSB has signal power in only one sideband and both measures contribute the same amount of IF frequency noise, generally the SSB NF will amount about 3dB more than that of the Double Sideband Noise Figure (DSB NF).

The measure of noise figure (NF) is the noise contributed by the device in the overall system noise. The input noise corruption relative to the output noise corruption is defined as the noise factor (F), and the decibel measurement of F is known as the NF. The system noise figure determines the minimum detectable signal or the sensitivity of the receiver. In the systems with multiple stages, the overall noise figure depends upon the NF and gain of each block. Noise factor is the linear version of the noise figure. The noise figure in terms of noise factor can be defined

as:

$$NF = 10 * \log (F) \quad (\text{Eq. 2})$$

2.3.2 Linearity

When the two different frequency signals are applied to a non-linear system, the output in general exhibits some components other than the harmonics of input frequencies; this action is defined as the Inter-Modulation (IM). The frequency relationship in a two-tone IM measurement is shown in Figure 10. The IIP3 is the IM measure in the system and it impacts the receiver-blocking performance. The signal handling capability of the mixer is determined by the IIP3. Specifically, the IIP3 offers the levels of third order products a mixer is likely to produce under the multi-tone excitation.

Figure 10. The frequency harmonics

The IIP3 is measured by applying the two closely spaced input tones at frequencies f_1 and f_2 . The third order products from the mixing of these tones with the LO frequency would be at frequencies: $(2f_1 \pm f_2) \pm f_{LO}$ and $(2f_2 \pm f_1) \pm f_{LO}$. The IIP3 products of most interest for the down-converted mixer are $(2f_1 - f_2) - f_{LO}$ and $(2f_2 - f_1) - f_{LO}$. The IM product distortion can be calculated by the relative magnitude of these tones. Figure 11 depicts the IF output spectrum of the down-converted mixer under the two-tone excitation. As a good rule-of-thumb, the IIP3 is estimated about 10 to 15 dB higher than the P1-dB. The third order product becomes as large as the direct down-converted product at an imaginary IIP3 point. The rate of increase of the input signal level and the fundamental output level is at the one third of those third order products.

Within the mixer output pass band, some of the spurious mixer products exist and the third and higher order distortion characteristics produce many of these additional spurious outputs. This phenomenon is defined as 1-dB compression point (P1-dB) of the input signal level that causes the small signal gain drops by 1 dB. The spurious-free dynamic range (SFDR) is described as the ratio where the input power level is characterized by the intersection of the minimally existed signal and the IM3 term. The SFDR is used to quantify the overall usable range of the mixer for a wide variety of the signal strengths. The output of the RF receiver starts to saturate for sufficiently high input levels and noise dominates below this dynamic range.

Figure 11. The graphical definitions of P1-dB, IIP3 and OIP3

2.3.3 Conversion Gain

The frequency translating or converting action of a mixer is characterized by conversion gain or loss. The ratio of the Root Mean Square (RMS) voltages of the IF output signal and RF input signal is the voltage conversion gain. The mixer design requires the maximum voltage gain rather than the power match and the lowest power dissipation. The same equipment set-up and measurement method are used to measure the conversion gain of the mixer as those used to measure the gain of an amplifier. The conversion gain lowers the noise impact of the following stages. The active mixer recovers the loss of gain from impedance transformation.

2.3.4 Isolation

The amount of power coupled from one port to the next port of the mixer is measured by the isolation between the ports of the mixer. The two most popular isolation measurements are the LO-to-IF isolation and the LO-to-RF isolation as shown in Figure 12. The LO-to-IF isolation indicates how much LO power leaks through the IF output port due to the parasitic capacitance and the power supply coupling, which is known as the LO feedthrough. The LO-to-RF isolation indicates how much LO power leaks through the RF input port only due to the parasitic capacitance, which is known as the reverse LO feedthrough. The mixer always need minimum interaction between the RF, IF, and LO ports and therefore, the sensitivity to process and the temperature variations must also be considered.

It is more difficult to suppress the interaction at the RF port because of wide separation between the two frequencies. A low pass filter can easily attenuate the IF output appearing at the LO port. If the mixer is used as the first down-converter in the wireless receiver, then reverse LO leakage through the RF port generally results in a re-radiation through the antenna.

Figure 12. The mixer isolation

2.4 Typical Specifications Range of the UWB Mixer

The following Table 4 shows the typical mixer specification for UWB systems. In this thesis, the mixer is targeted to achieve performance parameters in this specification range. This specification range is derived based on the data collected from the previous UWB mixer designs [3, 4, 5, and 6].

Table 4. The typical specifications range of the UWB mixer

Noise Figure (dB)	IIP3 (dBm)	Conversion Gain (dB)	1-dB Compression point (dB)	Power Consumption (mW)
<15	-15 to 0	>10	-10 to 5	<15

For an ideal UWB mixer, the noise figure must be less than 15dB, and the conversion gain must be greater than 10dB with less than 15 mW of power consumption. The noise figure number is very challenging to achieve for the UWB mixer as it operates over a wide frequency range. The detailed analysis and the simulation of these parameters will be discussed in Chapter 3.

CHAPTER 3. MIXER DESIGN

In this chapter, Section 3.1 describes the proposed mixer schematic and the simulation results conducted by the Cadence tool using TSMC 0.18 μ m CMOS technology. Section 3.2 presents the inductor analysis and the simulation results. Section 3.3 presents the mixer layout and the post-layout simulation results.

3.1 Proposed Mixer Design and Analysis

The CMOS process is chosen for this thesis because of low power dissipation and low cost. The TSMC 0.18 μ m CMOS technology has 6 metal layers and 1 poly-silicon layer. This process is designed for 1.8V low voltage applications and yields a unity gain cut-off frequency of about 40GHz suitable for high-speed applications. This mixer designed with this technology can be utilized for low voltage and low noise wireless applications such as UWB receiver front-end.

This section describes the operation of the proposed mixer and presents the simulation results for the 1-dB power compression point (P1-dB), third order input intercept point (IIP3), noise figure (NF), and voltage conversion gain of the mixer.

3.1.1 Operation of the Proposed Mixer

The proposed mixer utilizes the traditional Gilbert-cell topology with the degenerative inductors in the driver stage. The fundamental of mixing relies on the multiplication of two signals, the differential LO input signal (LO+ and LO-), and the

differential RF input signal (RF+ and RF-) as described in Chapter 2. The RF driver stage (the combination of the transistors M5 and M6) amplifies the voltage of the RF signal and converts it into the current. The LO signal is used to steer all of the current from one transistor to the other at the LO differential switching stage (the combination of the transistors M1, M2, M3, and M4). The LO input signal applied to the mixer is generally selected to be a square-wave signal to improve the noise performance in the real mixer implementations. However, the sinusoidal LO signal is utilized in the simulations because the sinusoidal signal at high frequencies closely resembles the square-wave signal with the very steep slope. Furthermore, the realization of the RF square-wave signal is very hard to achieve.

The currents of the load resistors R1 and R2 create the differential IF output voltage (IF+ and IF-). The transistors M7 and M8 form the current mirror. Therefore, all the tail current goes through the transistor M7. The simplified version of proposed mixer without including the parallel transistors and the high frequency model of the inductors is shown in Figure 13.

$$(p \cos w_1 t)^*(q \cos w_2 t) = pq/2 [\cos(w_1 + w_2)t + \cos(w_1 - w_2)t] \quad (\text{Eq. 3})$$
$$V_{GS} \geq V_{TH} \quad \text{and} \quad V_{TH} \geq V_{GS} - V_{TH} \quad (\text{Eq. 4})$$

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To satisfy the wide-bandwidth input characteristics and to match the input impedance of the mixer, the additional passive components including L_s , L , and R_{bias} are being utilized in this design. The degenerative source inductors L_s are utilized in this design to achieve the high linearity. The dc bias current of M5 and M6 sink to the ground by means of low resistance path presented by the inductors L_s , and hence the inductor L_s avoids the dc voltage drop across the current source. The inductors L_s also help to increase the IIP3 and to improve the conversion gain. The series inductors L help to boost the conversion gain as well as reduce the overall noise. The combination of L_s with L makes the wideband input-matching network and matches with RF input resistance of $50\ \Omega$. This mixer is designed to achieve the ultra-wide-bandwidth of about 7.5GHz in the frequency range of 3.1GHz to 10.6GHz. The Gilbert-cell architecture is essentially a narrowband design; however, in this design, the degenerative and input series inductors with combination of bias resistors help to boost the operating bandwidth of the mixer. The component values of the mixer schematic are shown in Table 5.

Table 5. The component values of the mixer circuit

M1- M4,M7,M8: W/L	15.03 μ m/180nm
M5-M6: W/L Ratio	60 μ m/180nm
Load Resistors- R1, R2	500 Ω
Bias Resistors- Rbias1,	1.4K Ω
Source Inductors- Ls	3 nH
Series Inductors- L	3 nH

The test bench of the mixer to simulate the transient response and the Discrete Fourier Transform (DFT) output spectrum are shown in Figure 14. The four input ports are connected to the differential LO input and differential RF input respectively. Figure 15(a) shows the differential LO and differential RF input signals applied to the mixer, and Figure 15(b) shows the simulated differential IF output signal of the mixer. The DFT output spectrum of the mixer shows the 200MHz down converted frequency, second order harmonic distortion (HD2), and third order harmonic distortion (HD3) as shown in Figure 16.

Figure 14. The mixer circuit test bench setup in Cadence schematic composer editor

Figure 15 (a) Differential Input Transient Response

Figure 15 (b). Differential IF Output Transient Response

Figure 16. The mixer DFT output spectrum

3.1.2 The P1-dB Simulation

The P1-dB is the measure of the linearity of the mixer as already discussed in Chapter 2. The degenerative inductors (L_s) help to boost the P1-dB. This section shows how P1-dB is actually simulated using the Swept Periodic Steady State Response (SPSS) analysis in Cadence analog affirm environment.

The prf variable in PSS analysis is linearly swept from -30 to 5 dBm with 10 steps. By selecting the differential output IF nets in the test bench, the input referred 1-dB compression and the 1st Order harmonics can be plotted as shown in Figure 17. In this thesis, the P-1dB of the mixer was found in the range of -11.36 dBm to 1.41

dBm for the RF frequency range of 3.4 GHz to 10GHz. Please refer to first section of Appendix (A.1) for detailed description of the SPSS simulation approach.

Figure 17. The mixer P1-dB for frf=10GHz

3.1.3 The IIP3 Simulation

The IIP3 is utilized to analyze the effect of the frequency spacing between the two RF inputs on the mixer linearity. The combination of L_S and L help to improve the linearity of the mixer and hence the IIP3. The spacing of the two tones is selected to be 20MHz away from the 200MHz tone of the down converted signal. Therefore, the tones frequencies are selected to be 180MHz and 220MHz. Because of the mixer non-linearity, the 3rd order and the 1st order harmonics of 220MHz, and 180MHz will be produced respectively at the output of the mixer. As the LO input mixes with the

RF input and the power level of RF input signal is swept, it produces the IIP3 plot as shown in Figure 18. This IIP3 plot shows that the intersection of fundamental power and intermodulation (IM) term yields IIP3 of -12.11 dBm at the input RF power of -9dBm at the 10GHz of RF frequency. Please refer to Appendix A.2 for further details regarding simulating IIP3.

Figure 18. The mixer Input Referred IP3 point for frf = 10GHz

3.1.4 The Noise Figure Simulation

The current switching in transistors (M1-M4 and M5-M6) produces the noise at the output of the mixer, and this noise depends on the total capacitance seen at the

source of each transistor in the circuit. The noise at the output of the mixer dominates at higher frequencies and degrades the linearity of the mixer. To reduce the effect of capacitance and to improve the transconductance (g_m) in the mixer design, the source degenerative inductors L_s have been utilized in this design. As L_s offers the low impedance path, they help increasing the bias current through the transconductance stage, and hence improving the g_m without actually increasing the current of the switching transistors (M1-M4). The SSB and DSB noise figures are simulated using PSS and Pnoise analyses as shown in Figure 19 and 20 respectively. Please refer to Appendix A.3 for further detailed description of the noise simulation approach.

Figure 19. The mixer SSB noise Figure for frf = 10GHz

Figure 20. The mixer DSB noise Figure (NFdsb) for frf=10GHz

3.1.5 The Voltage Conversion Gain Simulation

The voltage conversion gain of the mixer from transistors M5 and M6 is given by the following equation [5]:

$$A_v = (2/\pi) * g_m * R_1 \quad (\text{Eq. 5})$$

From the above equation, the voltage conversion gain depends on the load resistors (R_1 or R_2) and the transconductance (g_m) of the transistors (M5 and M6). Therefore, the voltage conversion gain is improved in this work by optimizing the g_m and R_1 or R_2 , and increasing the bias current through the transconductance stage so that the mixer dissipates the minimum power. The PSS and the Periodic Transfer Function (PXF) analysis are utilized to simulate the voltage conversion gain of the

mixer. The PXF analysis is implemented by linearly sweeping the frequency from 1MHz to 200MHz, and the voltage conversion gain is plotted by selecting the differential IF output of the mixer. The simulated conversion gain of 18.13dB is achieved for the 10GHz of the input RF frequency as shown in Figure 21. Please refer to Appendix A.4 for further detailed description to simulate the conversion gain.

Figure 21. The mixer voltage conversion gain for frf = 10 GHz

The mixer performance specifications achieved from the schematic simulation in Cadence are shown in Table 6. As discussed before in Section 2.4, this simulated mixer specifications fairly satisfy the UWB mixer requirements. The simulated IIP3

for this mixer ranges from -6.03dBm to -12.11dBm in the UWB frequency range that satisfy the -15dBm to 0dBm range of the UWB mixer. The simulated conversion gain ranges from about 18.13 dB to 23.68 dB in the UWB frequency range that satisfies the greater than 15dB of conversion gain requirement for the UWB mixer. The noise requirement for the UWB mixer is less than 15dB, which closely meet with simulated SSB noise figure range from 11.30dB to 16.75 dB in the UWB frequency range. The simulated P1-dB also fulfils the UWB mixer range of -10dBm to 5dBm as shown in Table 6 below.

Table 6. The mixer performance specifications

Parameters	Simulation Specifications												
RF (GHz)	3.4	4	4.4	5	5.8	6.4	7	7.4	8	8.4	9	9.4	10
LO (GHz)	3.6	4.2	4.6	5.2	6	6.6	7.2	7.6	8.2	8.6	9.2	9.6	10.2
Input IP3 (dBm)	-6.03	-6.73	-7.93	-8.96	-8.39	-11.54	-9.25	-10.52	-8.59	-7.31	-9.34	-10.65	-12.11
Conversion Gain (dB)	19.30	23.7	23.68	22.32	21.45	21.45	21.75	22	22.15	21.95	21	19.98	18.13
SSB NF (dB)	11.30	10.46	10.65	11.24	11.60	11.82	11.63	12.02	12.31	12.5	13.65	14.90	16.75
DSB NF (dB)	9.03	7.49	7.84	8.33	8.61	8.69	8.68	8.98	9.45	9.91	11.24	12.46	14.33
P1-dB (dBm)	-11.36	-11.33	-11.01	-10.53	-3.11	-4.68	-5.21	-5.26	-4.48	-3.17	-1.78	1.28	1.41

3.2 On-Chip Inductor Design and Simulation Results

The mixer uses L_s and L inductors, which play a significant role in the design performance of the mixer as discussed earlier. This section discusses the design and the analysis of on-chip planar inductors. This section defines the essential inductor parameters, and summarizes the design and the optimization of on-chip planar inductors.

Figure 21 shows the planar inductor- Π model. From this model, L defines the nominal inductance and R_s defines the series resistance. The sheet resistance of metal layer can be used only for calculating the DC resistance of the planar. The effective resistance of the planar inductor increases at higher frequencies because of the skin effect and the Eddy current effect. The skin effect is caused by the majority of the current flow near the surface of the inductor rather than its core. The Eddy current is caused by the induced current flow into the lossy substrate. The series capacitance (C_s) results from the spacing capacitor distributed along the inductor turns and the capacitance between the planar and the metal under-pass. Ideally, the adjacent turns are almost equipotential, so the effect of the interturn fringing capacitance can be neglected. However, there is a relatively large potential difference between the planar and the center-tap underpass, making this overlap capacitor considerable. The oxide capacitance C_{ox} presents the parasitic capacitor between the substrate and inductor. The R_{si} and C_{si} represent the substrate resistance and capacitance of the silicon, respectively, as shown in the inductor- Π model. [9].

Figure 22. The planar inductor-II model

The performance of an inductor is known as the Quality factor (Q), which is expressed as:

$$Q = 2\pi * \frac{\text{Energy Stored}}{\text{Energy Loss in one Oscillation Cycle}} \quad (\text{Eq. 6})$$

Where, the energy stored is the difference between the peak magnetic energy $E_{\text{peak (magnetic)}}$ and the peak electric energy stored in any parasitic capacitances $E_{\text{peak (electric)}}$. At the higher frequencies, the energy dissipation occurs in the silicon substrate, which degrades the inductor quality factor and hence this frequency is known as the self-resonance frequency of an inductor. The self-resonance of an inductor is moved to higher frequencies by increasing the metal thickness. The thick oxide inductor is implemented to isolate the inductor from lossy substrate and improve the self-resonance frequency.

The planar inductor layout is implemented using RF Momentum tool of Advanced Design Systems (ADS). This planar inductor has 5 numbers of turns, 120 μm of outer diameter, 2.4 μm of width, and 0.2 μm of spacing between each turn as listed in Table 7.

Table 7. The inductor layout specifications

Width (μm)	Spacing (μm)	No of Turns	Outer Diameter (μm)
2.4	.2	5	120

The 0.18 μm CMOS substrate layer parameters utilized in RF Momentum for planar inductor simulation is listed in Table 8 [10].

Table 8. The inductor substrate layers parameters

Substrate Layers	Thickness (μm)	Permittivity (ϵ_r)	Conductivity (Siemens/m)
Metallization Layer-Sheet Conductor	.99	-	2.8E07
Silicon Dioxide	7.7	3.8	0
Silicon	350	11.9	10

The simulated S-parameters results for planar inductor using RF Momentum tool in ADS is shown in Figure 23 [11], which will be used to extract the inductor parameters.

Figure 23: The S-parameter simulation results for planar inductor in ADS

The overall inductor parameters seen at one of its ports include resistance r , inductance L and Q and they are defined as:

$$r = \text{re}(Z_{in}) \quad (\text{Eq. 7})$$

$$L = \text{im}(Z_{in}) \quad (\text{Eq. 8})$$

$$Q = \frac{\text{im}(Z_{in})}{\text{re}(Z_{in})} \quad (\text{Eq. 9})$$

Where Z_{in} is the total impedance seen at one of the inductor ports with the other port connected to ground.

The extracted inductor parameters r , L , and Q seen at one of its port is shown in Figure 24. The quality factor of 4 to 5 is achieved from the planar inductor simulation in the UWB frequency range as the required inductor value for this design is about 3nH. The resonance frequency occurs when Q and L cross the zero or r becomes maximum which is at about 20GHz in this work.

Figure 24. The simulated Q , L and r of the inductor in ADS

The inductor-extracted parameters generated from S-parameters are shown in Figure 25.

Figure 25. The planar inductor- Π model schematic in ADS

3.3 Mixer Layout Design

The mixer layout is designed using the Virtuoso composer of Cadence in 0.18 μm CMOS TSMC technology as shown in Figure 26. The mixer is laid out with symmetry, and the differential signal connections to the pads are kept as symmetrical and of equal width and length as possible to avoid extra parasitic capacitance, and any mismatch losses. The ground-shielded RF pad layout is implemented using six different metal layers and vias. The supply and ground pads have the same area of 200 μm X 200 μm . The input and output pads are kept at the same size of 100 μm X 100 μm . The distance between the centers of two pads is kept about 100 μm to be compatible with signal-ground-signal RF probes during the measurement. The entire layout area including the pads is about 630 μm X 630 μm . The CMOS technology used has a resistive substrate that makes signal losses and noise degradation for the mixer. This effect is very critical in the high frequency applications above 3GHz. Therefore, the ground-shielded pad layout is very helpful for this kind of applications and for the better mixer performance.

The inductor has been designed using metal6 layer. The higher levels of metals are utilized in this design to avoid large additional capacitive effects to increase the self-resonance frequency. The large metal area is avoided in this design because it also includes more parasitic capacitors, which is not desirable for high frequency signals [11].

Figure 26. The final mixer layout including inductors

For more visual details of layout, Figure 27 shows the transistors (M1-M8), resistors (Rbias1, Rbias2 and Rcm), supply rail (avdd), and ground connection (agnd). The metal connections for supply rails and ground are implemented using metal 1 and metal 2. The ptaps, which connect the body of NMOS transistors, have been utilized to connect the ground signal. The transistors M1-M4 and M7-M8 are laid out with the same size of $15.03\mu\text{m}/180\text{nm}$ (W/L), and the transistors M5 and M6 are laid out

with same size of $60\mu\text{m}/180\text{nm}$ (W/L). The total area of layout without including inductors is about $30\mu\text{m} \times 55\mu\text{m}$.

Figure 27. The mixer layout without using inductors

The Cadence Virtuoso layout editor has Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification tools to check the design-rule violations, and errors in the layout. An extraction simulation is performed on the entire circuit from the layout editor. This allows the simulator to model the capacitive parasitics in the circuit due to the trace overlaps. Layout versus Schematic (LVS) check can then be executed. This verification routine compares the circuit layout with the schematic

design, and notifies the designer if they do not match. After the completion of the extraction and LVS simulation, the post layout simulation is performed to compare all the performance specification results described in the previous section. This provides a more accurate representation of the mixer's performance after the layout stage has been completed. These results are compared against the specification requirements to ensure that the characteristics of the mixer meet or exceed the requirements.

The post layout performance specification for this mixer is shown in Table 9, which closely meets with parameters shown in Table 6.

Table 9. The post layout simulation performance specifications of the mixer

Parameters	Post Layout Simulation Specifications												
RF (GHz)	3.4	4	4.4	5	5.8	6.4	7	7.4	8	8.4	9	9.4	10
LO (GHz)	3.6	4.2	4.6	5.2	6	6.6	7.2	7.6	8.2	8.6	9.2	9.6	10.2
Input IP3 (dBm)	-6.58	-6.96	-8.33	-9.26	-8.82	-12.14	-9.69	-10.91	-9.79	-7.68	-9.88	-11.08	-12.67
Conversion Gain (dB)	18.84	22.86	23.06	21.7	20.7	20.8	20.8	21.2	21.6	21.3	20.4	19.3	17.48
SSB NF (dB)	12.05	10.96	11.44	11.8	12.1	12.3	12.3	12.6	12.9	13.1	14.2	15.7	17.15
DSB NF (dB)	9.85	7.98	8.56	8.74	9.4	9.36	9.26	9.54	9.98	10.46	11.68	12.89	14.75
Input Referred P1-dB (dBm)	-10.72	-10.54	-10.29	-9.63	-2.27	-3.13	-4.61	-4.88	-3.72	-2.36	-1.09	2.06	2.11

CHAPTER 4. CONCLUSION

The main task involved in this thesis is to come up with the appropriate architecture for the mixer that works in 3.1 GHz to 10.6GHz of UWB frequency range. As a conclusion to this thesis, the significant contribution presented in the previous three chapters is described below.

The integrated low-voltage and low noise UWB mixer was designed and analyzed using the TSMC 0.18 μ m CMOS technology with differential Gilbert-cell architecture. This mixer is different from the conventional architecture in a way that it proposes the wide-bandwidth characteristics of 7.5GHz in the UWB band. The designed mixer requires only a 1.8 V supply voltage and it downconverts the RF frequency to 200MHz UWB operation region. This mixer achieves the SSB NF of 16.75 dB, the P-1dB of 1.49dBm, the IIP3 of -12.11 dBm, and the voltage conversion gain of 18.13 at the RF frequency of 10 GHz. The mixer performance represents the low noise figure, low supply voltage, good linearity, and the excellent conversion gain.

The noise figure of the mixer is about 16.75 dB because of the switching action of the LO pair and the internal parasitic capacitance. Therefore, this mixer design could be improved in the future in terms of noise figure (NF). The noise figure must be less than 10 dB for an ideal mixer. This mixer can be utilized for the UWB receiver front-end, and for the low voltage and the low noise wireless applications such as WPAN, and mobile communications.

The summary of the mixer performance achieved in this thesis work is listed in Table 10 and compared with other work. The operating range of this mixer is over

the entire UWB band as opposed to operating at only one RF frequency. The voltage conversion gain of this mixer is about 11dB more than the previous works at 10GHz [5, 6]. This mixer dissipates about 3mW less power compared to the other work [5, 12].

Table 10. The summary and comparison of the mixer performance

Performance Parameters	This Work	[3]	[4]	[5]	[6]	[12]
Technology	TSMC 0.18 μ m	TSMC 0.18 μ m	TSMC 0.18 μ m	TSMC 0.18 μ m	–	0.5 μ m CMO
Supply Voltage (V)	1.8	1.8	1.8	1.5	–	2.5
Frequency (GHz)	10	1.32	2.45	5.8	2	0.435
Conversion Gain	18.13	20.5	27	7	7.2	20.8
Noise Figure (dB)	16.75	5.6	12.5	14.3	9.15	9.2
IIP3 (dB)	-12.11	11.25	-3.7	-2.94	-2.5	-13.25
P1- dB (dB)	1.41	–	–	–	-9	-21
Power (mW)	2.96	11.5	–	6.89	5mA	5.4

REFERENCES

- [1] A. Silvennoinen (2004, Sept.). Unlicensed reuse of licensed spectrum: case UWB. Helsinki University of Technology, FIN-02150 Espoo. [Online]. Available: http://www.netlab.tkk.fi/opetus/s38042/s04/Presentations/24112004_Silvennoinen/Silvennoinen_paper.pdf
- [2] Intel Corporation, CA. Ultra-Wideband (UWB) Technology. [Online]. Available: <http://www.intel.com/technology/comms/uwb/>
- [3] T. Phan, C. Kim, Y. Shim and S. Lee. (2005, April). High Performance CMOS Direct Down Conversion Mixer for UWB System. *IEICE Trans. on Electronics*. [Online] *Volume E88-C, Number 12*, pp 2316-2321. Available: <http://ietele.oxfordjournals.org/cgi/content/abstract/E88-C/12/2316>
- [4] Q. Li, "Linearity Analysis and Design Optimization for 0.18 μm CMOS RF Mixer," *IEE Proceedings of Circuits, Devices and Systems*, vol. 149, no. 2, April. 2002.
- [5] X. Wang. (2003, Aug.). A Novel Low Voltage Low Power 5.8 GHz CMOS Down-Conversion Mixer Design. Presented at IEEE Radio and Wireless Conference. [Online]. Available: <http://ieeexplore.ieee.org/iel5/8697/27540/01227952.pdf>
- [6] G. Watanabe, H. Lau and J. Schoepf. (2000, Aug.). Integrated Mixer design. Presented at 2nd IEEE Asia Pacific Conference. [Online]. Available: <http://ieeexplore.ieee.org/iel5/7202/19406/00896936.pdf>
- [7] Maxim Integrated Products, Inc., CA. Mixer 2x2 Spurious Responses and IP2 Relationship. [Online]. Available:

http://www.maxim-ic.com/appnotes.cfm/appnote_number/1838

[8] National Semiconductor Corporation, CA. Integrated LNA and Mixer Basics.

[Online]. Available: <http://www.national.com/an/AN/AN-884.pdf>

[9] S. S. Mohan, "Modeling, Design and Optimization of On-Chip Inductors and Transformers," Stanford University, CA. Thesis. PhD. Source DAI-B 61/02, p.1000, Aug 2000.

[10] R. Zarnaghi, "Designing a CMOS Ultra Wide Band Low Noise Amplifier Considering Parasitic of Package," San Jose State University, CA. August 2005.

[11] N. Oh, H. Choi, N. Trung Kien, J. Choi, S. Lee. 0.25 μm CMOS Transistor and Inductor Test Pattern Layout for RFIC Applications. Hoing-Ik University,

Chochiwon, Korea. [Online]. Available:

<http://rfcmos.icu.ac.kr/pdf/domestic/conferences/12.pdf>

[12] P. Rossi, A. Liscidini, M. Brandolini, F. Svelto. (2004, Feb.) A 2.5dB NF Direct-Conversion receiver Front-End for HiperLAN2/IEEE802.11a. Presented at IEEE Solid-State Circuits Conference (ISSCC). [Online]. Available:

<http://ieeexplore.ieee.org/iel5/9264/29428/01332614.pdf>

APPENDICES

A.1 The P1-dB Simulation Procedure

To simulate the voltage conversion gain in Cadence, the SPSS analysis has been implemented using the analog affirma environment. In the SPSS analysis, the input ports of the test bench are specified by sine type, RF frequency in Hz, 50Ω input resistance, and input power amplitude in prf dBm. The prf variable in PSS analysis is linearly swept from -30 to 5 dBm with about 10 steps. By selecting the differential output IF nets in the test bench, the input referred 1-dB compression could be plotted as shown in Figure 17.

A.2 The IIP3 Simulation Procedure

To simulate IIP3 in Cadence, the RF ports in the test bench are set-up by defining the sine type, rf frequency in Hz, prf amplitude in dBm, 1V of DC level, and prf in PAC magnitude. For the 10GHz of RF frequency, the PAC analysis is implemented by selecting the sweep type as absolute, the single point frequency as 1020MHz, the array of indices as 49 -51, and then running the PSS and the PAC analysis in the analog affirma environment. The results can be plotted by selecting the following options from the main form of the direct plot: the function as IPN curves, the differential nets with $R=50\Omega$; the sweep variable, the 1st and 3rd order harmonics as 180MHz and 220MHz, respectively, and then positive and negative nets from the test bench. Similar simulations can be done for all the bands in 3.4 GHz to 10 GHz RF

frequency range. Please refer to the Table 6 for all the IIP3 simulation results.

A.3 The Noise Simulation Procedure

The Pnoise analysis is implemented by sweeping frequencies from 1MHz to 200MHz with logarithmic sweep, and 10 points per decades; selecting differential output voltage nets and the input RF port from the test bench schematic, and defining the reference side band of -1. After running the PSS and the Pnoise simulations in an analog affirma environment, the SSB NF and DSB NF are plotted by choosing the Pnoise in the main form, and selecting the NF and NFdsb respectively. The mixer's simulated SSB NF is 16.75dB and DSB NF is 13.83dB for 10GHz of input RF frequency.

A.4 The Voltage Conversion Gain Simulation Procedure

The PSS and the Periodic Transfer Function (PXF) analysis are implemented to simulate the voltage conversion gain of the mixer. The RF port is set-up as a DC source type with the DC voltage of 1 V and the PAC magnitude of 1V; The LO port and the PSS is set up in the same way same as the NF analysis. The PXF analysis is implemented by selecting the absolute sweep type with start and stop frequencies as 1MHz and 200MHz, respectively, in linear sweep, and the maximum sideband as 3; and choosing the positive and negative output node from the schematic to see the conversion gain. The simulated conversion gain of 18.13dB is found for the 10GHz of the input RF frequency as shown in Figure 21.