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Super MOS transistors : lambda reducing circuits and their applications

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SUPER MOS TRANSISTORS:
LAMBDA REDUCING CIRCUITS AND THEIR APPLICATIONS

A Thesis

Presented to

The Faculty of the Department of Electrical Engineering

San Jose State University

In Partial Fulfillment

of the Requirements for the Degree

Masters of Science

by

Vincent Wall

December 2008

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SUPER MOS TRANSISTORS:

LAMBDA REDUCING CIRCUITS AND THEIR APPLICATIONS

by

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ABSTRACT

SUPER MOS TRANSISTORS: LAMBDA REDUCING CIRCUITS AND THEIR APPLICATIONS

By Vincent Wall

Transistors do not operate like ideal current sources when they are in the saturation region, using the following equation $I_d = \frac{\mu_n C_{ox}}{2} \frac{w}{l} (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$. The reason for this in MOS devices is channel length modulation, modeled approximately by $(1 + \lambda V_{ds})$. Channel length modulation is caused when the voltage on the drain is increased, which increases the width of the drain depletion region, thereby shortening the channel, and increasing the current through the drain. This directly decreases the output resistance of the transistor. Standard 0.18u MOS transistors have a lambda, in the saturation region, between 75mV^{-1} and 21mV^{-1} . A Super MOS transistor circuit negates this effect by using negative feedback to stabilize the drain current, thereby reducing channel length modulation. Multiple Super MOS circuits and regular MOS transistors have been designed, fabricated, and tested using TSMC's 0.18 process. The results have shown that λ is reduced up to a factor of 4 with minimal reduction in drive when compared to a minimally sized 0.18u process transistor ($W=270\text{nm}$, $L=180\text{nm}$).

DEDICATIONS

To my mother who has drilled into me since I was a toddler the importance of an education. And to my son, Jacob, who is the reason that I did not give up three fourths of the way through my master's degree.

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CHAPTER 1

INTRODUCTION

1.1. Background

With transistor gate lengths one micron and smaller, the gain of analog circuits is severely degraded due to large channel conductance. Cascoding of transistors can and has been used to overcome the large channel conductance leading to greater gain and accuracy in the circuits [1]. The gain produced by this technique of cascoding transistors is too small to be used in several applications, OpAmps being one of these [2]. Taking a look at the small signal equation for a common source amplifier, equation 1.0, we see that there are two ways to increase the gain of the circuit.

$$A_v = \frac{V_{out}}{V_{in}} = -g_m \cdot r_o \quad (1.0)$$

The first way is to increase the transconductance, and the second would be to increase its output resistance. Transconductance (g_m) is calculated by equation 1.1b and it is the ratio of the output current to input current.

$$g_m = \frac{I_{out}}{V_{in}} \quad (1.0b)$$

The output resistance (r_o) is calculated by equation 1.1c.

$$r_o = \frac{1}{\lambda \cdot I_d} \quad (1.0c)$$

Super MOS circuits greatly improve the output resistance of the transistor by decreasing lambda. This is done by using a third transistor to provide feedback to the

drain transistor. Both types of Super MOS discussed in this paper, Super 3t and Super 13t, improve channel length modulation.

1.2. Gain Boosting Technique

One way to increase the gain of a MOS device is to create a cascode circuit (Figure 1) yielding a gain of [2]:

$$Av = g_{m1}r_{o1}(g_{m2}r_{o2} + 1) \quad (1.1)$$

Figure 1. Cascode Amplifier

Continuing to use the cascode method to increase the dc-gain of the circuit would quickly destroy the output swing of the circuit, since each transistor would need to have a V_t across it. To overcome this, one needs to increase the output resistance (decreasing λ) of the circuit. This can be done by using a third transistor as an

amplifying feedback loop to the cascading transistor as was done in the Super3t MOS model in Figure 2. This creates a gain [2] as described in equation 1.2 with an output resistance as described in equation 1.3.

$$A_v = g_{m1}r_{o1}(g_{m2}r_{o2}(g_{m3}r_{o3} + 1) + 1) \quad (1.2)$$

$$R_{out} = r_{o1}(g_{m2}r_{o2}(g_{m3}r_{o3} + 1) + 1) + r_{o2} \quad (1.3)$$

Figure 2. Super3t NMOS without Current Mirror [3]

One could get a higher dc-gain by adding an OpAmp to the gate of the cascoding transistor connecting the drain of the gate transistor to the OpAmp's negative input. The positive input of the OpAmp is connected to a V_{ref} , and its output connects to the gate of the cascoding transistor. This circuit uses the same equations as the Super3t MOS, 1.2 and 1.3, substituting $A_{v_{opamp}}$ for $g_{m3}r_{o3}$ [2].

With the gain-boosting principle one can overcome the inherent limitations of a MOS device by increasing the output resistance and dc gain of the cascaded circuit.

The new limitations on the gain of the transistor are now set by the following factors: leakage current, weak avalanche, and thermal feedback [4].

1.3. Low Output Conductance Composite MOSFET's

To increase the output resistance (R_{out}) of the transistor, one could use the circuit design technique that C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss demonstrated in their paper "Low Output Conductance MOSFET's for High Frequency Analog Design." They demonstrated a technique to create transistor arrays that were wider at the drain than at the source [5]. Their proposed transistors could be designed to increase the ratio of transconductance-to-output conductance over that of a short channel transistor. The trade-off in their design would be a slight penalty in its signal swing [5]. The Super MOS transistors incorporate their design technique by making the width of the drain transistor larger than the width of the gate transistor.

1.4. Laterally Diffused Implanted MOS Transistor

Based on the finding of Basham [6], a non-circuit way to reduce λ would be to use another family of transistors. The family that shows the greatest potential to increase R_{out} is the laterally diffused implanted MOS transistors (LDMOS). LDMOS is created by an additional well or shifted well that, when diffused, creates an asymmetric device. The devices were first introduced as a method of exceeding the limits of photolithography. At that time its analog capabilities were sparsely researched. This was in part due to the complexity in determining the position of the junction and its threshold voltage. These difficulties have been largely alleviated by the tight process controls required for submicron devices. It can be shown that the

initial channel current, in LDMOS, is significantly reduced, and that λ , channel length modulation, is reduced. Future studies should compare and contrast the performance and trade-offs of LDMOS transistors versus Super MOS transistors [6].

CHAPTER 2

DEVELOPMENT

2.1. Super MOS

Super MOS circuits are one way to decrease the effect of channel length modulation, Lambda (λ) is used to model channel length modulation. Lambda can be calculated by using the approximate calculation, equation 2.1, or by the more exact formula equation 2.2 [7].

$$\lambda = \frac{\Delta I_d}{I_d \cdot \Delta V_d} @ V_g \quad (2.1)$$

$$\lambda = \frac{\frac{\partial I_d}{\partial V_{ds}}}{I_d - \left(\frac{\partial I_d}{\partial V_{ds}} \right) V_{ds}} \quad (2.2)$$

The channel length shrinks because the drain voltage increases, which increases the drains depletion width, and it forms a junction with the substrate. This shortens the “effective” channel length [8]. When the channel length shrinks and the drain current increases, lambda becomes $1/V_d$ at a specific gate voltage. This effect can clearly be seen in current mirrors. In a current mirror, Figure 3, the biasing voltage V_g is tied to V_d , and any changes in V_d will result in a shift in the output current (I_d) of the device, even though I_{ref} is at a constant current. In Figure 4 one can see that even though I_{ref} has a constant value I_{out} ’s value fluctuates with V_d .

Figure 3. Standard Current Mirror

Figure 4. Standard Current Mirror Output

This is quite different for the Super MOS. The Super MOS has a smaller value for λ , which means that it is stable for all V_{ds} in the saturation region. This translates into a stable I_d for all values of V_{ds} in the saturation region. These curves and their properties will be discussed below.

There are several different types of Super MOS's. They have been named according to the number of transistors that are needed to create the circuit. These circuits are 3t, 13t novel, 13t patented, and 12t, to name a few. This thesis will be focusing on the 3t and 13t novel (hereinafter 13t) [2], [3]. All of the circuits come in both P-type and N-type varieties. A comparison and analysis of these two Super MOS's versus a regular 0.18u MOS will be shown.

The design of the two Super MOS's was done to show how well they compare to a regular transistor of minimal sizing. To address this it was decided to design the Super MOS's so that their current driving capabilities matched, as closely as possible, the curves of a regular MOS; $W=270\text{nm}$ and $L=180\text{nm}$. They could have been designed to produce the best Super MOS by focusing on a greater g_m and lower V_t , but it was felt that it would have provided a false comparison since their I_d vs. V_{ds} curves would no longer match. For fabrication, TSMC's 0.18u deep process, provided by MOSIS, was used.

A side benefit of the Super MOS circuits is that an analog designer will be able to use these Super MOS designs as a standard cell. To show how this can be done, several current mirrors and two OpAmps were designed and tested with no changes to their Super MOS components.

2.1.1. Cascode Super3t MOS

There were Super3t MOS that were designed, fabricated, and tested using TSMC's 0.18 μ process, the initial Super3t MOS and the improved Super3t MOS. The improved Super3t MOS is identical to the initial Super3t MOS with the addition of a current mirror.

2.1.1.1. Initial Super3t MOS

The Super3t MOS is the easiest type of Super MOS to design. The initial design was obtained from Francesc Serra-Graells, PhD, Problemes de Circuits Integrats Analogics, and originally published in, *Analog VLSI - Signal and Information Processing* by Klaas Bult [8]. As seen in Figure 2, it is composed of just three transistors and an external current source. The Super MOS pictured in Figure 2 was designed in AMI's 1.6 μ process, and was not optimized. The purpose of the circuit in Figure 2 was to study how the Super3t MOS functions, and to show that it could reduce λ while mimicking a regular MOS transistor. Figure 5 shows the Spectre simulation results, using AMI's 1.6 μ process, AMI16, for the Super3t NMOS (Figure 2) vs. a regular NMOS, with $W=6.4\mu\text{m}$ & $L=6.4\mu\text{m}$. On the left hand side of Figure 5 are the results of the regular NMOS; while on the right side are the results of the Super3t NMOS. The saturation region of the Super MOS is flat while the NMOS has a noticeable bend in it, which translates into a higher λ value. The inverted bend in the Super MOS's linear region is caused by not limiting the voltage on I_{in} . This issue was fixed in the Super3t MOS designed in this thesis by using a current mirror and attaching I_{out} of the current mirror to I_{in} of the super3t MOS.

Figure 5. Leafcell Simulation Results: Super3t NMOS vs. NMOS; $w=6.4\mu$, $l=6.4\mu$

Not limiting the voltage on I_{in} led to an interesting result when the circuit was fabricated and tested: when V_{ds} approached 3v the current rose in an exponential fashion. Graph 2 shows this behavior.

The discrepancies seen between simulation and testing of this Super3t NMOS are twofold. First, the exponential rise in I_d at the tail end of V_{ds} did not match the simulation and led to an increase of λ . During testing, V_{ds} was extended out to five volts (these results were not included) and the exponential rise in I_d continued. One notes the rise in λ followed it. The second discrepancy was the inverted slope in the linear region as seen in simulation, which was not seen in the testing results of

Figure 6. Both of these issues were resolved with the addition of the current source onto the Super 3t MOS, which limited the maximum voltage at the I_{in} node.

Figure 6. Leafcell Testing Results: Super3t NMOS - I_d vs. V_d

The Super3t NMOS circuit can be understood by considering the following description and equations. Transistor N0, in Figure 2, is the current limiting part of the circuit. If we take a look at the saturation current equation, equation 2.3, we see that we can limit the max current according to the standard CMOS equation below.

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{w}{l} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \quad (2.3)$$

Since the goal is to mimic a regular MOS, I_d could not be a design variable. In addition $(V_{gs} - V_t)$ is not available for to design with, since it will not be known what V_{gs} a future designer will use. This leaves only the width and I_{in} , of the Super MOS,

available as a design variable: if one wanted a larger length a different process would have been used.

In Figure 2, transistors N1 and N2 create a feedback loop. Their interactions with each other can be viewed in the following equations:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{w_1}{l} (V_{gs_1} - V_t)^2 (1 + \lambda_1 V_{ds_1}) \quad (2.4)$$

$$I_{in} = \frac{\mu_n C_{ox}}{2} \frac{w_2}{l} (V_{gs_2} - V_t)^2 (1 + \lambda_2 V_{ds_2}) \quad (2.5)$$

$$V_{gs_2} = V_{ds_0} \quad (2.5b)$$

Substituting $(V_{dd} - V_{gs_2})$ for V_{ds_1} into equation 2.4 yields:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{w_1}{l} (V_{gs_1} - V_t)^2 (1 + \lambda_1 (V_{dd} - V_{gs_2})) \quad (2.6)$$

Substituting $(V_{ds_2} - V_{gs_2})$ for V_{gs_1} into equation 2.6 yields:

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{w_1}{l} (V_{ds_2} - V_{gs_2} - V_t)^2 (1 + \lambda_1 (V_{dd} - V_{gs_2})) \quad (2.7)$$

Solving for V_{ds_2} in equation 2.5 yields:

$$V_{ds_2} = \frac{1}{\lambda_2} \left[I_{in} \frac{2}{\mu_n C_{ox}} \frac{l}{w_2} \frac{1}{(V_{gs_2} - V_t)^2} - 1 \right] \quad (2.8)$$

If we take a look at equation 2.8 we can see that width of transistor N2, W_2 , is inversely proportional to V_{ds_2} , and V_{ds_2} is a squared component of I_d . The more we increase the width of W_2 the lower I_d will be by the square of V_{ds_2} . W_2 , has the most direct effect on the slope of the I_d vs. V_d curve of the system in the saturation region, and is it is directly responsible for λ 's value. Care must be taken in choosing its

value because if it is increased too much then it will start to take over as the current limiting variable of the system. Transistor N1's width, W_1 , has the most effect on the curve in the linear region and the V_t of the circuit. Looking at equation 2.9, if the width, W , is increased significantly, then N1's overdrive voltage will shrink, thereby affecting the bias voltage.

$$V_{od} = \sqrt{\frac{2I_d}{\mu_n C_{ox} \frac{W}{L}}} \quad (2.9)$$

As the bias points of the transistors change, their corresponding λ changes; this changes the drain current.

2.1.1.2. Improved Super3t MOS

The improved design of the Super3t MOS, as previously stated, has been optimized to mimic a regular MOS in TSMC's 0.18 μ process. It is shown in Figure 7. The major difference between Figure 2 and Figure 7 is that Figure 7 has a current mirror attached to the I_{in} terminal. This allows the circuit to be self-biased, and removes the inverted bend, Figure 6, from the I_d vs. V_{ds} curve. One must be careful about the sizing of the current mirror. The output current is not the most important variable: what is important is to make transistor N1, Figure 7, biased appropriately at around 400mV to 600mV.

Figure 7. Super3t NMOS

2.1.2. Novel Super MOS Using Gain Boosting

The Super13t MOS, pictured in Figure 8, incorporates the gain boosting technique by using a transresistance amplifier. The trade-offs of the Super13t MOS, when compared to the Super3t model, are: an increase in area, an increase in complexity, and an increase in power consumption [1], [2]. The Super13t MOS, when incorporated into an OpAmp, is able to let the output go rail-to-rail. The circuit in Figure 3 is composed of three parts: a cascode output, a transresistance amplifier, and a biasing stage [9].

The cascode output stage, comprising transistors N0 and N1, functions just like the Super3t MOS. Transistor N1 is the current limiting factor for the drain current. As in the Super3t MOS, the overdrive voltage of N0 helps to determine the biasing of N1. Note that V_{ds1} should be set so that it is around 400mV - 600mV, as in the Super3t MOS. V_{gs0} should also be set around the same voltage. The best value for the width of N1 was 270nm and for N0 to be 4050nm, or a multiplier of 15.

Six transistors make up the transresistance amplifier of Figure 8. They are N2-N4 and P2-P5. Equations 2.10 and 2.11 below describe the output resistance and gain of the circuit [2].

$$R_{out} = [gm_{N0}ro_{N0}(gain + 1) + 1] \cdot [ro_{n1} \parallel ro_{n2}ro_{p5}ro_{p2}] \quad (2.10)$$

$$gain = gm_{n4}ro_{n4} [gm_{n3}ro_{n3} \parallel gm_{n4}(gm_{n3}ro_{n3}ro_{n4} \parallel gm_{p4}ro_{p4}ro_{p3})] \quad (2.11)$$

Figure 8. Super13t NMOS

Biasing is achieved with transistors N5-N6 and P0-P1. If one takes a look at transistors, N1, N2, and N5 form a loop. This loop ensures that the drain transistor, N0, is always biased at 500mV-600mV, allowing the output to swing almost rail to rail. The loop equations are below [2].

$$V_{ds1} = V_{gs5} - V_{gs2} \quad (2.12)$$

$$= \sqrt{\frac{2I_5}{k_5}} + V_{to} - \sqrt{\frac{2I_2}{k_2}} + V_{to} \quad (2.13a)$$

$$k = \mu n C_{ox} \frac{w}{l} \quad (2.13b)$$

$$= \sqrt{\frac{2I_5}{k_5}} - \sqrt{\frac{2I_2}{k_2}} \quad (2.14)$$

$$= \sqrt{\frac{2I_2}{\frac{1}{2}k_2}} - \sqrt{\frac{2I_2}{k_2}} \quad (2.15)$$

$$= \sqrt{\frac{4I_2}{k_2}} - \sqrt{\frac{2I_2}{k_2}} \quad (2.16)$$

$$\cong 0.414 \sqrt{\frac{I_2}{k_2}} \quad (2.17)$$

$$I_5 = I_2 \text{ and } k_5 = \frac{1}{2}k_2 \quad (2.18)$$

Thus, the ratio of the currents I_0 and I_2 can be found by solving for V_{ds1} (equations 2.19 – 2.24), comparing equation 2.24 to equation 2.17, and solving for I_2 .

$$\frac{w_5}{l_5} = \frac{w_2}{2l_2} \quad (2.19)$$

$$V_{ds1} \geq V_{gs1} - V_t \quad (2.20)$$

$$V_{ds1} = V_{gs1} - V_t \quad (2.21)$$

$$= V_{gs1} - V_t \quad (2.22)$$

$$= \sqrt{\frac{2I_0}{k_0}} + V_t - V_t \quad (2.23)$$

$$= \sqrt{\frac{2I_0}{k_0}} \quad (2.24)$$

$$0.414 \sqrt{\frac{I_2}{k_2}} = \sqrt{\frac{2I_0}{k_0}} \quad (2.25)$$

$$0.414 \sqrt{I_2} = \sqrt{2I_0}, k_2 = k_0 \quad (2.26)$$

$$\sqrt{I_2} = \frac{\sqrt{2I_0}}{0.414} \quad (2.27)$$

$$\frac{0.17}{2} = \frac{I_0}{I_2} \quad (2.28)$$

$$0.085 = \frac{I_0}{I_2} \quad (2.29)$$

From what has been found from numerous simulations of this circuit, the biasing stage does not affect λ as viewed from the drain of N0. However, it does affect the max current out of that drain.

2.2. Comparison and Results of Simulations

In this section, the simulation results of the Super MOS transistors will be discussed.

2.2.1. N-Type MOS

The first Super MOS transistors that will be looked at are the N-type transistors: standard nmos, Super 3t NMOS, and Super 13t NMOS.

2.2.1.1. I_d vs. V_d – Lambda

Figure 9 is a comparison of the simulation results of I_d vs. V_d for a V_{gs} sweep of 0.72V to 1.8V. Looking at the figure we will see that a regular NMOS has a well defined slope in the saturation region, unlike the Super3t NMOS or the Super13t NMOS. Using the figure of the regular NMOS as our baseline, the next thing observed are the slopes of the lines in the linear region. In the linear region, the Super3t NMOS follows the regular NMOS curves closer than the Super13t NMOS. What happens to the Super13t NMOS is that transistor N1, from Figure 8, gets saturated at a lower current than does transistor N0, from Figure 3. This leads to a lower saturation current for the Super13t NMOS.

From Figure 9, we can use equation 2.2 to calculate the Lambda for each value of V_{gs} and the lambdas for each transistor. The important thing to note is that the Super13t NMOS has a significantly lower, approximately a decade, lambda value than the Super3t NMOS and a lambda that is 4 to 5 decades lower than the regular NMOS, leading to a higher output resistance on the drain of the Super13t NMOS. Output resistance can be calculated in the equation 2.30, and can be seen in Table 1.

Figure 9. Id vs. Vd for NMOS, Super3t NMOS, & Super13t NMOS

$$R_{out} = \frac{1}{\lambda * I_d} \quad (2.30)$$

Table 1. Average Lambda for NMOS, Super3t NMOS, & Super13t NMOS

	Regular NMOS	Super3t NMOS	Super13t NMOS
Ave Lambda (sat)	0.149768V ⁻¹	0.00080065V ⁻¹	0.004941V ⁻¹
Ave R _{out} (sat) @ 100 uA	66.769 Kohm	12.489 Mohm	2.024 Mohm

2.2.1.2. Id vs. $V_g - V_t$, & Gm

Figure 10 shows both the Id vs. V_g and gm plots for the three NMOS circuits discussed in this paper. Notice that both the regular NMOS and Super3t NMOS line up fairly well, with the gm of the Super3t NMOS slightly lower. The problem with the Super13t NMOS is its max gm is significantly lower than the other two. The reason for this is that this design of the Super13t NMOS circuit was not optimized for gain. The design of the circuit focused on the minimization of λ and the ability to mimic the Id vs. V_d Graph of a regular NMOS. Thus, the transresistance sub-circuit could not be optimized because the Super13t NMOS's drain current would have been much greater than the imposed metric of a regular NMOS. From Figure 10, we can obtain the V_t of all three circuits (see Table 2).

Table 2. V_t & Gm for NMOS, Super3t NMOS, & Super13t NMOS

	Regular NMOS	Super3t NMOS	Super13t NMOS
$V_t @ V_{sb}=0V$	0.573V	0.630V	0.685V
$g_{m_{max}} @ V_{sb}=0V$	$2.53 \cdot 10^{-5} S$	$2.45 \cdot 10^{-5} S$	$1.67 \cdot 10^{-5} S$

Figure 10. I_{ds} vs. V_d & G_m for NMOS, Super3t NMOS, & Super13t NMOS

2.2.1.3. AC Response

Simulation of the AC response was done with the transistors in a common source configuration. From the Figure 11, we can see that both the Super13t and Super3t transistors have a unity gain of approximately 775 MHz, while a standard transistor has a unity gain of approximately 46.5 GHz (the y-axis was calculated by the following equation: $20 \cdot \log(V_{out}/V_{in})$). Table 3 lists the relevant information for the three transistor's AC response.

Table 3. AC Characteristics for NMOS, Super3t NMOS, & Super13t NMOS

	Regular NMOS	Super3t NMOS	Super13t NMOS
Unity Gain Freq	46.5 GHz	775 MHz	775 MHz
Unity Gain Phase	39.87 degrees	43.46 degrees	39.13 degrees
3dB Gain Freq	8.04 GHz	134 MHz	335.5 MHz
Max Gain	12.78 dB	15.32 dB	14.02 dB

Figure 11. Frequency Response for NMOS, Super3t NMOS, & Super13t NMOS

2.2.2. P-Type MOS

The P-Type MOS's that will be discussed are the same types as the N-Type MOS. These are the standard PMOS, Super3t PMOS, and the Super13t PMOS. Figures 12 and 13 are schematics of the Super3t PMOS and Super13t PMOS respectively.

2.2.2.1. Id vs. Vd - Lambda

Figure 14 shows the simulation results for the PMOS variety of the three transistors. The most notable difference between the PMOS's Graph and NMOS's Graph is that the Super13t PMOS transistors Id curves do not follow close at all to the regular PMOS's curves. The Super3t PMOS also does not follow as closely to the regular PMOS curves as does it Super3t NMOS counterpart. Looking at Table 4 we see that the lambdas are not as low as the NMOS circuits; meaning that the PMOS output resistance is slightly higher than the NMOS. Table 4 lists the values Lambda and R_{out} .

Table 4. Average Lambda for PMOS, Super3t PMOS, & Super13t PMOS

	Regular PMOS	Super3t PMOS	Super13t PMOS
Ave lambda (sat)	$-0.36208V^{-1}$	$-0.00010664V^{-1}$	$-0.09160V^{-1}$
Ave R_{out} (sat) @ 100 uA	27.618 Kohm	93.773 Mohm	100.17 Kohm

Figure 12. Super3t PMOS

Figure 13. Super13t PMOS

Figure 14. Id vs. Vd for PMOS, Super3t PMOS, & Super13t PMOS

2.2.2.2. Id vs. Vg – Vt, & Gm

The transconductance gain of the Super13t PMOS is poor. This is due to the design goals that were stated previously. This transconductance gain is illustrated in Figure 15. Additionally, Figure 15 shows that the Super3t PMOS has a slightly lower gm than a standard transistor. The Vt for each transistor and their corresponding minimum gm is shown in Table 5.

Table 5. Vt & Gm for PMOS, Super3t PMOS, & Super13t PMOS

	Regular PMOS	Super3t PMOS	Super13t PMOS
Vt @ Vsb=0V	-0.751V	-0.720V	-0.621V
gm _{min} @ Vsb=0V	-6.51*10 ⁻⁶ S	-6.38*10 ⁻⁶ S	-2.07*10 ⁻⁶ S

Figure 15. Id vs. Vg & Gm for PMOS, Super3t PMOS, & Super13t PMOS

2.2.2.3. AC Response

The AC Response of a Super PMOS is different from those of a Super NMOS. Looking at Table 6, one of the first differences is that the unity gain frequency is 175 MHz lower for the Super13t PMOS and 475 MHz lower for the Super3t PMOS than for their Super NMOS counterparts. The maximum gain possible is also about half as much as N-type MOS. But, if we compare the Super PMOS AC response to that of a regular PMOS we can clearly see that the major differences are in the max frequencies. This can clearly be seen in Figure 16. If we compare Figure 11 and Figure 16, it is seen that the Super3t NMOS has a higher gain. In Figure 16 however, the Super13t

PMOS has a higher gain. In Figure 16, the Super13t PMOS has a unity gain frequency 300 MHz higher than the Super3t PMOS. In contrast, the N-type Super MOS had approximately the same unity gain frequency. The difference in the unity gain frequencies is due to the different size of the N-type and P-type Super MOS. This is because the I_d vs. V_{ds} curves of the N-type and P-type Super MOS are not the same.

Table 6. AC Characteristics for PMOS, Super3t PMOS, & Super13t PMOS

	Regular PMOS	Super3t PMOS	Super13t PMOS
Unity Gain Freq	14.4 GHz	300 MHz	600 MHz
Unity Gain Phase	47.31 degrees	46.84 degrees	42.00 degrees
3dB Gain Freq	8.04 GHz	187.5 MHz	336.5 MHz
Max Gain	6.82 dB	6.68 dB	7.09 dB

Figure 16. Frequency Response for PMOS, Super3t PMOS, Super13t PMOS

CHAPTER 3

APPLICATIONS

3.1. Current Mirror Comparisons

The most important property of a current mirror is the ability of the output current (I_{out}) to mirror a reference current (I_{ref}). The Super3t type MOS was better in both of these characteristics.

3.1.1. Comparison of Super3t NMOS vs. Super13t NMOS

Figure 17 and 18 are the block diagrams of the Super3t NMOS and Super13t NMOS current mirrors. In simulation, the Super3t NMOS was able to track I_{ref} through a range of 0A to 200uA, whereas the Super13t NMOS cutoff at 100uA (Figure 19). This occurs because of the transresistance component of the circuit. The issue lies with the transistors P2-P4 in Figure 8. As more current passes through transistor N1, the voltage on the source of N2 rises. This allows less current to flow through transistors P2, P5, and N2, reducing the voltage at the gate of N0, and turning off the circuit. Output current to reference current linearity of the Super13t NMOS is also less than the Super3t NMOS. Looking at Figure 19, we see that the Super3t NMOS tracks extremely well except for when V_{ds} goes below 0.72V.

Figure 17. Super3t NMOS Current Mirror

Figure 18. Super13t NMOS Current Mirror

Figure 19. I_{out} vs. I_{ref} of Super3t NMOS & Super13t NMOS

3.1.2. Comparison of Super3t PMOS vs. Super13t PMOS

The results of the Super PMOS current mirrors are similar to the results for the Super NMOS current mirrors. Looking at Figure 20, we see that the Super13t PMOS cannot track I_{ref} beyond $-75\mu A$. The reason for this is the same as for the Super13 NMOS. The Super3t PMOS starts to veer away from I_{ref} when V_{ds} is $-1.44V$, and a deviation can clearly be seen once V_{ds} is at $-1.8V$. If one were looking to use one of these types of Super MOS for a current mirror it would be best to use the Super3t variety because of: higher output current range, the ability of I_{out} to track I_{ref} , and a simpler design that consumes less overall current and uses less area on a die. Figures

21 and 22 are block diagrams of the Super3t PMOS and Super13t PMOS current Mirrors.

Figure 20. I_{out} vs. I_{ref} of Super3t PMOS & Super13t PMOS

Figure 21. Super3t PMOS Current Mirror

Figure 22. Super13t PMOS Current Mirror

3.2. Operational Amplifier

The two-stage operational amplifiers, shown in Figure 23 and Figure 24, were designed to show how the Super MOS can easily be integrated as components in a design: the difference between the two designs is the differential inputs stage; The Super3t OpAmp's inputs are-sized with an $m=3$ ($W=810\text{nm}$) while the Super13t OpAmp's inputs are-sized with an $m=5$ ($W=1350\text{nm}$). The OpAmps were tested with a sine wave input of 50mV , and the load capacitance was varied through a range, shown in Table 7 and Table 8.

Table 7. Super3t OpAmp Frequency Response

	3db Freq (Hz)	Unity Gain Freq (Hz)	Unity Phase (degrees)
Vout dB@Cl=1pF	1.25E+07	6.55E+07	86.2
Vout dB@Cl=10pF	1.58E+07	3.03E+07	67.56
Vout dB@Cl=100pF	1.10E+05	2.38E+06	86.46
Vout dB@Cl=100uF	1.56E-01	1.74E+00	66.64
Vout dB@Cl=1mF	>1	>1	13.14

Table 8. Super13t OpAmp Frequency Response

	3db Freq (Hz)	Unity Gain Freq (Hz)	Unity Phase (degrees)
Vout dB@Cl=1fF	1.14E+08	5.98E+08	64.43
Vout dB@Cl=10fF	1.14E+08	5.98E+08	64.55
Vout dB@Cl=50fF	1.14E+08	4.37E+08	70.30
Vout dB@Cl=100fF	1.14E+08	4.37E+08	69.28
Vout dB@Cl=1pF	6.55E+07	1.98E+08	67.71
Vout dB@Cl=10pF	7.18E+06	3.77E+07	65.75

3.2.1. Super3t OpAmp

The Super3t OpAmp seen in Figure 23 is made with two regular PMOS transistors, as the differential pair: an active load made with two Super3t NMOS circuits, a current mirror made with two Super3t PMOS transistors. A third Super MOS transistor is used as a resistor to set the reference current. The output stage is a common source amplifier, using a Super3t NMOS and its active load is a Super3t PMOS. The max gain (25.1 dB) of this OpAmp is fairly uniform through the range of the selected load capacitances. Table 7 summarizes the gain and phase response of the OpAmp.

Figure 23. Super 3t OpAmp

3.2.2. Super13t OpAmp

Figure 24 shows the schematic for the Super13t OpAmp. It is similar to the Super3t OpAmp, except that its differential inputs are-sized with a width of 1350nm instead of 810nm as in the Super3t OpAmp. Similarly, it also has a constant max gain of 17.9db. This is less than the Super3t OpAmp because the gain boosting stage was not optimized for gain.

Table 8 lists the pertinent specs for this OpAmp. A note must be made that design constraints in implementing the gain boosting in the Super13t MOS transresistance amplifier results in that the Super13t OpAmp not being able to drive as great a load as the Super3t OpAmp. This can be seen when Table 7 is compared to Table 8.

CHAPTER 4

TESTING RESULTS and COMPARISONS

The testing of the extracted values and figures of the all the circuits was done by measuring five of every fabricated circuit and averaging the results.

4.1. Testing Station.

All of the circuits were measured by an HP4156 Parameter Analyzer. A custom probe card, see Figure 25, along with a Signatone probe state completed the interface to the circuit containing die. Figure 26 shows the complete testing Station, while Figure 27 shows a picture of the die. The die measured 1.5mm x 1.5mm and contained all 14 circuits. The biggest structures visible in figure 27 are the pads that the probe attaches to. Figure 28 is the layout of the pads that the test card interfaced with. Each pad measures 72um by 72um. The entire five pad layout measures 287.19um by 242.865um. Figure 29 is the layout of Figure 26.

Figure 25. Test Card

Figure 26. Testing Station

Figure 27. Fabricated Chip

Figure 28. Probe Pad 5

Figure 29. Pad-Frame Final

4.2. N-Type MOS.

The results of testing the N-Type MOS along with how each of the three circuits compares to each other will be discussed in the below sections. Figures 30 and 31 are the circuit layouts for the Super3t NMOS and Super13t NMOS that were tested. The layout for the Super3t NMOS measures 8.505um by 12.6 um. The layout for the Super13t NMOS measures 9.27um by 13.995 um.

Figure 30. Layout Super3t NMOS

Figure 31. Layout Super13t NMOS

4.2.1. Id vs. Vd – Lambda.

The testing results of the NMOS circuits Id vs. Vd can be seen in Figure 32. Comparing the results seen in Figure 32 to the results in Figure 9 it can clearly be seen that the Super3t NMOS produces the results that were predicted in simulation. The regular MOS results were expected, especially in the saturation region with the runaway current values. The most startling results were that of the Super13t NMOS. The max Id current was significantly lower than what the simulations predicted. Lambda was calculated using equation 2.2. For the lambda results shown in Table 9 the average lambda, minimum lambda, and the average output resistance of the three NMOS circuits, the values when Vgs is equal to zero were excluded and the saturation numbers were taken from a Vds of 0.612V to 1.8V. When Table 9, testing results, is compared to Table 1, simulation results, one can see that the tested lambdas are higher than the simulations predicted. This could be for several reasons. Some of these reasons could be the way that the circuits were tested, the design of the test card, the design of the circuits, and many more reasons. The problem of lambda that was test not matching up to the lambda of simulation is also seen for the P-Type MOS

Table 9. Average Lambda for Testing Results of NMOS, Super3t NMOS, & Super13t NMOS

	Regular NMOS	Super3t NMOS	Super13t NMOS
Ave lambda (sat)	0.215648 V ⁻¹	0.058099 V ⁻¹	0.059602 V ⁻¹
Ave R _{out} (sat) @ 100 uA	46.371 Kohm	172.120 Kohm	167.780 Kohm

Figure 32. Id vs. Vd Testing Results for NMOS, Super3t NMOS, & Super13t NMOS

4.2.2. Id vs. $V_g - V_t$, & G_m

The testing of g_m was done with a V_{ds} of 1.8V instead of the 50mV that was done for the simulations. This was because that the noise inherent in the testing produced unusable results. Using a V_{ds} of 1.8V did produce higher g_m results, but had minimal effect on V_t . This higher V_{ds} was also used to test gamma. Table 10 shows V_t and the max g_m at a V_{sb} of zero volts. When we compare Table 10 with the simulation results of Table 2, we see that the threshold voltage is within 70mV of what was predicted. The maximum g_m is significantly higher, due to the higher V_{ds} used it

still shows that the Regular NMOS and Super13t NMOS are about equal while the Super3t NMOS is shown to be noticeable smaller. This is clearly shown in Figure 33.

Table 10. V_t & G_m for Testing Results of NMOS, Super3t NMOS, & Super13t NMOS

	Regular NMOS	Super3t NMOS	Super13t NMOS
$V_t @ V_{sb}=0V$	0.648V	0.5760V	0.648V
$g_{m_{max}} @ V_{sb}=0V$	$157.051 \times 10^{-3} S$	$151.967 \times 10^{-3} S$	$106.242 \times 10^{-3} S$

Figure 33. I_d vs. V_g & G_m Testing Results for NMOS, Super3t NMOS, & Super13t NMOS

4.3. P-Type MOS.

The results of testing the P-Type MOS along with how each of the three circuits compares to each other will be discussed in the below sections. Figures 34 and 35 are the circuit layouts for the Super3t PMOS and Super13t PMOS that were tested. The layout for the Super3t PMOS measures 12.195um by 7.785 um. The layout for the Super13t PMOS measures 12.285um by 11.025 um.

Figure 34. Layout Super3t PMOS

Figure 35. Layout Super13t PMOS

4.3.1. Id vs. Vd – Lambda.

The testing results for the PMOS circuits produced very interesting results. Firstly the drain current is about 10 times more than simulation predicted. The second observation that can be made from the testing of these circuits is that the Super13t NMOS starts to output reverse current below 0.57V. The reason attributed to this occurrence is that the biasing was not done with the care that it needed. Once the Super13t NMOS drain to source voltage is greater than 0.57V, it follows the Id vs. Vd curves of the PMOS and Super3t PMOS closely, with a slightly less amount of current. These can be seen in Figure 36 below, with Figure 37 showing a close up of the curves from a Vds of -0.6V to -1.8V. The figures were obtained by stepping Vgs from 0V to 1.8V, as seen in figure 37.

The lambda results, as seen in Table 10, are not even close to the results that were expected from simulation. The average lambda of all three circuits is 10 times larger than simulation, and the minimum lambda in saturation is 100 times larger. These directly lead to a lower R_{out} , as seen in Table 11. Looking at the close up view of Lambda, Figure 37, the graphs don't follow the same path, but there slopes are dramatic enough that there lambda will be roughly in the same range.

Table 11. Average Lambda for Testing Results of PMOS, Super3t PMOS, & Super13t PMOS

	Regular PMOS	Super3t PMOS	Super13t PMOS
Ave lambda (sat)	-1.739 V^{-1}	-2.200 V^{-1}	-1.410 V^{-1}
Ave R_{out} (sat) @ 100 μA	5.75 Kohm	4.545 Kohm	7.092 Kohm

Figure 36. I_d vs. V_d Testing Results for PMOS, Super3t PMOS, & Super13t PMOS

Figure 37. Closeup - I_d vs. V_d Testing Results for PMOS, Super3t PMOS, & Super13t PMOS

4.3.2. I_d vs. $V_g - V_t$, & G_m

The g_m of the PMOS circuits was tested exactly as the NMOS circuits were, with a V_{ds} of 1.8V. This also produced a g_m that was significantly higher (equal to or greater than 10 times). Table 12 shows V_t and minimum g_m for the three PMOS circuits; Figure 38 shows the plots of I_d vs. V_g and g_m for all three circuits.

Table 12. V_t & G_m for Testing Results of PMOS, Super3t PMOS, & Super13t PMOS

	Regular PMOS	Super3t PMOS	Super13t PMOS
$V_t @ V_{sb}=0V$	-0.864V	-1.08V	-0.936V
$g_{m_{min}} @ V_{sb}=0V$	$-95.976 \cdot 10^{-6} S$	$-35.449 \cdot 10^{-6} S$	$-32.319 \cdot 10^{-6} S$

Table 12 also shows that the V_t of all three circuits is extremely high. When Table 12 is compared to Table 5, we see that the regular PMOS has a V_t 100mV greater than simulation. For the Super3t PMOS it is 260mV greater, and the Super13t PMOS is 315mV greater than simulation predicted.

Figure 38. I_{ds} vs. V_g & G_m Testing Results for PMOS, Super3t PMOS, & Super13t PMOS

4.4. Current Mirror

The following sections will look at a comparison of the current mirrors made up of the six types of circuits. The N-type circuits will be compared to each other and the P-type circuits will also be compared to each other. The layout of all four current mirrors can be seen in Figures 39 - 40. The NMOS layouts of Figure 39 measures 18.63um by 12.6um and 40 measures 13.95 by 20.16. The PMOS layouts of Figures 41 measures 7.785 by 26.01 and 42 measures 10.98um by 26.505um.

Figure 39. Super3t Current Mirror

Figure 40. Super13t NMOS Current Mirror

Figure 41. Super3t PMOS Current Mirror

Figure 42. Super13t PMOS Current Mirror

4.4.1. Comparisons of Super NMOS Current Mirrors

All the graphs in Figure 43 that have a V_{ds} greater than 0.36V lie within 0.05% of each other. Figure 43 does show that the Super3t NMOS current mirror cannot reach the full range of I_{ref} , 0A to 200uA. Its output current caps out at 175uA. In addition, from this figure we can see that between an I_{ref} of 25uA and 175uA that I_{out} is between 90% and 95% that of I_{ref} . The additional information that can be seen from Figure 44 is that when V_{ds} changes in a range from 0.72V to 1.8V that the I_{out} produces the same amount of current.

The Super13t NMOS current mirror is better at tracking I_{out} to I_{ref} than the Super3t NMOS current mirrors. The problem that can be seen in both Figure 45 and 46 is that its max I_{out} is around 120uA. When we look at the delta between I_{ref} and I_{out} (Figure 45) we see that between 25uA and 120uA that I_{out} is within approximately 5% of I_{ref} . In this sense, the Super13t NMOS current mirror is superior to the Super3t NMOS current mirror. The Super3t NMOS current mirror would offer the best performance if one wanted a wider range of I_{ref} than a standard current mirror, but if one wanted the output current to match the reference current, then the Super13t NMOS current mirror would be the better choice.

Figure 43. I_{out} vs. I_{ref} - Testing Results - Super3t NMOS Current Mirror

Figure 44. $\Delta(I_{ref}/I_{out})$ - Testing Results - Super3t NMOS Current Mirror

Figure 45. I_{out} vs. I_{ref} - Testing Results - Super13t NMOS Current Mirror

Figure 46. Delta (I_{ref}/I_{out}) - Testing Results - Super13t NMOS Current Mirror

4.4.2. Comparisons of Super PMOS Current Mirrors

Neither one of the Super PMOS current mirrors performed equal to their Super NMOS counterparts. This can be seen in both of their I_{out} vs. I_{ref} and Delta figures. Figure 47 shows the results for the Super3t PMOS current mirror. We can see that the best performance was when V_{ds} was equal to or greater than 1.08V. Figure 47 also tells us that when V_{ds} changes on the output transistor that the corresponding output current also changes. The ability of the Super3t PMOS to mirror I_{ref} , as shown in Figure 48, is poor. From Figure 48, we can see that from -200uA to -140uA that I_{out} goes from 0.7 I_{ref} to 0.8 I_{ref} . This means that the Super3t PMOS is useful for a range of I_{ref} from -140uA to 0A. This maximum current of 140uA is short of the 200uA that needs to be tracked.

The Super13t PMOS current mirror (Figure 49) was only able to mirror up to 70uA; this is much less than its Super13t NMOS counterpart, which was able to achieve 120uA. Once I_{ref} reached approximately 75uA, the current mirror saturated and was no longer able to put out any more current. Although this current mirror did better than the Super3t PMOS current mirror in that its delta (Figure 50) from 0.72V to 1.8V was closer to the standard PMOS current mirror, it was still not to the same performance level as the Super13t NMOS versions.

Figure 47. I_{out} vs. I_{ref} - Testing Results - Super3t PMOS Current Mirror

Figure 48. $\Delta (I_{ref}/I_{out})$ - Testing Results - Super3t PMOS Current Mirror

Figure 49. I_{out} vs. I_{ref} - Testing Results - Super13t PMOS Current Mirror

Figure 50. $\Delta(I_{ref}/I_{out})$ - Testing Results - Super13t PMOS Current Mirror

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

It has been shown that a Super NMOS circuit will improve λ when compared to a standard transistor; improving it up to a factor of 4. This then increases the output resistance of the transistor by that same factor. Depending on the specific application, the design trade-offs may not be worth it. Those trade-offs are: a severe loss in the max frequency that can be designed for, an increase of V_t , and an increase of area on the die.

There are several more aspects that need to be studied for these designs. Primarily the Super PMOS circuits will need to be reevaluated as they performed poorly during test. This was reflected in both the transistor and current mirror circuits. Improvements in layout will increase their tested performance. The second point would be to create real world OpAmps. The two OpAmps that were designed were for academic purposes and would be impractical for use in a real-world application. They were made to demonstrate how the Super MOS circuits would function and could be used in a design. Thirdly, one would need to fully take advantage of the gain boosting stage of the Super13t MOS circuits. If this is done, they will be of much greater benefit to future circuit designers. By comparison, the Super3t MOS circuits have one characteristic that makes them superior to the Super13t MOS: they are easier to design, and therefore faster to implement in a final circuit.

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