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Hybrid RFID-Based System Using Active Two-Way Tags

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HYBRID RFID-BASED SYSTEM USING ACTIVE TWO-WAY TAGS

A Thesis

Presented to

The Faculty of the Department of General Engineering

San José State University

In Partial Fulfillment

of the Requirements for the Degree

Master of Science

by

Girish N. Jadhav

December 2010

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The Designated Thesis Committee Approves the Thesis Titled

HYBRID RFID-BASED SYSTEM USING ACTIVE TWO-WAY TAGS

by

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ABSTRACT

HYBRID RFID-BASED SYSTEM USING ACTIVE TWO-WAY TAGS

by Girish N. Jadhav

Ultra High Frequency (UHF) Radio Frequency Identification (RFID) is a promising technology that has experienced tremendous growth by revolutionizing a variety of industry sectors and applications, such as automated data management, the tracking of a specified object, highway toll collection, library inventory tracking, multi-level asset tracking, and airport baggage control. For many RFID applications, it is desired to maximize the operating distance or read range.

This thesis proposes a design of an analog front-end architecture and the baseband controller for a Class-4 Active Two-Way (C4-ATW) RFID tag in order to maximize or increase the tracking range by implementing a tag-hopping technique. In tag-hopping, C4-ATW RFID tags power their own communication with other C4-ATW RFID tags and existing passive RFID tag while the reader's functionality remains unchanged.

The simulation results indicate that the C4-ATW RFID tag can detect a minimum incident RF input power of -20 dBm at a 120 Kbps data rate. For -20 dBm input power; the achieved read range between a reader and tag is 36.7 meters at 4 W of reader power and between two tags, the read range is 2.15 meters at 25 mW tag power. Combined, the analog front end and baseband controller consume 50.3 mW of power and the area of the chip, including pads, is 854 μm x 542 μm .

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CHAPTER 1

INTRODUCTION

Ultra High Frequency (UHF) Radio Frequency Identification (RFID), an automatic wireless information collection/tagging technology that allows an object, place, or person/living being to be automatically identified, is expanding rapidly in many industrial applications. It provides a long operating range or read range, in the order of several meters, which is a vital parameter for many applications.

Despite its wide use, the ability to track an object when it goes out of range has been a major drawback as shown in Figure 1.1.

Figure 1.1. Existing RFID-Based System Using Passive and Active Tags.

In Figure 1.1.

- P-Tag x : P stands for passive tag, x stand for tag number.
- A-Tag x : A stands for active tag, x stand for tag number.
- H-Tag x : H stands for C4-ATW RFID tag, x stand for tag number.

Other tags (e.g., Tag-A, Tag-B, and Tag-C), in Figure 1.1 can be either passive or active tags, which are not within the passive or active tracking range.

The objective of this master's thesis is to study and analyze existing RFID systems and propose an interactive tracking RFID-based system that enables consumers to track items over a wider read range by using enhanced C4-ATW RFID tags that communicate with other tags and power their own communication in order to maximize their read range.

A typical RFID system is comprised of one or more readers that communicate with many transponders (tags). These tags are attached to the objects or persons to be identified or tracked. The two ends of an RFID system are 1) an RFID tag, or transponder, which stores information about an object, and 2) a reader that is typically a stationary system that communicates with the tag. The reader is usually connected to a computer or a network. A tag is a small device consisting of two parts 1) an integrated circuit (IC) that stores and processes information and is capable of modulating and demodulating radio frequency signals, and 2) an antenna for receiving and transmitting the signal.

Each tag contains a silicon chip and antenna, which enable it to receive and respond to radio-frequency queries from RFID readers. In addition, these tags receive both information and operating energy from the RF signal transmitted by the reader. The reader must transmit and receive simultaneously in order to be able to communicate with tags. Three different types of tags exist: passive, active, and semi-passive.

1.1 Passive Tag

A passive tag is comprised of a rectifier, a limiter, power-on-reset circuitry, a demodulator, a modulator, a shift register, and digital control logic, as shown in Figure 1.2. In a passive tag, the reader transmits a modulated RF signal to the tag. The tag receives the incident RF signal that contains both the information and operating energy. The passive tag operates when an electrical current is induced on the tag's antenna by the incident RF signal, which provides just enough power for the tag circuitry to power up and transmits a response. A passive tag transmits its response by backscattering the carrier signal received from the reader. The tag antenna should be capable of extracting power from the incident RF signal as well as transmitting the backscatter signal. The passive tag is distinguished mainly due to its high data rate and small antenna size; it is maintenance free and has an unlimited life time [1].

Figure 1.2. Architecture of a Passive Tag.

1.2 Active Tag

An active tag is composed of the power supply circuitry, power-on-reset circuitry, a demodulator, a modulator, a shift register, and a digital control logic as shown in Figure 1.3. An active tag includes its own internal power supply in the form of a battery used to power the tag's circuitry and generate the backscattering signal. Active tags do not require power from the reader. These tags operate on various frequencies and can have very long reading ranges (i.e., up to 30 meters) [1].

Figure 1.3. Architecture of an Active Tag.

1.3 Semi-Passive Tag

Semi-passive tags are very similar to passive tags except for the addition of a small battery. This battery allows the tag to be constantly powered, which removes the need for the antenna to be designed to collect power from the incoming signal. This allows the antenna to be optimized for the backscattering signal [1].

CHAPTER 2

LITERATURE SURVEY

2.1 Technology Survey

Figure 2.1 shows the achieved performance of other technologies compared with the RFID technology.

Figure 2.1. Technological Survey.

Figure 2.2 shows the achievable performance level of RFID technology across different frequency bands. RFID operating frequencies are located in the low frequency (LF), high frequency (HF), ultra-high frequency (UHF), and microwave bands. A frequency used in very early RFID implementations was the low frequency (LF) band of 125-133 kHz.

Figure 2.2. Achievable RFID Tag Performance across Different Frequency Bands.

The 13.56 MHz band, also known as high frequency (HF), is available in most parts of the world. HF systems are very frequently used for smart shelf applications, access

control, and smart-cards. The 915 MHz band, known as ultra-high frequency (UHF), has a higher range and a faster data transfer rate than HF. Finally, the microwave frequency is 2.45 GHz, although there are some systems available in the 5.8 GHz band. The microwave frequency is the same band as wireless LANs (also known as Wi-Fi) and Bluetooth. Microwave tags have the advantage of being smaller than UHF tags but generally have shorter ranges. Figure 2.3 shows the achieved read range by using passive and active RFID tags. The information is collected from the following references. [2] [4] [5] [6] [7] [8]

Figure 2.3. Achieved Read Range by Using Passive and Active RFID Tags.

2.2 Power Amplifier Survey

Power amplifiers are categorized into different classes according to their circuit configurations and operating conditions, ranging from Class A to Class S. Industry rates the performance of an RF power amplifier in terms of its power gain, efficiency, and linearity. It is important to understand the terminology used in the world of power amplifiers as well as the basic operating principles of different classes of power amplifiers.

The main purpose of a power amplifier is to amplify a transmitted signal so that it can reach the receiver at a specified distance. Depending on the distance between the transmitter and receiver, the output power of a power amplifier is determined. Since a power amplifier dissipates a lot of power, high efficiency is necessary to improve the battery life for wireless applications. If the power efficiency is low, the temperature of the chip will also be increased, which degrades its performance so that an expensive and bulky cooling system may be required. So the power efficiency and linearity of a power amplifier are very important parameters.

Power amplifiers are categorized into linear and nonlinear power amplifiers. Usually, a linear power amplifier has lower power efficiency than a nonlinear power amplifier. There are several types of power amplifiers, namely Classes A, B, AB, C, D, E, and F. Classes A, B, and AB are highly linear power amplifiers, while a Class C power amplifier is partially nonlinear. Class D and Class E power amplifiers are high efficiency, nonlinear switching power amplifiers. A Class F power amplifier is a high efficiency,

nonlinear power amplifier obtained by creating a square-wave overdrive voltage using harmonic shaping. The following section provides the performance summary of Class A, AB, B, C, D, E, and F power amplifiers.

2.2.1 Summary of Different Classes of Power Amplifiers

Efficiency and linearity are the primary considerations when selecting a class of power amplifier. It is very important to understand the specifications of the power amplifier in advance because different applications will result in different choices of power amplifiers. Table 2.1 summarizes the performance of each power amplifier class discussed.

Table 2.1. Performance Summary of Different Power Amplifiers by Classes.

	Linear PA (Current Source)				Non-Linear PA (Switch)		
Mode	Class-A	Class-AB	Class-B	Class-C	Class-D	Class-E	Class-F
Conduction Angle	360°	180°- 360°	180°	< 180°	-	-	-
Ideal Efficiency	50%	50-78%	78%	78-100%	100%	100%	100%
Practical Efficiency	35%	45%	49%	55%	57%	62%	80%
Linearity	Excellent	Good	Moderate	Poor	Poor	Poor	Poor
Output Power	Moderate		Moderate	Small	Large	Large	Large
Gain	Large		Moderate	Small	Small	Small	Small
V _{peak}	2*VDD	2*VDD	2*VDD	2*VDD	2*VDD	3.6*VDD	2*VDD
Normalized Output Power [W] VDD=1V; RL=1Ω	0.5		0.5		0.8106	0.5768	0.6328
Maximum Output Power [W] VDS=1V; RL=1Ω	0.125		0.125		0.2026	0.0455	0.1582

CHAPTER 3

PROPOSED C4-ATW RFID TAG ARCHITECTURE

The existing RFID tag, such as passive and active RFID tags, has two drawbacks. First, the RFID tag can communicate only with readers and cannot communicate with other passive or active RFID tags. Secondly, the limited read range.

To address the above two drawbacks, we propose a C4-ATW RFID tag that can communicate with a reader as well as another C4-ATW RFID tag or passive RFID tag. By using a tag-hopping technique, C4-ATW RFID tags can power their own communication with other C4-ATW RFID tags and existing passive RFID tags to expand/enhance the total read range while the reader's functionality remains unchanged.

The C4-ATW RFID tag architecture is proposed to maximize its read or tracking range. The read range for any tag is primarily limited by the up-link and the distance between the reader and tag. An RFID reader transmits information to a tag by modulating an RF signal in the 860 MHz to 960 MHz frequency range, and the tag receives both information and operating energy from this RF signal. C4-ATW RFID tags receive operating energy either from the reader or from another C4-ATW RFID tag. Therefore, an C4-ATW RFID tag relies on the energy provided by the incident radiation to power up. It must receive sufficient energy to power the tag. The power received by the tag diminishes gradually with distance; hence, tags in close proximity with the reader or another C4-ATW RFID tag are far more likely to have sufficient power for operation when compared with tags that are farther away.

C4-ATW RFID tags perform uplink and downlink functions in addition to repeater functions which retransmit or repeat a reader's or tag's request on to another tag, which effectively leads to an increase in the tracking range.

The reader sends information to one or more tags by modulating an RF carrier using Amplitude Shift Keying (ASK) at a bit rate between 120 kbits/sec and 4 Mbits/sec. If the C4-ATW RFID tag lies within the range of the reader or another C4-ATW RFID tag, an alternating RF voltage is induced on the two-way tag's antenna and is rectified in order to provide a DC supply voltage for tag operation.

The following sections describe the architecture and the communication protocols of an C4-ATW RFID tag.

3.1 Architecture of C4-ATW RFID Tags

The C4-ATW RFID tag architecture is shown in Figure 3.1 and is comprised of a rectifier block, a voltage regulator block, and a demodulator block which receives its operating energy from the reader or another tag. The ring oscillator (i.e., a modulating frequency generator), baseband controller, power amplifier, modulator, and ring VCO (i.e., carrier frequency generator), blocks are powered by an external battery.

The rectifier converts RF energy received by the antenna into the DC voltage for the rectifier, voltage regulator, and demodulator blocks. The rectifier is followed by a voltage regulator that limits and regulates voltage produced by the rectifier. The envelope detector detects and demodulates the reader data and produces the digital demodulated

signal or bit-stream. The ring oscillator generates the modulating frequency for the baseband controller.

Figure 3.1. Architecture of a C4-ATW RFID tag.

The baseband controller decodes the incoming data and generates control signals to compose transmit or repeater packet data. The data is directly fed to the modulator input. The modulator places the modulated data onto the power amplifier and the power amplifier delivers the amplified signal to the antenna for transmission back to the reader or on to another tag.

3.2 Communication Protocols for C4-ATW RFID tags

The EPC C4-ATW RFID tag communication protocol is shown in Figure 3.2. The communication protocol packet consists of a 20-bit power pattern (PWR), a 16-bit synchronization pattern (SYNC), 1 R/T bit indicating if the packet belongs to the reader

Figure 3.2. Proposed Hybrid RFID-based System Using C4-ATW RFID tags.

or a tag, 3 Address-1 bits (ADD1), 3 Address-2 bits (ADD2), and a 16-bit Tag ID pattern.

- If the R/T bit is set to 1, then the respective packet belongs to a tag. The ADD1 field contains the tag's address, and the ADD2 field contains the reader's address.
- If the R/T bit is 0, then the respective packet belongs to the reader, the ADD1 field contains the reader's address, and the ADD2 field contains the tag's address.

There are three types of communication packet transfer protocols:

1. Uplink (Reader-to-tag)
2. Downlink (Tag-to-reader)
3. Repeater (Tag-to-tag) : Repeater uplink and repeater downlink.

3.2.1 Uplink

As shown in Figure 3.3 the uplink carries the reader's data from the reader to the tag.

Figure 3.3. Packet Transfer during Uplink.

3.2.2 Downlink

As shown in Figure 3.4 the downlink carries the tag's data from the tag to the reader.

Figure 3.4. Packet Transfer during Downlink.

Downlink Protocol Example:

If the received RF signal address matches the tag's address, and if the received signal belongs to the tag, then the baseband controller generates a packet which includes tag information, the requester address, the tag address, the packet belonging to the reader, or tag information is transmitted through the power amplifier.

3.2.3 Repeater

If the received RF signal address does not match the tag's address, then the power amplifier retransmits the received signal. A repeater has two types of communication protocols: repeater uplink and repeater downlink.

Repeater Uplink: As shown in Figure 3.5 the repeater uplink carries the reader's data from one tag to another tag, until it finds the corresponding tag.

Figure 3.5. Packet Transfer during Repeater Uplink.

Repeater Downlink: As shown in Figure 3.6 the repeater downlink carries the tag's data from one tag to another tag/reader, until it finds the corresponding reader.

Figure 3.6. Packet Transfer during Repeater Downlink.

Repeater Protocol Example: If a two-way tag's address and the reader requesting the tag address is matched, and then the two-way tag will transmit the tag's information to the reader. If the address does not match, then the two-way tag will perform a repeater operation by transmitting the received signal to another tag.

Figures 3.7 through 3.9 show the communication protocol during uplink and downlink for a valid and invalid C4-ATW RFID tag.

Figure 3.7. Uplink Communications Protocol for Valid Tag.

Figure 3.8. Uplink Communications Protocol for Invalid Tag.

Figure 3.9. Downlink Communications Protocol for a Tag.

3.3 Applications

Typical applications of the C4-ATW RFID Tag technology include multiple levels of asset tracking in warehouses, manufacturing and production lines, library inventory tracking, highway toll collection, access control, airline baggage, and retail applications.

Figure 3.10. Warehouse Application using C4-ATW RFID Tag.

Figure 3.11. Multiple Level Asset Tracking using C4-ATW RFID and Passive Tag.

CHAPTER 4

DESIGN OF CLASS-4 ACTIVE TWO-WAY RFID TAG

This section describes the design and realization/implementation of a compact integrated analog front-end and baseband controller in a 90 nm CMOS process. A C4-ATW RFID tag is a short-distance communication device which operates at a frequency of 912 MHz.

Figure 4.1. Proposed Architecture of Class-4 Active Two-Way RFID tag.

The C4-ATW RFID tag consists of the following sub-blocks: rectifier, voltage regulator, demodulator, ring oscillator, baseband controller, ring voltage controlled oscillator, modulator, and power amplifier, as illustrated in Figure 4.1.

The sub-blocks are as follows:

Rectifier: A rectifier, or voltage multiplier circuit, converts an incident RF signal from the reader (or another tag) to a DC voltage, which is then regulated by a voltage regulator to provide a 1 V supply voltage to the demodulator, ring oscillator, and baseband controller blocks. The voltage multiplier is impedance matched with the antenna in order to ensure the maximum power transfer from the transponder's antenna to the input of the voltage multiplier.

Voltage Regulator: A voltage multiplier converts the input alternating voltage into a DC voltage which is used by a series voltage regulator to provide the regulated voltage required for the correct operation of the transponder.

Demodulator: A demodulator (ASK) sub-block extracts the baseband data bit-stream from the incident RF input signal and delivers the extracted baseband data to the baseband controller sub-block.

Ring Oscillator: The ring oscillator sub-block provides a 4 MHz clock signal to the baseband controller circuit.

Baseband Controller: The tag operates in three modes: LISTEN (i.e., receive), TALK (i.e., transmit), and SLEEP. During LISTEN Mode, the ANT_{SEL} signal from the baseband controller is pulled low and the tag receives an RF signal from either the reader or another tag. During TALK Mode, ANT_{SEL} from the baseband controller is pulled high and the tag transmits the signal to either the reader or another tag through a power amplifier. During SLEEP Mode, the tag is neither receiving nor transmitting a signal to the reader or another tag, and ANT_{SEL} from the baseband controller is pulled high. SLEEP Mode is used to avoid/prevent collision. During power ON, the tag is in LISTEN Mode, and ANT_{SEL} is held low.

Ring Voltage Controlled Oscillator: The voltage controlled oscillator sub-block is used to modulate baseband data using a 912 MHz carrier frequency.

Modulator: The Modulator sub-block modulates the baseband data (BB_{DATA}) using the carrier signal (i.e., $F_C = 912$ MHz), and provides the modulated baseband signal to power amplifier.

Power Amplifier: The power amplifier sub-block amplifies the baseband signal (i.e., BB_{DATA}), before the signal is transmitted/broadcasted through the antenna. Because there are losses in the channel, the signal power should be great enough so the signal remains readable by another tag or reader. Therefore, required design parameters for the selected power amplifier include a high transmit output power level and increased efficiency with moderate linearity at a 1.0 V supply voltage. Since the linearity specification for the power amplifier is somewhat relaxed, non-linear power amplifiers can be used in order to achieve increased efficiency. Also, the output signal (i.e., BB_{DATA}), of the baseband controller is a square wave (i.e., 0-1 V), and the BB_{DATA} signal is the input to the power amplifier.

Antenna Impedance: A matching network is essential in order to match the antenna's impedance with that of the rectifier. The antenna impedance is $50\ \Omega$. Finally, an LC matching network is used to match the input impedance of the tag to that of the antenna for maximum power transfer.

Anti-collision: In order to read multiple tags simultaneously, both tags and readers must be designed to detect when more than one tag is active. Otherwise, the tags may each transmit their modulated carrier signal simultaneously and cause a collision resulting in corrupt data and no data being transferred to the reader or another tag. An anti-collision

block is included in the baseband controller. The timing diagram to prevent collision is shown in Figure 4.2.

Figure 4.2. Timing Diagram to Prevent Collision.

A tag starts transmitting data packets after having received its power in a different time slot that has been selected randomly by each tag ID, and then goes into sleep mode after having sent a data packet.

Read Range: Read range is the maximum distance from which a tag can be detected.

The theoretical read range depends on the power reflection coefficient and can be calculated using the Friis free-space formula as follows:

$$Read\ Range = \frac{\lambda}{4\pi} \sqrt{\frac{P_t G_t G_r \tau}{P_{th}}} \quad (\text{Eq. 4.1})$$

Where, λ = Wavelength

P_t = Transmit Power for the reader or another tag.

G_t = Gain of the transmitting antenna (either reader or tag)

G_r = Gain of the receiving antenna (either reader or tag)

P_{th} = Tag response threshold power or minimum threshold
power necessary to power up the tag

τ = mismatch factor ($0 \leq \tau < 1$)

$$\lambda = \frac{\text{Speed of light}}{\text{Carrier frequency}} \quad (\text{Eq. 4.2})$$

$$\lambda = \frac{3 * 10^8}{912 * 10^6} = 0.329$$

The read range is for C4-ATW RFID tag is determined by:

a. Reader-to-Tag or Tag-to-Tag Read Range:

The maximum distance from which the tag receives (either from a reader or another tag) the minimum power required to turn on the demodulator section.

b. Tag-to-Reader Range:

The maximum distance from which the reader can detect a tag signal.

Table 4.1. Converting dBm to mW.

Value in dBm	$10^{dBm/10}$	Value in mW
-2	$10^{-2/10}$	0.63095
+14	$10^{+14/10}$	25.1188
-20	$10^{-20/10}$	0.01

The read range is dependent on the tag's response threshold power, and the tag's response threshold power is dependent on the transmit/receive data rates.

Example 1: If the modulating frequency (F_M or CLK) is 4 MHz, then transmit and receive data rates are 4 M bits/sec for which the minimum tag response threshold power is -2 dBm. It is assumed there is no mismatch.

- **Calculate the read range from reader to tag:**

Using Equation (4.1)

$$Read\ Range_{[Reader-to-Tag]} = \frac{\lambda}{4\pi} \sqrt{\frac{P_t G_t G_r \tau}{P_{th}}}$$

$$P_t = 4\ W$$

$$G_t = 3$$

$$G_r = 1.64$$

$$P_{th} = 631\ \mu W$$

$$Read\ Range_{[Reader-to-Tag]} = \frac{0.329}{4\pi} \sqrt{\frac{4 \cdot 3 \cdot 1.64}{631\ \mu W}}$$

$$Read\ Range_{[Reader-to-Tag]} = 4.62\ \text{meters (181.8 inch)}$$

- Calculate the read range from one tag to another tag:

Using Equation (4.1)

$$Read\ Range_{[Tag-to-Tag]} = \frac{\lambda}{4\pi} \sqrt{\frac{P_t G_t G_r \tau}{P_{th}}}$$

$$P_t = 25.119\text{ mW}$$

$$G_t = 1.64$$

$$G_r = 1.64$$

$$P_{th} = 631\text{ }\mu\text{W}$$

$$Read\ Range_{[Tag-to-Tag]} = \frac{0.329}{4\pi} \sqrt{\frac{25.119\text{m} \cdot 1.64 \cdot 1.64}{631\text{ }\mu\text{W}}}$$

$$Read\ Range_{[Tag-to-Tag]} = 0.27\text{ meters (10.6 inch)}$$

The achieved read range between reader and tag (i.e., reader-to-tag), is 4.6 meters at 4 W reader power, while the read range between two tags (i.e., tag-to-tag), is 0.27 meters at 25 mW tag power.

Example 2: If the modulating frequency (F_M or CLK) is 120 kHz, then the transmit and receive data rates are 120 kbits/sec for which the minimum tag response threshold power is -20 dBm. It is assumed there is no mismatch.

- **Calculate the read range from reader to tag:**

Using Equation (4.1)

$$Read\ Range_{[Reader-to-Tag]} = \frac{\lambda}{4\pi} \sqrt{\frac{P_t G_t G_r \tau}{P_{th}}}$$

$$P_t = 4\ W$$

$$G_t = 3$$

$$G_r = 1.64$$

$$P_{th} = 10\ \mu W$$

$$Read\ Range_{[Reader-to-Tag]} = \frac{0.329}{4\pi} \sqrt{\frac{4 \cdot 3 \cdot 1.64}{10\ \mu}}$$

$$Read\ Range_{[Reader-to-Tag]} = 36.728\ \text{meters (1445 inch)}$$

- **Calculate the read range from one tag to another tag:**

Using Equation (4.1)

$$Read\ Range_{[Tag-to-Tag]} = \frac{\lambda}{4\pi} \sqrt{\frac{P_t G_t G_r \tau}{P_{th}}}$$

$$P_t = 25.119\ \text{mW}$$

$$G_t = 1.64$$

$$G_r = 1.64$$

$$P_{th} = 10\ \mu W$$

$$Read\ Range_{[Tag-to-Tag]} = \frac{0.329}{4\pi} \sqrt{\frac{25.119m \cdot 1.64 \cdot 1.64}{10\ \mu}}$$

$$Read\ Range_{[Tag-to-Tag]} = 2.15\ \text{meters (85 inch)}$$

The achieved read range between reader and tag (i.e., reader-to-tag), is 36.7 meters at 4 W reader power, while the read range between two tags (i.e., tag-to-tag), is 2.15 meters at 25 mW tag power.

The overall analog front-end and baseband controller circuitry of C4-ATW RFID tag was simulated by using Cadence SpectreTM with 90 nm CMOS process technology.

Figure 4.3. Block Diagram of the Incident Signal Generator.

Figure 4.4. Simulation Test Bench for an C4-ATW RFID tag.

4.1.1 Simulations Results for the C4-ATW RFID tag

The simulation results illustrate how a two-way tag reacts when it receives a valid tag and an invalid tag packet with 1.0 V power supply. The layout area for the C4-ATW RFID tag is $700\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$. The area of the chip, including pads, is $854\text{ }\mu\text{m} \times 542\text{ }\mu\text{m}$ as shown in Figure 3.12.

The waveforms illustrated in Figures 4.5 through 4.7 are in the following order: incident RF input signal (RF_{IN}), demodulator output signal (RX_{OUT}), baseband output signal (BB_{OUT}), modulator output signal (MBB), power amplifier output signal (RF_{OUT}) and antenna select signal (ANT_{SEL}).

Figure 4.5. Uplink Response for a Valid Tag.

Figure 4.6. Uplink Response for an Invalid Tag.

Figure 4.7. Downlink Response for a Tag.

(a)

(b)

Figure 4.8. (a) ISG and (b) Transmitted Uplink Response for a Valid Tag.

(a)

(b)

Figure 4.9. (a) ISG and (b) Transmitted Uplink Response for an Invalid Tag.

Figure 4.10. (a) ISG and (b) Transmitted Downlink Response for a Tag.

Figure 4.11. Floor-plan of C4-ATW RFID tag.

Figure 4.12. Layout of a C4-ATW RFID tag.

4.2 Rectifier

The function of the rectifier is to convert incident RF signal power into a DC voltage, which is then regulated by a voltage regulator to power the two-way tag. Figure 4.13 illustrates the schematic diagram of the rectifier.

The rectifier circuit uses a cascaded Dickson voltage multiplier circuit with multiple cascade sections in order to convert the incoming/incident RF signal power into a DC voltage. The voltage multiplier is the most crucial element of the transponder's design, and its power efficiency directly affects the performance of the system. In this design, a four-stage voltage multiplier is designed using low threshold-voltage PMOSFET device in a diode-connected configuration to provide a 1.3 V output voltage.

Figure 4.13. Schematic of Rectifier.

The rectified DC voltage is stored in a large capacitor and supplied to a 1 V regulator which then powers the two-way tag.

Table 4.2. Rectifier Component Values

Device Name	Optimized Values
MP1 – MP8	$W = 30 \mu\text{m}$, $L = 0.1 \mu\text{m}$, $M = 1$
C1 – C4	1.0 pF
C5 – C8	1.5 pF

4.2.1 Simulations Results for the Rectifier

The simulation results illustrate how the rectifier reacts when it receives a valid tag and an invalid tag packet with 1.0 V power supply. The layout area for the C4-ATW RFID tag is $450 \mu\text{m} \times 100 \mu\text{m}$.

The waveforms illustrated in Figures 4.14 through 4.16 are in the following order: antenna raw signal (ANT_{DATA}), antenna PIE signal (ANT_{PIE}), incident RF input signal (RF_{IN}) and rectified output signal (RECT_{OUT}).

Figure 4.14. Uplink Rectifier Response for Valid Tag.

Figure 4.15. Uplink Rectifier Response for Invalid Tag.

Figure 4.16. Downlink Rectifier Response for a Tag.

Figure 4.17. Layout of the Rectifier.

4.3 Voltage Regulator

A voltage regulator is used to prevent the chip from being damaged due to high input power. Figure 4.18[34, Fig.9.4] shows the schematic diagram of a voltage regulator.

Figure 4.18. Schematic Diagram of the Voltage Regulator. [34, Fig.9.4]

It consists of two parts: the reset circuit block for low power, and the shunt circuit block for high power. Both blocks are self-biased via diode-connected transistors (which work as a voltage divider). The reset circuit block turns off the power supply when the input voltage is lower than the required minimum voltage, and turns it on when the input voltage meets or exceeds the minimum voltage requirement.

All operations are realized by switching on/off PMOS device MP5. Inverter MP2, MN2 is a voltage level detector. When the input voltage increases to a certain level, the output of inverter MP2, MN2 is reversed. Two inverters MP3, MN3, and MP4, MN4

amplify the control signal for MP5 to achieve rail-to-rail swing. The shunt circuit block operates similarly. When the input voltage reaches its maximum, inverter MP1, MN1 reverses its output and the shunt PMOS device MP6 is turned on. Extra current flows through MP6, resulting in a large voltage drop across the rectifier and the power source. Thus, a reasonable output voltage level is maintained for the digital circuit block even at high input power. The combination of these two blocks provides stable voltage regulation. However, this regulator is passive, and any variation in threshold voltage and/or temperature could alter its voltage range.

Table 4.3. Voltage Regulator Component Values.

Device Name	Optimized Values [34]
MP1, MP3, MP4	$W = 0.22 \mu\text{m}$, $L = 4 \mu\text{m}$, $M = 1$
MN1	$W = 0.22 \mu\text{m}$, $L = 7.2 \mu\text{m}$, $M = 1$
MP6	$W = 2 \mu\text{m}$, $L = 0.18 \mu\text{m}$, $M = 20$
MN5-MN8, MN3, MN4	$W = 0.22 \mu\text{m}$, $L = 2 \mu\text{m}$, $M = 1$
MP2	$W = 0.22 \mu\text{m}$, $L = 4 \mu\text{m}$, $M = 1$
MN2	$W = 0.22 \mu\text{m}$, $L = 4.3 \mu\text{m}$, $M = 1$
MP5	$W = 2 \mu\text{m}$, $L = 0.22 \mu\text{m}$, $M = 3$
R_{VG}	200 k Ω

4.3.1 Simulation Results for the Voltage Regulator

The simulation results illustrate how the voltage regulator reacts when it receives a valid tag and an invalid tag packet with 1.0 V power supply. The results also indicate that the current consumption for the voltage regulator is 39.8 μA . The layout area for the voltage regulator is 37 μm x 11 μm excluding resistor R_{VG} .

The waveforms illustrated in Figures 4.19 through 4.21 are in the following order: antenna raw signal (ANT_{DATA}), antenna PIE signal (ANT_{PIE}), incident RF input signal (RF_{IN}), rectified output signal (RECT_{OUT}), and voltage regulator output signal (VREG_{OUT}).

Figure 4.19. Uplink Voltage Regulator Response for Valid Tag.

Figure 4.20. Uplink Voltage Regulator Response for Invalid Tag.

Figure 4.21. Downlink Voltage Regulator Response for a Tag.

Figure 4.22. Transient Current Response of the Voltage Regulator.

Figure 4.23. Layout of the Voltage Regulator.

4.4 Demodulator

Figure 4.24 illustrates a block diagram of the ASK demodulator architecture that is used to extract the baseband data bit-stream from the incident RF input signal.

The ASK demodulator is comprised of an envelope detector, low pass filter, comparator, and buffer to recover baseband data.

Figure 4.24. Block Diagram of the ASK Demodulator.

Figure 4.25. Schematic Diagram of the Envelope Detector.

Envelope Detector:

The envelope detector extracts the carrier wave/signal from the modulated RF envelope signal. The envelope detector uses a structure similar to that of the voltage multiplier with fewer stages. In this design, the envelope detector uses a two-stage voltage multiplier to detect the envelope of the incident RF signal.

Table 4.4 Demodulator Component Values.

Device Name	Optimized Values
MN1-MN4	$W = 10 \mu\text{m}$, $L = 0.1 \mu\text{m}$, $M = 1$
C1, C2	1 pF
C3, C4	1.5 pF

The time constant, $\tau = 1/(R_{ENV}C_{ENV})$, is chosen to allow the output waveform to follow the envelope of the sinusoidal input signal.

Figure 4.26. Cut-off Frequencies of the Carrier, Modulator, LPF, and Envelope Detector.

Figure 4.26 illustrates the cut-off frequencies for the carrier (F_C), modulator (F_M), low pass filter (F_{LPF}), and envelope detector (F_{ENV}).

The values for the resistor and capacitor are chosen such that the time constant ($F_{ENV}=182\text{ MHz}$) is significantly smaller than the carrier frequency ($F_C=912\text{ MHz}$).

The envelope is transferred through a low pass filter to reject all frequencies at the output except for the DC component. The cut-off frequency for the low pass filter is 19 MHz (F_{LPF}).

The output voltage of the low pass filter is then amplified to the generated rail-to-rail baseband signal.

$$F_C = 912\text{ MHz}$$

$$\tau = \frac{F_C}{5} \quad (\text{Eq. 4.3})$$

$$\tau = \frac{912\text{ MHz}}{5} = 182\text{ MHz}$$

$$\tau = \frac{1}{R_{ENV}C_{ENV}} \quad (\text{Eq. 4.4})$$

$$\text{Assume } C_{ENV} = 1\text{ pF}$$

$$R_{ENV} = \frac{1}{182\text{ MHz} \cdot 1\text{ pF}} = 5.49\text{ k}\Omega \approx 5.5\text{ k}\Omega$$

$$F_{ENV} = \frac{1}{2 \cdot \pi \cdot R_{ENV} \cdot C_{ENV}} \quad (\text{Eq. 4.5})$$

$$\text{Assume } C_{LPF} = 1\text{ pF}$$

$$F_{ENV} = \frac{1}{2 \cdot \pi \cdot 5.5\text{ k}\Omega \cdot 1\text{ pF}} = 29\text{ MHz}$$

$$R_{LPF} = 1.5 * R_{ENV} \quad (\text{Eq. 4.6})$$

$$R_{LPF} = 1.5 * 5.5\text{ k}\Omega = 8.22\text{ k}\Omega \approx 8\text{ k}\Omega$$

From Equation 4.5

$$F_{LPF} = \frac{1}{2 \cdot \pi \cdot 8k\Omega \cdot 1pF} = 19.89MHz$$

Figure 4.27. Schematic Diagram of the Comparator and Output Buffer.[34, Fig.9.7]

Table 4.5. Component Values for the Comparator and Output Buffer.

Device Name	Optimized Values
MP1, MP2	W = 0.22 μm , L = 10 μm , M = 1
MN1, MN2	W = 0.22 μm , L = 5 μm , M = 1
MP3	W = 0.22 μm , L = 4 μm , M = 1
MN3	W = 0.22 μm , L = 2 μm , M = 1
MP4	W = 2 μm , L = 0.1 μm , M = 1
MP5, MP7	W = 2 μm , L = 0.1 μm , M = 4
MP6	W = 2 μm , L = 0.1 μm , M = 16
MN4, MN7	W = 1 μm , L = 0.1 μm , M = 1
MN5	W = 1 μm , L = 0.1 μm , M = 4
MN6	W = 1 μm , L = 0.1 μm , M = 16

4.4.1 Simulation Results for the Demodulator

The simulation results illustrate how the demodulator reacts when it receives a valid tag and an invalid tag packet with a 1.0 V power supply. The results also indicate that the current consumption of the comparator is 1.24 μA and the output buffer is 3.376 μA . The layout area for the C4-ATW RFID tag is 42 μm x 10.2 μm .

The waveforms illustrated in Figures 4.28 through 4.30 are in the following order: antenna raw signal (ANT_{DATA}), antenna PIE signal (ANT_{PIE}), incident RF input signal (RF_{IN}), voltage regulator output signal (VREG_{OUT}), envelope detector output signal (ED_{OUT}), low pass filter output signal (LPF_{OUT}), and demodulator output signal (RX_{OUT}).

Figure 4.28. Uplink Demodulator Response for Valid Tag.

Figure 4.29. Uplink Demodulator Response for Invalid Tag.

Figure 4.30. Downlink Demodulator Response for a Tag.

Figure 4.31. Transient Current Response of the Comparator and Output buffer.

Figure 4.32. Layout of the Envelope Detector.

Figure 4.33. Layout of the Comparator and Buffer.

Figure 4.34. Layout of the Demodulator.

4.5 Baseband Controller

The block diagram of the proposed baseband controller (BBC) is illustrated in Figure 4.35. The BBC is comprised of a receive input buffer, transmit output buffer, window detector, ID generator, counters, and control logic.

The received bit-stream data from the demodulator RX_{OUT} is passed to input $DATA_{IN}$ of the BBC and, depending on the RX_{OUT} data, either the receive or repeater packet or the transmit packet is sent to the modulator input.

If the received bit-stream data from the demodulator belongs to the tag, then the BBC composes a transmit packet which includes PWR, SYNC, R/T, ADD1, ADD2, and TAG_ID, and forwards the composed transmit packet to the modulator input. If the received packet from the demodulator does not belong to the respective tag, then the BBC composes a repeater packet depending on the R/T received bit and forwards the composed repeater packet to the modulator input. If the R/T bit is low then the repeater packet includes PWR, SYNC, R/T, ADD1, ADD2, and TAG-ID. If the R/T bit is high, then the repeater packet includes PWR, SYNC, R/T, ADD1, and ADD2.

- **Receive Input Buffer**

The receive input buffer is a Serial-In-Parallel-Out (SIPO) register composed of the TAG-ID, ADD2, ADD1, R/T, SYNC, and PWR fields.

The TAG_ID field is a 16-bit register storing the tag identification number or tag information in which the requester is interested. If the R/T bit is low, the received packet contains TAG-ID and this TAG-ID information is used to retransmit. If the R/T bit is high, the received packet does not contain TAG-ID.

ADD2 field is a 3-bit register and stores the address of the reader or requester.

ADD1 field is a 3-bit register and stores the tag's/sender's address.

R/T field is a 1-bit register that indicates if a packet belong to the reader (R/T=0) or a tag (R/T=1).

If the R/T field is “0,” then the BBC will not assert the TAG_{MATCH}, TX_{LD}, or TX_{EN} signals, and will remain low so that RX_{DATA} is sent to the modulator input. If R/T is “1,” then the following ADD1 field will contain the tag’s address. If ADD1 data is matched with a tag’s address, then the window detector generates a TAG_{MATCH} signal, which in turn initiates or starts creating the transmit packet and enables TX_{EN} so that TX_{DATA} is passed to the modulator input.

The SYNC field is a 16-bit register containing a fixed, user-defined synchronization pattern “0xA55A.” The reader and tag use the same fixed synchronization pattern to communicate with each other. Currently, “0xA55A” is hardcoded, but in the future this value could be programmable.

The PWR field is a 20-bit register containing a fixed pattern, “0xFFFFF,” which helps the tag generate a stable, regulated V_{DD} voltage for the demodulator sub-block before the receive packet begins with the synchronization pattern so that the demodulator can extract the bit-stream/data from the incident RF signal.

- **Transmit Output Buffer**

The transmit buffer is a Parallel-Input-Serial-Output (PISO) register comprised of the TAG_ID, ADD2, ADD1, R/T, SYNC, and PWR fields.

The TAG_ID field is a 16-bit register storing the tag’s identification number or tag’s information in which the requester is interested.

The ADD2 field is a 3-bit register containing the tag's or sender's address.

The ADD1 field is a 3-bit register containing the reader's/requester's address which is loaded from the receive-buffer. The reader address is extracted or decoded from the received packet and is stored in the receive-buffer "LATCH".

The R/T field is a 1-bit register that indicates if the information or the packet belongs to the reader (R/T=0) or the tag (R/T=1). Since ADD1 contains the reader's/requester's address, the R/T bit will be set to "0".

The SYNC and PWR fields perform same operation as explained in receive input buffer section.

Figure 4.36. Schematic Diagram of the Load Generator.

- **Control Signal**

The TX_{EN} signal selects either a transmit packet (TX_{EN} = 1) or receive packet (TX_{EN} = 0) at the input of the modulator block.

Based on the TX_{EN} signal, either TX_{DATA} or RX_{DATA} will be selected. If TX_{EN} is high, then the TX_{DATA} bit-stream is given to the modulator input. Otherwise the RX_{DATA} bit-stream is given to the modulator input. At any given time, either the TX_{DATA} or RX_{DATA} bit-stream is connected to the modulator input.

The window detector is responsible for monitoring the received data and changes the BBC's operating mode from receive mode to transmit mode when the received SYNC pattern is recognized. The output from the receive/repeater-buffer is continuously monitored by the window detector and the main function of the window detector is to generate SYNC_{MATCH} and TAG_{MATCH} control signals.

The SYNC_{MATCH} pulse is generated to indicate that a valid synchronization bit-stream "0xA55A" has been received by the receive-buffer. The TAG_{MATCH} pulse is generated when R/T is high indicating the received packet belongs to the tag and the ADD1 field contains the tag address that should match with the respective tag address ("0x5"). The TAG_{MATCH} signal initiates/enables the creation of the transmit packet. (i.e., enable the ID generator, counters, and control logic.)

After the ID_{DATA} is generated by the "Tag ID Generator" block, a load pulse (TX_{LD}) is generated by the "Load Generator" block to load the transmit buffer (PISO) with TAG_ID, ADD2, ADD1, R/T, SYNC, and PWR information/data. The ANT_{SEL} signal is used to select the tag operation as either transmit or receive mode. By default, the tag is in receive mode, meaning ANT_{SEL} is low.

The SYNC_{MATCH} signal is used to change the tag's operation from receive to transmit mode. When ANT_{SEL} is low, the tag is in receive mode. When ANT_{SEL} is high, the tag is in transmit mode.

The REFRESH signal is used to clear or reset the transmit buffer, receive buffer, counters, control logic, etc., before a new packet arrives.

Figure 4.37. Schematic of the Tag ID Generator.

Figure 4.38. Timing Diagram of Pulse-Interval Encoding (PIE).

Figure 4.39. Uplink Timing Diagram for a Valid Tag.

Figure 4.40. Uplink Timing Diagram for an Invalid Tag.

Figure 4.41. Downlink Timing Diagram for a Tag.

a. For DATA_{PIE} , RX_{PIE} , and ANT_{PIE} (Receiver) signals:

Figure 4.42. Uplink Timing Diagram of DATA_{PIE} , RX_{PIE} , and ANT_{PIE} for a Valid Tag.

Figure 4.43. Uplink Timing Diagram of DATA_{PIE} , RX_{PIE} , and ANT_{PIE} for an Invalid Tag.

Figure 4.44. Downlink Timing Diagram of DATA_{PIE} , RX_{PIE} , and ANT_{PIE} for a Tag.

b. For BB_{PIE} , TX_{PIE} , and ANT_{PIE} (Transmit):

Figure 4.45. Uplink Timing Diagram of BB_{PIE} , TX_{PIE} , and ANT_{PIE} for a Valid Tag.

Figure 4.46. Uplink Timing Diagram of BB_{PIE} , TX_{PIE} , and ANT_{PIE} for an Invalid Tag.

Figure 4.47. Downlink Timing Diagram of BB_{PIE} , TX_{PIE} , and ANT_{PIE} for a Tag.

Table 4.6. Number of Standard Cell Required for the Baseband Controller.

Block Name	NOT	AND2in	OR2in	XOR2in	DDF
RX input buffer [SIPO] (43-bit)					43
TX output buffer [PISO] (59-bit)					59
Tag ID SISO (16 bit)					16
Counter-16					4
Counter-80					7
Counter-45					6
Counter-61					6
Counter-61					6
Latch for ADD2 (3 bits)					3
Latch for R/T (1 bit)					1
Window detector		19			
REG					3
Tag ID generator			1	1	4
Start pulse		1			1
Tag ID SIPO (16-bit)					16
Load generator	2	1			1
Load generator	2	1			1
Control logic	7	10	2		3
Total	11	32	3	1	193

Table 4.7. CMOS 90nm Standard Cell.

STD Cell	Gate Count	Width (μ m)	Height (μ m)	C _{LOAD} (f F)	Power dissipation V _{DD} = 1V, 27 °C
NOT	0.5	0.84	2.52	2.5	$2.4n + (3.7n * 2.5fF) = 2.4nW$
AND2in	1.5	1.4	2.52	2.5	$3.5n + (7.4n * 2.5fF) = 3.5nW$

OR2in	1.5	1.4	2.52	2.5	$5n + (8.7n * 2.5fF) = 5nW$
XOR2in	3	2.8	2.52	2.5	$4.3n + (14.7n * 2.5fF) = 4.3nW$
DFF	6.5	5.6	2.52	2.5	$9.3n + (43.5n * 2.5fF) = 9.3nW$

Table 4.8. Physical Dimensions and Power Dissipation for the Baseband Controller.

STD CELL	BBC	Gate Count	Width (μm)	Height (μm)	WxH (S F.)	Power dissipation $V_{DD} = 1V, 27^\circ C$
NOT	11	5.5	9.24	2.52	23.285	$11 * 2.4nW = 26.4nW$
AND2in	32	48	44.8	2.52	112.896	$32 * 3.5nW = 112nW$
OR2in	3	4.5	4.2	2.52	10.584	$3 * 5nW = 15nW$
XOR2in	1	1.5	2.8	2.52	7.056	$1 * 4.3nW = 4.3nW$
DFF	193	1255	1075.2	2.52	2583.5	$193 * 9.3nW = 1795nW$
Total		1316			2737.3	1.9526μW

Table 3.8 shows that the power dissipation of the baseband controller is 1.9526 μW per MHz. The operating frequency of the baseband controller is 4 MHz, and the estimated power dissipation of the baseband controller is 7.8 $\mu Watts$. The estimated layout area (2737 sf. and 30% for routing) of the baseband controller is 68 μm x 68 μm .

- **Implementation of Baseband Controller in Verilog-RTL**

```

module bb_controller (data_in, clk, reset, bb_pie, ant_sel );
input    data_in;
input    clk;
input    reset;

output    bb_pie;
output    ant_sel;

reg       data_in_ne;
reg [59:0] rx_in_buffer;
reg       rt_lat;
reg [5:0]  div_61_45_count;
reg [6:0]  div_80_count;
reg       ant_sel;
reg       refresh;
reg [2:0]  addr2_lat;
reg [3:0]  div_16_count;
reg       tx_load;
reg [3:0]  tag_id_gen;
reg [15:0] tag_id_sipo;
reg [59:0] tx_out_buffer;
reg [5:0]  div_60_count;
reg       div_60_count_nz_q;
reg       tx_en;

wire [15:0] tag_id;
wire [2:0]  addr2;
wire [2:0]  addr1;
wire       rt;
wire [15:0] sync;
wire [19:0] pwr;
wire       reg_reg;
wire       tag_match;
wire       sync_match;
wire       reset_div_61_45_count;
wire       div_61_45_count_nz;
wire       rx_pie;
wire       tag_id_gen_3_d;
wire       tx_pie;

// Latch data on negedge clock since it is in pie format
always @(negedge clk or posedge reset)
if (reset)
    data_in_ne <= 1'b0;
else
    data_in_ne <= data_in;

always @(posedge clk or posedge reset)
if (reset)

```

```

    rx_in_buffer <= 60'h0;
else if (sync_match)
    rx_in_buffer <= {data_in_ne, rx_in_buffer[59:21], 20'hffffff};
else
    rx_in_buffer <= {data_in_ne, rx_in_buffer[59:1]};

assign tag_id   = rx_in_buffer[59:44];
assign addr2    = rx_in_buffer[43:41];
assign addr1    = rx_in_buffer[40:38];
assign rt       = rx_in_buffer[37];
assign sync     = rx_in_buffer[36:21];
assign pwr      = rx_in_buffer[20:1];
assign reg_reg  = rx_in_buffer[0];

assign tag_match = (addr1 == 3'h5) & (rt == 1'b1) & (sync ==
16'ha55a);
assign sync_match = (sync == 16'ha55a);

always @(posedge clk or posedge reset)
if (reset)
    rt_lat <= 1'b0;
else if (sync_match)
    rt_lat <= rt;

always @(posedge clk or posedge reset)
if (reset)
    div_61_45_count <= 6'h0;
else if (reset_div_61_45_count)
    div_61_45_count <= 6'h0;
else if (sync_match || div_61_45_count_nz)
    div_61_45_count <= div_61_45_count + 1;

assign reset_div_61_45_count = rt_lat ? (div_61_45_count == 6'd45)
: (div_61_45_count == 6'd61);
assign div_61_45_count_nz = (div_61_45_count != 6'h0);
assign rx_pie = div_61_45_count_nz & (rx_in_buffer[0] | ~clk);
//assign rx_pie = (clk ? (div_61_45_count_nz & rx_in_buffer[0]) :
div_61_45_count_nz);

always @(posedge clk or posedge reset)
if (reset)
    div_80_count <= 7'h0;
else if (div_80_count == 7'd80)
    div_80_count <= 7'h0;
else if (sync_match || (div_80_count != 0))
    div_80_count <= div_80_count + 1;

always @(posedge clk or posedge reset)
if (reset)
    ant_sel <= 1'b0;
else if (sync_match)
    ant_sel <= 1'b1;

```

```

else if (div_80_count == 7'd80)
    ant_sel <= 1'b0;

// Generate refresh singal when count == 80
always @(posedge clk or posedge reset)
if (reset)
    refresh <= 1'b0;
else
    refresh <= (div_80_count == 7'd80);

always @(posedge clk or posedge reset)
if (reset)
    addr2_lat <= 3'h0;
else if (tag_match)
    addr2_lat <= addr2;

always @(posedge clk or posedge reset)
if (reset)
    div_16_count <= 4'h0;
else if (div_16_count == 4'd15)
    div_16_count <= 4'h0;
else if (tag_match || (div_16_count != 0))
    div_16_count <= div_16_count + 1;

// Generate tx_load
always @(posedge clk or posedge reset)
if (reset)
    tx_load <= 1'b0;
else
    tx_load <= (div_16_count == 4'd15);

// Tag ID generator
always @(posedge clk or posedge reset)
if (reset)
    tag_id_gen <= 4'h0;
else if (refresh)
    tag_id_gen <= 4'h0;
else
    tag_id_gen <= {tag_id_gen_3_d, tag_id_gen[3:1]};

assign tag_id_gen_3_d = tag_match | (tag_id_gen[0] ^ tag_id_gen[3]);

always @(posedge clk or posedge reset)
if (reset)
    tag_id_sipo <= 16'h0;
else if (tag_match || (div_16_count != 4'h0))
    tag_id_sipo <= {tag_id_gen[0], tag_id_sipo[15:1]};

// TX output buffer
always @(posedge clk or posedge reset)
if (reset)
    tx_out_buffer <= 60'h0;

```

```

else if (tx_load)
    tx_out_buffer <= {tag_id_sipo, addr2_lat, 3'h5, 1'b0, 16'ha55a,
20'hffffff, 1'b0};
else if (div_60_count != 6'h0)
    tx_out_buffer <= {1'b0, tx_out_buffer[59:1]};

always @(posedge clk or posedge reset)
if (reset)
    div_60_count <= 6'h0;
else if (div_60_count == 6'd60)
    div_60_count <= 6'h0;
else if (tx_load || (div_60_count != 6'h0))
    div_60_count <= div_60_count + 1;

always @(posedge clk or posedge reset)
if (reset)
    div_60_count_nz_q <= 1'b0;
else
    div_60_count_nz_q <= (div_60_count != 6'h0);

assign tx_pie = div_60_count_nz_q & (tx_out_buffer[0] | ~clk);

always @(posedge clk or posedge reset)
if (reset)
    tx_en <= 1'b0;
else if (tag_match)
    tx_en <= 1'b1;
else if (refresh)
    tx_en <= 1'b0;

assign bb_pie = tx_en ? tx_pie : rx_pie;

endmodule

```

4.5.1 Simulation Results for the Baseband Controller

The simulation results illustrate how a baseband controller reacts during uplink when a packet received from a valid tag or an invalid tag and during downlink when a packet received from a tag.

4.5.1.1 Generation of Receive Data

The waveforms illustrated in Figures 4.48 through 4.50 are in the following order: baseband controller input signal or demodulator output ($DATA_{IN}$ or RX_{OUT}), synchronization detect signal ($SYNC_{MATCH}$), tag address match signal (TAG_{MATCH}), received data signal (RX_{DATA}), enable signal (EN), transmit data (TX_{DATA}), and refresh or reset signal ($REFRESH$).

Figure 4.48. Uplink Receive Data Response for a Valid Tag.

Figure 4.49. Uplink Receive Data Response for an Invalid Tag.

Figure 4.50. Downlink Receive Data Response for a Tag.

4.5.1.2 Generation of Tag ID Signal

The waveforms illustrated in Figures 4.51 through 4.53 are in the following order: baseband controller input signal or demodulator output ($DATA_{IN}$ or RX_{OUT}), enable signal (EN), start ID generation signal (SP), ID enable signal (ID_{EN}), tag ID data signal (ID_{DATA}), and refresh or reset signal (REFRESH).

Figure 4.51. Uplink Tag ID Response for a Valid Tag.

Figure 4.52. Uplink Tag ID Response for an Invalid Tag.

Figure 4.53. Downlink Tag ID Response for a Tag.

4.5.1.3 Generation of Transmit Data

The waveforms illustrated in Figures 4.54 through 4.56 are in the following order: baseband controller input signal or demodulator output (DATA_{IN} or RX_{OUT}), enable signal (EN), transmit output buffer load signal (TX_{LD}), transmit output buffer enable signal (TX_{EN}), transmit data signal (TX_{DATA}), and refresh or reset signal (REFRESH).

Figure 4.54. Uplink Transmit Data Response for a Valid Tag.

Figure 4.55. Uplink Transmit Data Response for an Invalid Tag.

Figure 4.56. Downlink Transmit Data Response for a Tag.

4.5.1.4 Generation of REFRESH Signal

The waveforms illustrated in Figures 4.57 through 4.59 are in the following order: baseband controller input signal or demodulator output (DATA_{IN} or RX_{OUT}), received data (RX_{DATA}), transmit data (TX_{DATA}), transmit output buffer enable signal (TX_{EN}), antenna select signal (ANT_{SEL}), and refresh or reset signal (REFRESH).

Figure 4.57. Uplink REFRESH Signal Response for a Valid Tag.

Figure 4.58. Uplink REFRESH Signal Response for an Invalid Tag.

Figure 4.59. Downlink REFRESH Signal Response for a Tag.

4.5.1.5 Generation of Raw Baseband Signal

The waveforms illustrated in Figures 4.60 through 4.62 are in the following order: baseband controller input signal or demodulator output (DATA_{IN} or RX_{OUT}), received data (RX_{DATA}), transmit data (TX_{DATA}), transmit enable (TX_{EN}), baseband output signal (BB_{DATA}), and antenna select signal (ANT_{SEL}).

Figure 4.60. Uplink Baseband Output Response for a Valid Tag.

Figure 4.61. Uplink Baseband Output Response for an Invalid Tag.

Figure 4.62. Downlink Baseband Output Response for a Tag.

4.5.1.6 Generation of PIE Baseband Signal

The waveforms illustrated in Figures 4.63 through 4.65 are in the following order: baseband controller input signal or demodulator output in raw data format (RX_{OUT}), baseband controller input signal in PIE format (RX_{OUT}), transmit enable (TX_{EN}), received data (RX_{DATA}), PIE received data (RX_{PIE}), transmit data (TX_{DATA}), PIE transmit data (TX_{PIE}), baseband output signal (BB_{DATA}), and antenna select signal (ANT_{SEL}).

Figure 4.63. Uplink PIE Baseband Output Response for a Valid Tag.

Figure 4.64. Uplink PIE Baseband Output Response for an Invalid Tag.

Figure 4.65. Downlink PIE Baseband Output Response for a Tag.

Figure 4.66. Layout of the Baseband Controller.

4.6 Modulator

Figure 4.67. Block Diagram of the Modulator.

Figure 4.67 illustrates the block diagram of the modulator. The modulator is responsible for modulating the baseband data signal with a carrier frequency (i.e., 912 MHz), signal. The baseband data generated from the baseband controller is transmitted through the power amplifier after modulating the baseband data with the carrier frequency (i.e., 912 MHz). When the baseband data is high, the carrier frequency is amplified by the power amplifier and transmitted. When the baseband data is low, the zero DC voltage is transmitted.

Table 4.9. Modulator Component Values.

Device Name	Optimized Values
MN1	$W = 3 \mu\text{m}$, $L = 0.1 \mu\text{m}$, $M = 1$
N1, N3	$W_p = 2 \mu\text{m}$, $L_p = 100 \text{ nm}$, $M_p = 4$ $W_n = 1 \mu\text{m}$, $L_n = 100 \text{ nm}$, $M_n = 4$
N2, N4	$W_p = 2 \mu\text{m}$, $L_p = 100 \text{ nm}$, $M_p = 8$ $W_n = 1 \mu\text{m}$, $L_n = 100 \text{ nm}$, $M_n = 8$
N5, N6	$W_p = 2 \mu\text{m}$, $L_p = 100 \text{ nm}$, $M_p = 1$ $W_n = 1 \mu\text{m}$, $L_n = 100 \text{ nm}$, $M_n = 1$
TG	$W_p = 3 \mu\text{m}$, $L_p = 100 \text{ nm}$, $M_p = 2$ $W_n = 3 \mu\text{m}$, $L_n = 100 \text{ nm}$, $M_n = 2$

4.6.1 Simulation Results for the Modulator

The simulation results illustrate how the modulator reacts when it receives a valid tag and an invalid tag packet. The results indicate that the current consumption of the modulator is 145 μA , and the layout area for the modulator is 20 μm x 10 μm .

The waveforms illustrated in Figures 4.68 through 4.73 are in the following order: baseband controller input signal or demodulator output (DATA_{IN} or RX_{OUT}), baseband controller output signal (BB_{OUT}), carrier frequency (F_C), modulated baseband signal or modulator output signal (MBB), and antenna select signal (ANT_{SEL}).

Figure 4.68. Uplink Modulator Response for a Valid Tag.

Figure 4.69. Close-up of Uplink Modulator Response for a Valid Tag.

Figure 4.70. Uplink Modulator Response for an Invalid Tag.

Figure 4.71. Close-up of Uplink Modulator Response for an Invalid Tag.

Figure 4.72. Downlink Modulator Response for a Tag.

Figure 4.73. Close-up of Downlink Modulator Response for a Tag.

Figure 4.74. Layout of the Modulator

4.7 Ring Voltage Controlled Oscillator

A current-starved ring voltage controlled oscillator (VCO_{CSR}) is used to modulate baseband data using a 912 MHz carrier frequency. Current-starved ring VCO topologies are used because of their wide frequency range of operation allowing for tunable designs that can easily accommodate the high-speed specifications in an RF application.

The block diagram of a current-starved ring voltage controlled oscillator is shown in Figure 4.75 and includes a bias, output latch, and ring oscillator structure designed using four current-starved delay cells forming a closed loop. A VCO_{CSR} controls the frequency by varying the delay through each stage of the ring. The input control voltage, V_C , sets the current through the bias stage and current mirrors, which subsequently controls the current through the current-starved delay cell of each stage. The output clock frequency is determined by the delay of each delay cell which, in turn, is controlled by a control voltage. A wide oscillator frequency range means a wide tuning range for each delay cell.

The current-starved delay cell is as shown in Figure 4.76. The delay cell is typically a differential pair structure with a tail current. The delay of each cell is controlled by the tail current.

Figure 4.76. Schematic Diagram of a Ring Voltage Controlled Oscillator Cell.

The delay cell includes a pair of PMOS loads transistors, MP1 and MP2. The cross-coupled NMOS gates, MN1 and MN2, control the maximum gate voltage of the PMOS transistor. MN3 and MN4 are a pair of differential inputs. The control voltage is supplied to the gate of NMOS transistors MN5 and MN6. When the control voltage is

changed, the current through the MN5 and MN6 also changes. Also, the gate voltage on MN1 and MN2 varies simultaneously.

Table 4.10. Component Values for the Ring Voltage Controlled Oscillator Cell.

Device Name	Optimized Values
MN1, MN2	$W = 1 \mu\text{m}$, $L = 0.5 \mu\text{m}$, $M = 3$
MN3, MN4	$W = 1 \mu\text{m}$, $L = 0.2 \mu\text{m}$, $M = 4$
MN5	$W = 6 \mu\text{m}$, $L = 0.18 \mu\text{m}$, $M = 1$
MN6	$W = 25 \mu\text{m}$, $L = 0.35 \mu\text{m}$, $M = 3$
MP1, MP2	$W = 11 \mu\text{m}$, $L = 0.21 \mu\text{m}$, $M = 1$
MP3	$W = 11 \mu\text{m}$, $L = 0.21 \mu\text{m}$, $M = 1$

The schematics of the latch and bias circuits are shown in Figure 4.77 and Figure 4.78, respectively.

Figure 4.77. Schematic Diagram of the Ring Voltage Controlled Oscillator Latch.

Table 4.12. Component Values for the Bias Circuit

Device Name	Optimized Values
MN1, MN3	$W = 10 \mu\text{m}$, $L = 2 \mu\text{m}$, $M = 1$
MN2	$W = 20 \mu\text{m}$, $L = 2 \mu\text{m}$, $M = 1$
MN4	$W = 6.5 \mu\text{m}$, $L = 3 \mu\text{m}$, $M = 1$
MN5	$W = 10 \mu\text{m}$, $L = 0.13 \mu\text{m}$, $M = 1$
MN6, MN7	$W = 20 \mu\text{m}$, $L = 6 \mu\text{m}$, $M = 1$
MP1, MP2	$W = 6 \mu\text{m}$, $L = 2 \mu\text{m}$, $M = 1$

Power consumption by the VCO_{CSR} is higher. Future enhancements to the VCO_{CSR} include designing for low power and operating at one fixed frequency. Currently, the VCO_{CSR} is used to generate ASK (PIE) modulation. The same VCO_{CSR} architecture can be also used to generate QPSK modulation.

4.7.1 Simulation Results for the Ring Voltage Controlled Oscillator

The simulation results illustrate the VCO_{CSR} is capable of delivering a 912 MHz output carrier frequency with 1.0 V power supply. The results indicate that the current consumption of the VCO_{CSR} is 4.0739 mA and the layout area for the VCO_{CSR} is $85 \mu\text{m} \times 48 \mu\text{m}$.

The waveforms illustrated in Figures 4.79 and 4.80 are in the following order: control voltage (V_C), VCO_{CSR} output signal (F_C), and current through the VCO_{CSR} ($\text{CSRVCO}_{\text{CURRENT}}$).

Figure 4.79. Transient Response of the Ring VCO.

Figure 4.80. Close-up Transient Response of the Ring VCO.

Figure 4.81. Layout of the Delay Cell.

Figure 4.82. Layout of the Four Delay Cell.

Figure 4.83. Layout of the Latch and Buffer Stages.

Figure 4.84. Layout of the Bias Stage.

Figure 4.85. Layout of the Ring Voltage Controlled Oscillator.

4.8 Ring Oscillator

Figure 4.86. Block Diagram of the Ring Oscillator.

A current-starved 5-stage ring oscillator according to [35] is chosen to generate a 4 MHz clock for the baseband controller.

Figure 4.87. Schematic Diagram for the Ring Oscillator. [35, Fig.2]

As shown in Figure 4.87[35, Fig.2], the transistors MP7 through MP11 and MN8 through MN12 form a classic ring oscillator, PMOS transistors MP1 through MP6 control the upper side current, and NMOS transistors MN1 through MN7 control the lower side current. The delay can be fine-tuned by changing the rate at which the capacitor is charged.

$$F_{OSC} = F_M = \frac{1}{2 \cdot N \cdot \tau} \quad (\text{Eq. 4.7})$$

Where

F_M : Frequency of oscillation or modulating frequency

N : Number of stages.

τ : Delay for one stage which could be given as,

We know the modulating frequency F_M is 4 MHz and the number of stages is 5.

$$\tau = \frac{1}{2 \cdot N \cdot F_M} = \frac{1}{2 \cdot 5 \cdot 4MHz} = 25 \text{ ns}$$

$$\tau = \frac{V_{OCS} \cdot C_{TOTAL}}{I_{OCS}} \quad (\text{Eq. 4.8})$$

Assume the current I_{OCS} through the oscillator is 30 μA .

V_{OCS} is the output voltage, 1 V peak-to-peak.

$$25 \text{ ns} = \frac{1V \cdot C_{TOTAL}}{30 \mu\text{A}}$$

Therefore, $C_{TOTAL} = 750 \text{ fF}$

C_{TOTAL} is the combination of MOSFET gate capacitance C_{gg} and the external capacitor C_L .

$$C_{TOTAL} = C_{gg} + C_L \quad (\text{Eq. 4.9})$$

From the process database we know the C_{gg} is 190 fF

$$C_L = 750 \text{ fF} - 190 \text{ fF}$$

$$C_L = 560 \text{ fF}$$

Table 4.13. Component Values for the Ring Oscillator.

Device Name	Optimized Values
MP1	W = 2 μm , L = 350 nm, M = 1
MP2-MP6	W = 6 μm , L = 350 nm, M = 1
MP7-MP11	W = 5.4 μm , L = 180 nm, M = 1
MN8-MN12	W = 1.8 μm , L = 180 nm, M = 1
MN1, MN2	W = 1 μm , L = 350 nm, M = 1
MN3-MN7	W = 2 μm , L = 350 nm, M = 1

CL	580 fF
N1	W _p = 5.4 μ m, L _p = 180 nm, M _p = 1 W _n = 1.8 μ m, L _n = 180 nm, M _n = 1
N2	W _p = 7.2 μ m, L _p = 180 nm, M _p = 1 W _n = 3.6 μ m, L _n = 180 nm, M _n = 1
N3	W _p = 7.2 μ m, L _p = 180 nm, M _p = 2 W _n = 3.6 μ m, L _n = 180 nm, M _n = 2
N4	W _p = 7.2 μ m, L _p = 180 nm, M _p = 4 W _n = 3.6 μ m, L _n = 180 nm, M _n = 4

4.8.1 Simulation Results for the Ring Oscillator

The simulation results indicate the ring oscillator is capable of delivering 4 MHz output modulating frequency with a 1.0 V power supply. The results also indicate that the current consumption of the ring oscillator is 29.7 μ A and the output buffer is 16.2 μ A. The layout area of the ring oscillator is 60 μ m x 85 μ m and the output buffer is 12 μ m x 16 μ m.

The waveforms illustrated in Figures 4.88 and 4.89 are in the following order: ring oscillator output signal (OSC_{OP}), buffer output signal (F_M), current through the OSC (OSC_{CURRENT}), and current through the output buffer (BUFFER_{CURRENT}).

Figure 4.88. Transient Response of the Ring Oscillator.

Figure 4.89. Close-up Transient Response of the Ring Oscillator.

Figure 4.90. Layout of the Ring Oscillator without Capacitor.

Figure 4.91. Layout of the Output Buffer.

Figure 4.92. Layout of the Ring Oscillator.

4.9 Power Amplifier

Another technique to increase drain efficiency, η , is to use a switching mode power amplifier (i.e., Class-E). The Class-E power amplifier realizes very high efficiency (theoretically 100%) by operating the device as a switch. Several criteria must be satisfied in order for a power amplifier to be categorized as Class-E:

1. The device sustains zero voltage when it carries current.
2. The device carries zero current when it sustains a finite voltage.
3. There is no transition time between the “on” and “off” states of the device.
4. The voltage across the switch remains low when the switch turns off. When the switch turns on, the voltage across the switch should be zero.
5. It is assumed that the transistor behaves as a switching component rather than as a current source

This is also referred as the “non-overlapping-current-and-voltage” condition and underlies all switching-mode amplifiers. One unique feature which distinguishes the Class-E power amplifier from other switching-mode amplifiers is that it requires *zero* slope of the drain (or collector) voltage at the moment when the device turns on. This requirement substantially lowers the sensitivity of the amplifier’s efficiency as a function of component variations and other non-ideal effects in practical implementations.

The circuit topology of a Class-E power amplifier is shown in Figure 4.93. Inductor L_S acts as either an RF choke or a finite DC-feed inductance. Capacitor C_O and inductor L_O are designed to be a series $L_O C_O$ resonator plus an excess inductance L_X at

the frequency of interest. C_S and L_X are designed so that the conditions for Class-E power amplifier operation are satisfied.

Figure 4.93. Circuit Topology of a Class-E Power Amplifier.

Figure 4.94. Voltage and Current Waveforms for a Class-E Power Amplifier.

Figure 4.94 shows the voltage and current waveform at the output and drain of the Class-E power amplifier for an ideal switch. When the drain current is maximized, the drain voltage is zero, and when the drain voltage is maximized, the drain current is zero. That is, the power, which is voltage times current, is zero. So, all power drawn from the DC source is driven into the output node; that is, the Class-E power amplifier theoretically achieves 100% efficiency at the expense of poor linear performance. When the switch is off, a leakage current still flows because of the non-ideal properties of the transistor. The peak drain voltage is approximately $3.6 \cdot V_{DD}$ which increases the stress on the device, especially for low breakdown CMOS processes.

The Class-E power amplifier requires a larger output impedance than other types of power amplifiers. The Class-E power amplifier is suitable for CMOS implementation because Class-E power amplifiers use transistors as switches and CMOS devices are excellent switches. Finally, the drain efficiency of a Class-E power amplifier is greater than that for any other power amplifier.

An C4-ATW RFID tag is a short distance communication device, which operates in the 912 MHz frequency band, and the target requirements for the power amplifier are to achieve a high transmit output power level with increased efficiency and moderate linearity at 1 V supply voltage. Since the linearity specification for the power amplifier is quite relaxed, non-linear power amplifiers can be used to achieve high efficiency. Also, the input signal from the baseband controller is a square wave (i.e., 0-1V), and the BB_{DATA} signal is supplied to the input of the power amplifier.

4.9.1 Design of the 0.9 mW Class-E Power Amplifier

The circuit topology of a single ended Class-E power amplifier, including an output impedance matching network (OIMN), is shown in Figure 4.93. The circuit has been optimized for an output power of 0.9 mW with an operating frequency of 912 MHz at a 1 V supply voltage.

$$F_o = 912 \text{ MHz}$$

$$P_{OUT} = 0.0009 \text{ Watts}$$

$$Q = 9$$

$$V_{DD} = 1.0 \text{ V}$$

$$C_S = \frac{1}{5.447 \cdot \omega \cdot R_L} = \frac{P_{OUT}}{\pi \cdot \omega \cdot V_{DD}^2} \quad (\text{Eq. 4.10})$$

$$C_S = \frac{P_{OUT}}{\pi \cdot (2 \cdot \pi \cdot F_o) \cdot V_{DD}^2} = \frac{0.0009}{\pi \cdot (2 \cdot \pi \cdot 912M) \cdot 1^2} = 49.99 \text{ fF}$$

From Equation (4.10)

$$\begin{aligned} R_L &= \frac{2 \cdot V_{DD}^2}{\left(1 + \frac{\pi^2}{4}\right) \cdot P_{OUT}} \\ &= \frac{2 \cdot 1^2}{5.447 \cdot 0.0009} = 640.89 \, \Omega \end{aligned}$$

$$\begin{aligned} L_S &= \frac{Q \cdot R_L}{2 \cdot \pi \cdot F_o} \\ &= \frac{9 \cdot 640.89}{2 \cdot \pi \cdot 912M} = 1007 \text{ nH} \end{aligned} \quad (\text{Eq. 4.11})$$

$$X = \frac{\pi(\pi^2 - 4) \cdot R_L}{16} \quad (\text{Eq. 4.12})$$

$$= \frac{\pi(\pi^2 - 4) \cdot 640.89}{16} = 738.622 \, \Omega$$

$$\theta = \tan^{-1} \left[\frac{X}{R_L} \right] \quad (\text{Eq. 4.13})$$

$$= \tan^{-1} \left[\frac{738.622}{640.89} \right] = 49.053^\circ = 0.856 \, \text{rad}$$

$$R_{OPT} = \left(\frac{2 \cdot \tan(\theta)}{\sin(2 \cdot \theta)} \right) \cdot R_L \quad (\text{Eq. 4.14})$$

$$= \left(\frac{2 \cdot \tan(49.053)}{\sin(2 \cdot 49.053)} \right) \cdot 640.89 = 1.492 \, k\Omega$$

Assumed $L_0 = 10 \, nH$

$$C_O = \frac{1}{L_0} \left[\frac{1}{2 \cdot \pi \cdot F_O} \right]^2 \quad (\text{Eq. 4.15})$$

$$= \frac{1}{10n} \left[\frac{1}{2 \cdot \pi \cdot 912M} \right]^2 = 3.045 \, pF$$

$$L_X = \frac{X}{2 \cdot \pi \cdot F_O} \quad (\text{Eq. 4.16})$$

$$= \frac{738.622}{2 \cdot \pi \cdot 912M} = 128.9 \, nH$$

To determine the switch size, the switch's on-resistance (R_{ON}) must be at least 10 times smaller than R_L .

$$R_{ON} = \frac{R_L}{10} = \frac{640.89}{10} = 64.089 \, \Omega$$

So, the required width of the NMOS transistor to provide 64.089Ω of R_{on}

$$K_N = 300\mu$$

$$L = 100n$$

$$V_{GS} = 0.65V$$

$$V_{THN} = 0.17V$$

$$W = \frac{L}{R_{ON} \cdot K_N \cdot (V_{GS} - V_{THN})} \quad (\text{Eq. 4.17})$$

$$= \frac{100n}{64.089 \cdot 300\mu \cdot (0.65 - 0.17)} = 10.84 \mu\text{m}.$$

Table 4.14. Component Values of the 0.9 mW Power Amplifier.

Device Name	Calculated Values	Optimized Values
M1 [W1/L1]	W1=10.84 μm , L1=0.1 μm	W1=10 μm , L1=0.1 μm
L_S	1007 nH	1000 nH
C_S	49.99 fF	55.5 fF
L_O	10 nH	10 nH
C_O	3.045 pF	3.045 pF
L_X	128.9 nH	140 nH
R_{OPT}	1492 Ω	1500 Ω

Next, we design the Output Impedance Matching Network (OIMN) for a 60 mW Class-E power amplifier.

Figure 4.95. Schematic of the OIMN for a 0.9 mW Power Amplifier.

Hand calculation of output matching network for a 0.9 mW Class-E power amplifier.

$$Q = 20$$

$$R_{OPT} = 1500 \, \Omega$$

$$R_L = 50 \, \Omega$$

$$Q^2 > \left[\frac{R_{OPT}}{R_L} - 1 \right] \quad (\text{Eq. 4.18})$$

$$400 > \left[\frac{1500}{50} - 1 \right]$$

If the above condition is true

$$X_1 = \frac{R_{OPT}}{Q} \quad (\text{Eq. 4.19})$$

$$= \frac{1500}{20} = 75 \, \Omega$$

$$C_1 = \frac{1}{2 \cdot \pi \cdot F_{OUT} \cdot X_1} \quad (\text{Eq. 4.20})$$

$$= \frac{1}{2 \cdot \pi \cdot 912M \cdot 75 \, \Omega} = 2.33 \, pF$$

$$X_2 = \frac{R_L}{\sqrt{\frac{R_L}{R_{OPT}} (1 + Q^2) - 1}} \quad (\text{Eq. 4.21})$$

$$= \frac{50}{\sqrt{\frac{50}{1500} (1 + 20^2) - 1}} = 14.218$$

$$C_2 = \frac{1}{2 \cdot \pi \cdot F_{OUT} \cdot X_2} \quad (\text{Eq. 4.22})$$

$$= \frac{1}{2 \cdot \pi \cdot 912M \cdot 14.218} = 12.27 \text{ pF}$$

$$X_L = \frac{R_{OPT}}{1 + Q^2} \left[Q + \sqrt{\frac{R_L}{R_{OPT}} (1 + Q^2) - 1} \right] \quad (\text{Eq. 4.23})$$

$$= \frac{1500}{1 + 20^2} \left[20 + \sqrt{\frac{50}{1500} (1 + 20^2) - 1} \right] = 87.967$$

From Equation (4.16)

$$L_1 = \frac{87.967}{2 \cdot \pi \cdot 912M} = 15.35 \text{ nH}$$

Table 4.15. Component Values for the OIMN for a 0.9 mW Power Amplifier.

Device Name	Calculated Values	Optimized Values
R _{OPT}	1500 Ω	1500 Ω
R _L	50 Ω	50 Ω
L ₁	15.25 nH	15.25 nH
C ₁	2.327 pF	2.327 pF
C ₂	12.27 pF	12.27 pF

4.9.1.1 Simulation Results for the 0.9 mW Class-E Power Amplifier

The simulation results indicate the single-ended non-linear Class-E power amplifier is capable of delivering -2.6 dBm of output power to a $50\ \Omega$ load with 1 V power supply and has a power gain of 28 dB at 912 MHz with 82 % power added efficiency (PAE). Linearity is HD2=55.8 dB, HD3=59.2 dB, return loss S22 is -12.6 dB, output voltage is 0.5 V (peak-to-peak), and the power consumption is 0.8 mW.

The waveforms illustrated in Figure 4.96 are in the following order: power amplifier input signal (IN), gate voltage (V_G), drain current (I_D), drain voltage (V_D), and output of the power amplifier (RF_{OUT}).

Figure 4.96. Transient Response for a 0.9 mW Power Amplifier.

Figure 4.97. PAE, Power, and Power Gain for a 10 mW Power Amplifier.

Figure 4.98. Return-loss S22 for a 0.9 mW Power Amplifier.

Figure 4.99. Linearity for a 0.9 mW Power Amplifier.

4.9.2 Design of a 10 mW Class-E Power Amplifier

The circuit topology of a single ended Class-E power amplifier, including an output impedance matching network, is shown in Figure 4.93. The circuit has been optimized for an output power of 10 mW with an operating frequency of 912 MHz at a 1 V supply voltage.

$$F_o = 912 \text{ MHz}$$

$$P_{OUT} = 10 \text{ mWatts}$$

$$Q = 9$$

$$V_{DD} = 1.0 \text{ V}$$

From Equation (4.10)

$$C_S = \frac{P_{OUT}}{\pi \cdot (2 \cdot \pi \cdot Fo) \cdot V_{DD}^2} = \frac{10m}{\pi \cdot (2 \cdot \pi \cdot 912M) \cdot 1^2} = 555.5 \text{ fF}$$

From Equation (4.10)

$$R_L = \frac{\pi \cdot V_{DD}^2}{5.447 \cdot P_{OUT}}$$

$$= \frac{\pi \cdot 1^2}{5.447 \cdot 10m} = 57.68 \Omega$$

From Equation (4.11)

$$L_S = \frac{9 \cdot 57.68}{2 \cdot \pi \cdot 912M} = 90.59 \text{ nH}$$

From Equation (4.12)

$$X = \frac{\pi(\pi^2 - 4) \cdot 57.68}{16} = 66.476 \Omega$$

From Equation (4.13)

$$\theta = \tan^{-1} \left[\frac{66.476}{57.68} \right] = 49.053^\circ \text{C} = 0.856 \text{ rad}$$

From Equation (4.14)

$$R_{OPT} = \left(\frac{2 \cdot \tan(49.053)}{\sin(2 \cdot 49.053)} \right) \cdot 57.68 = 134.293 \Omega$$

Assumed $L_0 = 10 \text{ nH}$

From Equation (4.15)

$$C_O = \frac{1}{10n} \left[\frac{1}{2 \cdot \pi \cdot 912M} \right]^2 = 3.045 \text{ pF}$$

From Equation (4.16)

$$L_X = \frac{66.476}{2 \cdot \pi \cdot 912M} = 11.6 \text{ nH}$$

To determine the switch size, the switch's on resistance (R_{ON}) needs be at least 10 times smaller than R_L .

$$R_{ON} = \frac{R_L}{10} = \frac{57.68}{10} = 5.768 \Omega$$

So, the required width of the NMOS transistor to provide 5.768 Ω of R_{on}

$$K_N = 300\mu$$

$$L = 100n$$

$$V_{GS} = 0.65V$$

$$V_{THN} = 0.17V$$

From Equation (4.17)

$$W = \frac{100n}{5.768 \cdot 300\mu \cdot (0.65 - 0.17)} = 120 \mu m$$

Table 4.16. Component Values of a 10 mW Power Amplifier.

Device Name	Calculated Values	Optimized Values
M1 [W1/L1]	W1=120 μm , L1=0.1 μm	W1=690 μm , L1=0.1 μm
L_S	90.59 nH	100 nH
C_S	555.5 fF	555 fF
L_O	10 nH	10 nH
C_O	3.045 pF	3.045 pF
L_X	11.6 nH	11.6 nH
R_{OPT}	134.293 Ω	134.3 Ω

Next, we design the OIMN for the 10 mW Class-E power amplifier.

Figure 4.100. Schematic of the OIMN for a 10 mW Power Amplifier.

Hand calculation of output matching network for the 10 mW Class-E power amplifier.

$$Q = 10$$

$$R_{OPT} = 134.3 \, \Omega$$

$$R_L = 50 \, \Omega$$

From Equation (4.18)

$$100 > \left[\frac{134.3}{50} - 1 \right]$$

If above condition is true

Then from Equation (4.19)

$$X_1 = \frac{134.3}{10} = 13.43 \, \Omega$$

From Equation (4.20)

$$C_1 = \frac{1}{2 \cdot \pi \cdot 912M \cdot 13.43} = 12.29 \, pF$$

From Equation (4.21)

$$X_2 = \frac{50}{\sqrt{\frac{50}{134.3}(1 + 10^2) - 1}} = 8.264$$

From Equation (4.22)

$$C_2 = \frac{1}{2 \cdot \pi \cdot 912M \cdot 8.264} = 21.12 \text{ pF}$$

From Equation (4.23)

$$X_L = \frac{20}{1 + 10^2} \left[10 + \sqrt{\frac{50}{22.3}(1 + 10^2) - 1} \right] = 21.342$$

From Equation (4.16)

$$L_1 = \frac{21.342}{2 \cdot \pi \cdot 912M} = 3.724 \text{ nH}$$

Table 4.17. Component Values for the OIMN for a 10 mW Power Amplifier.

Device name	Calculated values	Optimized values
R _{OPT}	134.293 Ω	134.3 Ω
R _L	50 Ω	50 Ω
L ₁	3.724 nH	950 pH
C ₁	12.29 pF	12.99 pF
C ₂	21.12 pF	21.12 pF

4.9.2.1 Simulation Results for the 10 mW Class-E Power Amplifier

The simulation results indicate the single-ended Class-E power amplifier is capable of delivering 7.2 dBm of output power to a $50\ \Omega$ load with 1 V power supply and has a power gain of 21.8 dB at 912 MHz with 86 % power added efficiency (PAE). Linearity is HD2=56.6 dB, HD3=58.4 dB, return loss S22 is -17.3 dB, output voltage is 0.9 V (peak-to-peak), and the power consumption is 9.8 mW.

The waveforms illustrated in Figure 4.101 are in the following order: power amplifier input signal (IN), gate voltage (V_G), drain current (I_D), drain voltage (V_D), and output of the power amplifier (RF_{OUT}).

Figure 4.101. Transient Response for a 10 mW Power Amplifier.

Figure 4.102. PAE, Power, and Power Gain for a 10 mW Power Amplifier.

Figure 4.103. Return-loss S22 for a 10 mW Power Amplifier.

Figure 4.104. Linearity for a 10 mW Power Amplifier.

4.9.3 Design of a 60 mW Class-E Power Amplifier

The circuit topology of a single ended Class-E power amplifier (PA), including output impedance matching network, is shown in Figure 4.93. The circuit has been optimized for an output power of 60 mW with an operating frequency of 912 MHz at a 1 V supply voltage.

$$F_o = 912 \text{ MHz}$$

$$P_{OUT} = 60 \text{ mWatts}$$

$$Q = 9$$

$$V_{DD} = 1.0 \text{ V}$$

From Equation (4.10)

$$C_S = \frac{P_{OUT}}{\pi \cdot (2 \cdot \pi \cdot Fo) \cdot V_{DD}^2} = \frac{60m}{\pi \cdot (2 \cdot \pi \cdot 912M) \cdot 1^2} = 3.33 \text{ pF}$$

From Equation (4.10)

$$R_L = \frac{\pi \cdot 1^2}{5.447 \cdot 60m} = 9.613 \Omega$$

From Equation (4.11)

$$L_S = \frac{9 \cdot 9.613}{2 \cdot \pi \cdot 912M} = 15.1 \text{ nH}$$

From Equation (4.12)

$$X = \frac{\pi(\pi^2 - 4) \cdot 9.613}{16} = 11.079 \Omega$$

From Equation (4.13)

$$\theta = \tan^{-1} \left[\frac{11.079}{9.613} \right] = 49.053^\circ \text{C} = 0.856 \text{ rad}$$

From Equation (4.14)

$$R_{OPT} = \left(\frac{2 \cdot \tan(49.053)}{\sin(2 \cdot 49.053)} \right) \cdot 9.613 = 22.382 \Omega$$

Assumed $L_0 = 10 \text{ nH}$

From Equation (4.15)

$$C_O = \frac{1}{10n} \left[\frac{1}{2 \cdot \pi \cdot 912M} \right]^2 = 3.045 \text{ pF}$$

From Equation (4.16)

$$L_X = \frac{11.079}{2 \cdot \pi \cdot 912M} = 1.933 \text{ nH}$$

To determine the switch size, the switch's on resistance (R_{ON}) needs be at least 10 times smaller than R_L .

$$R_{ON} = \frac{R_L}{10} = \frac{9.613}{10} = 0.961 \Omega$$

So, the required width of the NMOS transistor to provide 0.961 Ω of R_{on}

$$K_N = 300\mu$$

$$L = 100n$$

$$V_{GS} = 0.65V$$

$$V_{THN} = 0.17V$$

From Equation (4.17)

$$W = \frac{100n}{0.961 \cdot 300\mu \cdot (0.65 - 0.17)} = 722.4 \mu m$$

Table 4.18. Component Values for a 60 mW Power Amplifier.

Device Name	Calculated Values	Optimized Values
M1 [W1/L1]	W1=722 μm , L1=0.1 μm	W1=600 μm , L1=0.1 μm
L _S	15 nH	15 nH
C _S	3.33 pF	3.33 pF
L _O	10 nH	10 nH
C _O	3.045 pF	3.045 pF
L _X	1.933 nH	2 nH
R _{OPT}	22.382 Ω	22.3 Ω

Next, we design the OIMN for a 60 mW Class-E power amplifier.

Figure 4.105. Schematic of the OIMN for a 60 mW Power Amplifier.

Hand calculation of output matching network for a 60 mW Class-E power amplifier.

$$Q = 10$$

$$R_{OPT} = 22.3 \, \Omega$$

$$R_L = 50 \, \Omega$$

From Equation (4.18)

$$10^2 > \left[\frac{22.3}{50} - 1 \right]$$

If above condition is true

From Equation (4.19)

$$X_1 = \frac{22.3}{10} = 2.23 \, \Omega$$

From Equation (4.20)

$$C_1 = \frac{1}{2 \cdot \pi \cdot 912M \cdot 2.23} = 78.26 \, pF$$

From Equation (4.21)

$$X_2 = \frac{50}{\sqrt{\frac{50}{22.3}(1 + 10^2) - 1}} = 3.33$$

From Equation (4.22)

$$C_2 = \frac{1}{2 \cdot \pi \cdot 912M \cdot 3.33} = 52.41 \text{ pF}$$

From Equation (4.23)

$$X_L = \frac{20}{1 + 10^2} \left[10 + \sqrt{\frac{50}{22.3}(1 + 10^2) - 1} \right] = 5.523$$

From Equation (4.16)

$$L_1 = \frac{5.523}{2 \cdot \pi \cdot 912M} = 963.9 \text{ pH}$$

Table 4.19. Component Values for the OIMN for a 60mW Power Amplifier.

Device Name	Calculated Values	Optimized Values
R _{OPT}	22.3 Ω	22.3 Ω
R _L	50 Ω	50 Ω
L ₁	963.9 pH	950 pH
C ₁	78.26 pF	75.875 pF
C ₂	52.4 pF	51.6 pF

4.9.3.1 Simulation Results for a 60 mW Class-E Power Amplifier

The simulation results indicate the non-linear Class-E power amplifier is capable of delivering 14.1 dBm of output power to a $50\ \Omega$ load with a 1 V power supply and has a power gain of 24.1 dB at 912 MHz with 80% power added efficiency (PAE). Linearity is $HD_2=68.6\text{ dB}$, $HD_3=53.3\text{ dB}$, return loss S_{22} is -12.5 dB, output voltage is 3.6 V (peak-to-peak), and the power consumption is 46.6 mW. The layout area for the power amplifier is $680\ \mu\text{m} \times 370\ \mu\text{m}$.

The waveforms illustrated in Figure 4.106 are in the following order: power amplifier input signal (IN), gate voltage (V_G), drain current (I_D), drain voltage (V_D), and output of the power amplifier (RF_{OUT}).

Figure 4.106. Transient Response for a 60 mW Power Amplifier.

Figure 4.107. PAE, Power and Power Gain for a 60 mW Power Amplifier.

Figure 4.108. Return-loss S22 for a 60 mW Power Amplifier.

Figure 4.109. Linearity for a 60 mW Power Amplifier.

Figure 4.110. Layout of a 60 mW Power Amplifier.

4.9.4 Summary of Achieved Results for Class-E Power Amplifiers

Table 4.20. Component Values for a PA Delivering Different Output Power Levels.

Parameter	Power Amplifier Design		
P_{OUT}	0.9 mW	10 mW	60 mW
L_S	1000 nH	100 nH	15 nH
C_S	55.5 fF	555 fF	3.33 pF
L_O	10 nH	10 nH	10 nH
C_O	3.045 pF	3.045 pF	3.045 pF
L_X	140 nH	11.6 nH	2 nH
R_{OPT}	1500 Ω	134.3 Ω	22.3 Ω
M1 [W1/L1]	W1 = 10 μm , L1 = 0.1 μm	W1 = 690 μm , L1 = 0.1 μm	W1 = 600 μm , L1 = 0.1 μm

Table 4.21. Output Impedance Matching.

Parameters	Output Matching Network Design		
P_{OUT}	0.9mW	10mW	60mW
Q	20	10	10
R_L	50 Ω	50 Ω	50 Ω
L_1	15.25 nH	3.633 nH	950 pH
C_1	2.327 pF	12.99 pF	75.875 pF
C_2	12.27 pF	21.12 pF	51.6 pF

Table 4.22. Summary of the Three Power Amplifier's Achieved Performance.

Parameters	Power Amplifier		
	P_{OUT}	10mW	60mW
Technology	90 nm CMOS	90 nm CMOS	90 nm CMOS
Signal Frequency	912 MHz	912 MHz	912 MHz
Signal Bandwidth	10 MHz	10 MHz	10 MHz
Supply Voltage	1.0 V	1.0 V	1.0 V
Power Dissipation	0.8 mW	9.8 mW	46.6 mW
V _{OUT} (peak-to-peak)	0.5 V	0.9 V	3.6 V
PAE (Efficiency)	83 %	86 %	80 %
Output Power	-2.6 dBm	7.2 dBm	14.1 dBm
Power Gain	28 dB	21.8 dB	24.1 dB
Return loss S22	-12.6 dB	-17.7dB	-13.8 dB
HD2	55.8 dB	56.6 dB	68.6 dB
HD3	59.2 dB	58.4 dB	53.3 dB

Table 4.23. Comparison of Achieved Power Amplifier Performance.

Reference	Process	VDD	Frequency	Pout	PAE
[14]	0.35μm CMOS	1.5 V	403 MHz	20.4 dBm	65.6%
[16]	0.25μm CMOS	1.8 V	900 MHz	29.5 dBm	41.0%
[19]	0.18μm CMOS	1.8 V / 2.5 V	915 MHz	20.0 dBm	32.1%
[23]	CMOS	1.9 V	900 MHz	30.0 dBm	41.0%
[28]	CMOS	3 V	900 MHz	19.3 dBm	30.0%
This work	90nm CMOS	1.0 V	912 MHz	14.1 dBm	80%
This work	90nm CMOS	1.0 V	912 MHz	7.2 dBm	86%
This work	90nm CMOS	1.0 V	912 MHz	-2.6 dBm	82%

4.10 Summary of Achieved Results for an C4-ATW RFID tag

Table 4.24. Achieved Results for an C4-ATW RFID tag.

C4-ATW RFID tag	Power Consumption	Layout Dimension (width x height)
Rectifier	0 W	450 μm x 40 μm
Voltage regulator	39.8 μW	37 μm x 11 μm
Demodulator	1.24 μW	265 μm x 80 μm
Ring oscillator	29.7 μW	77 μm x 85 μm
Ring oscillator buffer	16.2 μW	12.5 μm x 16 μm
Ring voltage controlled oscillator	4.1 mW	85 μm x 48 μm
Modulator	145 μW	20 μm x 10 μm
Power amplifier with 60mW	46 mW	680 μm x 370 μm
Baseband controller	6.4 μW	98 μm x 98 μm
C4-ATW RFID tag	50.3 mW	854 μm x 542 μm

CHAPTER 5

CONCLUSIONS

In this thesis, a novel class-4 active two-way RFID tag has been proposed to address two drawbacks. First, the RFID tag can communicate only with readers and cannot communicate with other passive or active RFID tags. Second, the limited read range.

The C4-ATW RFID tag can communicate with reader as well as other C4-ATW RFID tags or passive RFID tags. By using a tag-hopping technique, C4-ATW RFID tags can power their own communication with other C4-ATW RFID tags and existing passive RFID tags to expand/enhance the total read range.

The 1V C4-ATW RFID tag has been designed using a 90 nm 1P9M standard CMOS process which operates in the 912 MHz band. The simulation results indicate that the active two way RFID tag can detect a minimum incident RF input power of -2 dBm at a 4 Mbps data rate, or -20 dBm at a 120 kbps data rate. For -2 dBm input power, the achieved read range between the reader and tag is 4.6 meters at 4 W of reader power, and between two tags, the read range is 0.27 meters at 25 mW of tag power. For -20 dBm input power, the achieved read range between a reader and tag is 36.7 meters at 4 W of reader power and between two tags, the read range is 2.15 meters at 25 mW tag power. Combined, the analog front-end and baseband controller consume 50.3 mW of power, and the area of the chip, including pads, is 854 μm x 542 μm

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APPENDIX A : IMPLEMENTATION OF BASEBAND CONTROLLER

In Appendix A we will implement behavioral models of incident signal generator and baseband controller using Verilog-A.

A.1. Implementation of Incident Signal Generator Using Verilog-A.

Verilog-A code for “PATTERN-i BUFFER [PISO]”

```
module a_RX_PISO_PATTERN_1ANT (  
    vin_d0,vin_d1,vin_d2,vin_d3,vin_d4,vin_d5,vin_d6,vin_d7,vin_d8,vin_d9,vin_d10,vin_  
    d11,vin_d12,vin_d13,vin_d14,vin_d15,vin_d16,vin_d17,vin_d18,vin_d19,vin_d20,vin_d  
    21,vin_d22,vin_d23,vin_d24,vin_d25,vin_d26,vin_d27,vin_d28,vin_d29,vin_d30,vin_d3  
    1,vin_d32,vin_d33,vin_d34,vin_d35,vin_d36,vin_d37,vin_d38,vin_d39,vin_d40,vin_d41  
    ,vin_d42,vin_d43,vin_d44,vin_d45,vin_d46,vin_d47,vin_d48,vin_d49,vin_d50,vin_d51,  
    vin_d52,vin_d53,vin_d54,vin_d55,vin_d56,vin_d57,vin_d58,vin_d59,vin_d60,vin_d61,v  
    in_d62,vin_d63,vin_d64,vin_d65,vin_d66,vin_d67,vin_d68,vin_d69,vin_d70,vin_d71,vi  
    n_d72,vin_d73,vin_d74,vin_d75,vin_d76,vin_d77,vin_d78,vin_d79,vin_d80,vin_d81,vin_  
    _d82,vin_d83,vin_d84,vin_d85,vin_d86,vin_d87,vin_d88,vin_d89,vin_d90,vin_d91,vin_  
    _d92,vin_d93,vin_d94,vin_d95,vin_d96,vin_d97,vin_d98,vin_d99,vin_d100,vin_d101,vin_  
    _d102 ,vin_d ,vout_d ,vclk ,vload);  
  
    electrical vin_d0,vin_d1,vin_d2,vin_d3,vin_d4,vin_d5,vin_d6,vin_d7,vin_d8,vin_d9,  
    vin_d10,vin_d11,vin_d12,vin_d13,vin_d14,vin_d15,vin_d16,vin_d17,vin_d18,vin_d19,v  
    in_d20,vin_d21,vin_d22,vin_d23,vin_d24,vin_d25,vin_d26,vin_d27,vin_d28,vin_d29,vi  
    n_d30,vin_d31,vin_d32,vin_d33,vin_d34,vin_d35,vin_d36,vin_d37,vin_d38,vin_d39,vin_  
    _d40,vin_d41,vin_d42,vin_d43,vin_d44,vin_d45,vin_d46,vin_d47,vin_d48,vin_d49,vin_  
    _d50,vin_d51,vin_d52,vin_d53,vin_d54,vin_d55,vin_d56,vin_d57,vin_d58,vin_d59,vin_d  
    60,vin_d61,vin_d62,vin_d63,vin_d64,vin_d65,vin_d66,vin_d67,vin_d68,vin_d69,vin_d7  
    0,vin_d71,vin_d72,vin_d73,vin_d74,vin_d75,vin_d76,vin_d77,vin_d78,vin_d79,vin_d80  
    ,vin_d81,vin_d82,vin_d83,vin_d84,vin_d85,vin_d86,vin_d87,vin_d88,vin_d89,vin_d90,  
    vin_d91,vin_d92,vin_d93,vin_d94,vin_d95,vin_d96,vin_d97,vin_d98,vin_d99,  
    vin_d100,vin_d101,vin_d102,vin_d,vclk,vout_d,vload;  
  
    parameter real vlogic_high = 1;  
    parameter real vlogic_low = 0;  
    parameter real vtrans = 0.5;  
    parameter real tdel = 200p from [0:inf);  
    parameter real trise = 20p from (0:inf);  
    parameter real tfall = 20p from (0:inf);
```

```

integer d[0:102];
integer bit_num, enable;

analog begin
  @ ( cross ( V(vload) - vtrans, -1, 1.0, vload.potential.abstol))
  begin
    enable = 1;
    d[0] = V(vin_d0) > vtrans;
    d[1] = V(vin_d1) > vtrans;
    d[2] = V(vin_d2) > vtrans;
    d[3] = V(vin_d3) > vtrans;
    d[4] = V(vin_d4) > vtrans;
    d[5] = V(vin_d5) > vtrans;
    d[6] = V(vin_d6) > vtrans;
    d[7] = V(vin_d7) > vtrans;
    d[8] = V(vin_d8) > vtrans;
    d[9] = V(vin_d9) > vtrans;
    d[10] = V(vin_d10) > vtrans;
    d[11] = V(vin_d11) > vtrans;
    d[12] = V(vin_d12) > vtrans;
    d[13] = V(vin_d13) > vtrans;
    d[14] = V(vin_d14) > vtrans;
    d[15] = V(vin_d15) > vtrans;
    d[16] = V(vin_d16) > vtrans;
    d[17] = V(vin_d17) > vtrans;
    d[18] = V(vin_d18) > vtrans;
    d[19] = V(vin_d19) > vtrans;
    d[20] = V(vin_d20) > vtrans;
    d[21] = V(vin_d21) > vtrans;
    d[22] = V(vin_d22) > vtrans;
    d[23] = V(vin_d23) > vtrans;
    d[24] = V(vin_d24) > vtrans;
    d[25] = V(vin_d25) > vtrans;
    d[26] = V(vin_d26) > vtrans;
    d[27] = V(vin_d27) > vtrans;
    d[28] = V(vin_d28) > vtrans;
    d[29] = V(vin_d29) > vtrans;
    d[30] = V(vin_d30) > vtrans;
    d[31] = V(vin_d31) > vtrans;
    d[32] = V(vin_d32) > vtrans;
    d[33] = V(vin_d33) > vtrans;
    d[34] = V(vin_d34) > vtrans;
  end
end

```

```

d[35] = V(vin_d35) > vtrans;
d[36] = V(vin_d36) > vtrans;
d[37] = V(vin_d37) > vtrans;
d[38] = V(vin_d38) > vtrans;
d[39] = V(vin_d39) > vtrans;
d[40] = V(vin_d40) > vtrans;
d[41] = V(vin_d41) > vtrans;
d[42] = V(vin_d42) > vtrans;
d[43] = V(vin_d43) > vtrans;
d[44] = V(vin_d44) > vtrans;
d[45] = V(vin_d45) > vtrans;
d[46] = V(vin_d46) > vtrans;
d[47] = V(vin_d47) > vtrans;
d[48] = V(vin_d48) > vtrans;
d[49] = V(vin_d49) > vtrans;
d[50] = V(vin_d50) > vtrans;
d[51] = V(vin_d51) > vtrans;
d[52] = V(vin_d52) > vtrans;
d[53] = V(vin_d53) > vtrans;
d[54] = V(vin_d54) > vtrans;
d[55] = V(vin_d55) > vtrans;
d[56] = V(vin_d56) > vtrans;
d[57] = V(vin_d57) > vtrans;
d[58] = V(vin_d58) > vtrans;
d[59] = V(vin_d59) > vtrans;
d[60] = V(vin_d60) > vtrans;
d[61] = V(vin_d61) > vtrans;
d[62] = V(vin_d62) > vtrans;
d[63] = V(vin_d63) > vtrans;
d[64] = V(vin_d64) > vtrans;
d[65] = V(vin_d65) > vtrans;
d[66] = V(vin_d66) > vtrans;
d[67] = V(vin_d67) > vtrans;
d[68] = V(vin_d68) > vtrans;
d[69] = V(vin_d69) > vtrans;
d[70] = V(vin_d70) > vtrans;
d[71] = V(vin_d71) > vtrans;
d[72] = V(vin_d72) > vtrans;
d[73] = V(vin_d73) > vtrans;
d[74] = V(vin_d74) > vtrans;
d[75] = V(vin_d75) > vtrans;
d[76] = V(vin_d76) > vtrans;

```

```

d[77] = V(vin_d77) > vtrans;
d[78] = V(vin_d78) > vtrans;
d[79] = V(vin_d79) > vtrans;
d[80] = V(vin_d80) > vtrans;
d[81] = V(vin_d81) > vtrans;
d[82] = V(vin_d82) > vtrans;
d[83] = V(vin_d83) > vtrans;
d[84] = V(vin_d84) > vtrans;
d[85] = V(vin_d85) > vtrans;
d[86] = V(vin_d86) > vtrans;
d[87] = V(vin_d87) > vtrans;
d[88] = V(vin_d88) > vtrans;
d[89] = V(vin_d89) > vtrans;
d[90] = V(vin_d90) > vtrans;
d[91] = V(vin_d91) > vtrans;
d[92] = V(vin_d92) > vtrans;
d[93] = V(vin_d93) > vtrans;
d[94] = V(vin_d94) > vtrans;
d[95] = V(vin_d95) > vtrans;
d[96] = V(vin_d96) > vtrans;
d[97] = V(vin_d97) > vtrans;
d[98] = V(vin_d98) > vtrans;
d[99] = V(vin_d99) > vtrans;
d[100] = V(vin_d100) > vtrans;
d[101] = V(vin_d101) > vtrans;
d[102] = V(vin_d102) > vtrans;
end

@ (cross( V(vclk) - vtrans, +1, 1.0, vclk.potential.abstol) )
begin
    if (enable == 1)
        begin
            for (bit_num = 102; bit_num > 0; bit_num = bit_num-1)
                d[bit_num] = d[bit_num-1];
            d[0] = V(vin_d) > vtrans;
        end
    end
    V(vout_d) <+ transition((d[102] ? vlogic_high : vlogic_low),tdel,trise,tfall);
end
endmodule

```

A.2. Implementation of Baseband Controller using Verilog-A

A.2.1. Verilog-A code for “COUNTER (DIV-16)”

```
module a_divider_16_en(OUT, IN, EN);
input  IN, EN;
output OUT;
electrical IN, EN, OUT;

parameter real Vlo=0,Vhi=1.0;
parameter vth = 0.5;
parameter integer dir=1 from [-1:1] exclude 0;
parameter real tr=20p from (0:inf);
parameter real tf=20p from (0:inf);
parameter real ttol=0.0001p from (0:inf);

integer count, n, seed, selector;
real dt,ratio;

analog begin
    selector = (V(EN) > vth) ? 1: 0;
    @ (cross(V(EN) - vth, +1.0, 1.0, EN.potential.abstol))
        selector = 1;
    @ (cross(V(EN) - vth, -1.0, 1.0, EN.potential.abstol))
        selector = 0;
    if (selector == 1)
        count=count;
    else
        count=0;
    @(initial_step) seed=-311;

    @(cross(V(IN)-0.5, dir, ttol))
    begin
        if (count == 17)
            count=count;
        else
            count=count+1;

            if (count == 17)
                n=0;
            else if (selector == 0)
```



```

        n=0;
    else
        n=1;
    end
    V(OUT) <+ transition(n ? Vhi: Vlo, 0.0, tr, tf);
end
endmodule

```

A.2.2. Verilog-A code for “Start Pulse”

```

module a_start_pulse(SP_OUT, SP_IN, SP_EN);
input  SP_IN, SP_EN;
output SP_OUT;
electrical SP_IN, SP_EN, SP_OUT;

parameter real Vlo=0,Vhi=1.0;
parameter vth = 0.5;
parameter integer dir=1 from [-1:1] exclude 0;
parameter real tr=20p from (0:inf);
parameter real tf=20p from (0:inf);
parameter real ttol=0.0001p from (0:inf);

integer count, n, seed, selector;
real dt,ratio;

analog begin
    selector = (V(SP_EN) > vth) ? 1: 0;
    @ (cross(V(SP_EN) - vth, +1.0, 1.0, SP_EN.potential.abstol))
        selector = 1;
    @ (cross(V(SP_EN) - vth, -1.0, 1.0, SP_EN.potential.abstol))
        selector = 0;
    if (selector == 1)
        count=count;
    else
        count=0;

    @(initial_step) seed=-311;

    @(cross(V(SP_IN)-0.5, dir, ttol))
begin
    if (count == 2)
        count=count;

```

```

        else
            count=count+1;

        if (count == 2)
            n=0;
        else if (selector == 0)
            n=0;
        else
            n=1;
    end

    V(SP_OUT) <+ transition(n ? Vhi: Vlo, 0.0, tr, tf);
end
endmodule

```

A.2.3. Verilog-A code for “COUNTER (DIV-80)”

```

module a_Transmit_pulse_1ANT(TX_PULSE_OUT, TX_PULSE_IN,
TX_PULSE_EN);
input  TX_PULSE_IN, TX_PULSE_EN;
output TX_PULSE_OUT;
electrical TX_PULSE_IN, TX_PULSE_EN, TX_PULSE_OUT;

parameter real Vlo=0,Vhi=1.0;
parameter vth = 0.5;
parameter integer dir=1 from [-1:1] exclude 0;
parameter real tr=20p from (0:inf);
parameter real tf=20p from (0:inf);
parameter real ttol=0.0001p from (0:inf);

integer count, n, seed, selector;
real dt,ratio;

analog begin
    selector = (V(TX_PULSE_EN) > vth) ? 1: 0;
    @ (cross(V(TX_PULSE_EN) - vth, +1.0, 1.0, TX_PULSE_EN.potential.abstol))
        selector = 1;
    @ (cross(V(TX_PULSE_EN) - vth, -1.0, 1.0, TX_PULSE_EN.potential.abstol))
        selector = 0;

    if (selector == 1)
        count=count;

```

```

else
    count=0;

@(initial_step) seed=-311;
@(cross(V(TX_PULSE_IN)-0.5, dir, ttol))
begin
    if (count == 80)
        count=count;
    else
        count=count+1;
    if (count == 80)
        n=0;
    else if (selector == 0)
        n=0;
    else
        n=1;
end

V(TX_PULSE_OUT) <+ transition(n ? Vhi: Vlo, 0.0, tr, tf);
end
endmodule

```

A.2.4. Verilog-A code for “COUNTER (DIV-64)”

```

module a_TX_COMPLETE_1ANT(TX_COMPLETE, IN_CLK);
input  IN_CLK;
output TX_COMPLETE;
electrical IN_CLK, TX_COMPLETE;

parameter real Vlo=0,Vhi=1.0;
parameter vth = 0.5;
parameter integer dir=+1 from [-1:1] exclude 0;
parameter real tr=20p from (0:inf);
parameter real tf=20p from (0:inf);
parameter real ttol=0.0001p from (0:inf);

integer count, n, seed;
real dt,ratio;

analog begin
    @(initial_step) seed=-311;
    @(cross(V(IN_CLK)-0.5, dir, ttol))

```

```

begin
    if (count == 64)
        count=0;
    else
        count=count+1;
    if (count == 64)
        n=1;
    else
        n=0;
end

V(TX_COMPLETE) <+ transition(!n ? Vhi: Vlo, 0.0, tr, tf);
end
endmodule

```

A.2.5. Verilog-A code for “TX OUTPUT BUFFER [PISO]”

```

module a_TX_PISO_40reg
(vin_d0,vin_d1,vin_d2,vin_d3,vin_d4,vin_d5,vin_d6,vin_d7,vin_d8,vin_d9,vin_d10,vin_
d11,vin_d12,vin_d13,vin_d14,vin_d15,vin_d16,vin_d17,vin_d18,vin_d19,vin_d20,vin_d
21,vin_d22,vin_d23,vin_d24,vin_d25,vin_d26,vin_d27,vin_d28,vin_d29,vin_d30,vin_d3
1,vin_d32,vin_d33,vin_d34,vin_d35,vin_d36,vin_d37,vin_d38,vin_d39,vin_d,vout_d,vcl
k,vload);

electrical
vin_d0,vin_d1,vin_d2,vin_d3,vin_d4,vin_d5,vin_d6,vin_d7,vin_d8,vin_d9,vin_d10,vin_
d11,vin_d12,vin_d13,vin_d14,vin_d15,vin_d16,vin_d17,vin_d18,vin_d19,vin_d20,vin_d
21,vin_d22,vin_d23,vin_d24,vin_d25,vin_d26,vin_d27,vin_d28,vin_d29,vin_d30,vin_d3
1,vin_d32,vin_d33,vin_d34,vin_d35,vin_d36,vin_d37,vin_d38,vin_d39,vin_d,vout_d,vcl
k,vload;

parameter real vlogic_high = 1;
parameter real vlogic_low = 0;
parameter real vtrans = 0.5;
parameter real tdel = 200p from [0:inf);
parameter real trise = 20p from (0:inf);
parameter real tfall = 20p from (0:inf);

integer d[0:39];
integer bit_num;

analog begin

```

```

@ ( cross ( V(vload) - vtrans, -1, 1.0, vload.potential.abstol))
begin
  d[0] = V(vin_d0) > vtrans;
  d[1] = V(vin_d1) > vtrans;
  d[2] = V(vin_d2) > vtrans;
  d[3] = V(vin_d3) > vtrans;
  d[4] = V(vin_d4) > vtrans;
  d[5] = V(vin_d5) > vtrans;
  d[6] = V(vin_d6) > vtrans;
  d[7] = V(vin_d7) > vtrans;
  d[8] = V(vin_d8) > vtrans;
  d[9] = V(vin_d9) > vtrans;
  d[10] = V(vin_d10) > vtrans;
  d[11] = V(vin_d11) > vtrans;
  d[12] = V(vin_d12) > vtrans;
  d[13] = V(vin_d13) > vtrans;
  d[14] = V(vin_d14) > vtrans;
  d[15] = V(vin_d15) > vtrans;
  d[16] = V(vin_d16) > vtrans;
  d[17] = V(vin_d17) > vtrans;
  d[18] = V(vin_d18) > vtrans;
  d[19] = V(vin_d19) > vtrans;
  d[20] = V(vin_d20) > vtrans;
  d[21] = V(vin_d21) > vtrans;
  d[22] = V(vin_d22) > vtrans;
  d[23] = V(vin_d23) > vtrans;
  d[24] = V(vin_d24) > vtrans;
  d[25] = V(vin_d25) > vtrans;
  d[26] = V(vin_d26) > vtrans;
  d[27] = V(vin_d27) > vtrans;
  d[28] = V(vin_d28) > vtrans;
  d[29] = V(vin_d29) > vtrans;
  d[30] = V(vin_d30) > vtrans;
  d[31] = V(vin_d31) > vtrans;
  d[32] = V(vin_d32) > vtrans;
  d[33] = V(vin_d33) > vtrans;
  d[34] = V(vin_d34) > vtrans;
  d[35] = V(vin_d35) > vtrans;
  d[36] = V(vin_d36) > vtrans;
  d[37] = V(vin_d37) > vtrans;
  d[38] = V(vin_d38) > vtrans;
  d[39] = V(vin_d39) > vtrans;

```

```

end

@ (cross( V(vclk) - vtrans, +1, 1.0, vclk.potential.abstol) )
begin
    for (bit_num = 39; bit_num > 0; bit_num = bit_num-1)
        d[bit_num] = d[bit_num-1];
    d[0] = V(vin_d) > vtrans;
end

V(vout_d) <+ transition((d[39] ? vlogic_high : vlogic_low),tdel,trise,tfall);
end
endmodule

```

A.2.6. Verilog-A code for “PWR PISO”

```

module a_TX_PWR_PISO
(vin_d0,vin_d1,vin_d2,vin_d3,vin_d4,vin_d5,vin_d6,vin_d7,vin_d8,vin_d9,vin_d10,vin_
d11,vin_d12,vin_d13,vin_d14,vin_d15,vin_d16,vin_d17,vin_d18,vin_d19,vin_d,vout_d,
vclk,vload);

electrical
vin_d0,vin_d1,vin_d2,vin_d3,vin_d4,vin_d5,vin_d6,vin_d7,vin_d8,vin_d9,vin_d10,vin_
d11,vin_d12,vin_d13,vin_d14,vin_d15,vin_d16,vin_d17,vin_d18,vin_d19,vin_d,vout_d,
vclk,vload;

parameter real vlogic_high = 1;
parameter real vlogic_low = 0;
parameter real vtrans = 0.5;
parameter real tdel = 200p from [0:inf);
parameter real trise = 20p from (0:inf);
parameter real tfall = 20p from (0:inf);

integer d[0:19];
integer bit_num;

analog begin
    @ ( cross ( V(vload) - vtrans, -1, 1.0, vload.potential.abstol))
    begin
        d[0] = V(vin_d0) > vtrans;
        d[1] = V(vin_d1) > vtrans;
        d[2] = V(vin_d2) > vtrans;
        d[3] = V(vin_d3) > vtrans;
    end
end

```

```

    d[4] = V(vin_d4) > vtrans;
    d[5] = V(vin_d5) > vtrans;
    d[6] = V(vin_d6) > vtrans;
    d[7] = V(vin_d7) > vtrans;
    d[8] = V(vin_d8) > vtrans;
    d[9] = V(vin_d9) > vtrans;
    d[10] = V(vin_d10) > vtrans;
    d[11] = V(vin_d11) > vtrans;
    d[12] = V(vin_d12) > vtrans;
    d[13] = V(vin_d13) > vtrans;
    d[14] = V(vin_d14) > vtrans;
    d[15] = V(vin_d15) > vtrans;
    d[16] = V(vin_d16) > vtrans;
    d[17] = V(vin_d17) > vtrans;
    d[18] = V(vin_d18) > vtrans;
    d[19] = V(vin_d19) > vtrans;
end

@ (cross( V(vclk) - vtrans, +1, 1.0, vclk.potential.abstol) )
begin
    for (bit_num = 19; bit_num > 0; bit_num = bit_num-1)
        d[bit_num] = d[bit_num-1];
        d[0] = V(vin_d) > vtrans;
    end

    V(vout_d) <+ transition((d[19] ? vlogic_high : vlogic_low), tdel, trise, tfall);
end
endmodule

```

A.2.7. Verilog-A code for “COUNTER (DIV-45)”

```

module a_divider_45_en(OUT, IN, EN);
input  IN, EN;
output OUT;
electrical IN, EN, OUT;

parameter real Vlo=0, Vhi=1.0;
parameter vth = 0.5;
parameter integer dir=1 from [-1:1] exclude 0;
parameter real tr=20p from (0:inf);
parameter real tf=20p from (0:inf);
parameter real ttol=0.0001p from (0:inf);

```

```

integer count, n, seed, selector;
real dt, ratio;

analog begin
    selector = (V(EN) > vth) ? 1: 0;
    @ (cross(V(EN) - vth, +1.0, 1.0, EN.potential.abstol))
    selector = 1;
    @ (cross(V(EN) - vth, -1.0, 1.0, EN.potential.abstol))
    selector = 0;
    if (selector == 1)
        count=count;
    else
        count=0;
    @(initial_step) seed=-311;

    @(cross(V(IN)-0.5, dir, ttol))
    begin
        if (count == 45)
            count=count;
        else
            count=count+1;

            if (count == 45)
                n=0;
            else if (selector == 0)
                n=0;
            else
                n=1;
        end
        V(OUT) <+ transition(n ? Vhi: Vlo, 0.0, tr, tf);
    end
endmodule

```

A.2.7. Verilog-A code for “COUNTER (DIV-61)”

```

module a_divider_61_en(OUT, IN, EN);
input  IN, EN;
output OUT;
electrical IN, EN, OUT;

parameter real Vlo=0, Vhi=1.0;

```



```

parameter vth = 0.5;
parameter integer dir=1 from [-1:1] exclude 0;
parameter real tr=20p from (0:inf);
parameter real tf=20p from (0:inf);
parameter real ttol=0.0001p from (0:inf);

integer count, n, seed, selector;
real dt,ratio;

analog begin
    selector = (V(EN) > vth) ? 1: 0;
    @ (cross(V(EN) - vth, +1.0, 1.0, EN.potential.abstol))
        selector = 1;
    @ (cross(V(EN) - vth, -1.0, 1.0, EN.potential.abstol))
        selector = 0;
    if (selector == 1)
        count=count;
    else
        count=0;
    @(initial_step) seed=-311;

    @(cross(V(IN)-0.5, dir, ttol))
    begin
        if (count == 61)
            count=count;
        else
            count=count+1;

            if (count == 61)
                n=0;
            else if (selector == 0)
                n=0;
            else
                n=1;
        end
        V(OUT) <+ transition(n ? Vhi: Vlo, 0.0, tr, tf);
    end
endmodule

```

APPENDIX B : IMPLEMENTATION OF BAND PASS FILTER

In Appendix B, we will design a 4th order band pass elliptic and chebyshev II filters.

B.1. Design of 4th Order Band Pass Elliptic Filter

Center Frequency = 912MHz

Pass Band Width = 10MHz

Stop Band Width = 20MHz

Stop Band Attenuation = 100 dB

Pass Band Ripple = 0.001 dB

Figure B.1. Schematic Diagram of 4th Order Band Pass Elliptic Filter.

Table B.1. Component Values for 4th Order Band Pass Elliptic Filter.

Device Name	Optimized Values	Device Name	Optimized Values
L1	354.4 nH	C1	8.93 fF
L2	101.4 pH	C2	300.4 pF
L3	26.99 nH	C3	1.452 pF
L4	20.97 nH	C4	1.129 pF
L5	215.8 pH	C5	141.1 pF
Rin	50 Ω	RL	50 Ω

Simulation Results:

Figure B.2. AC Response of 4th Order Band Pass Elliptic Filter.

Figure B.3. Phase Response of 4th Order Band Pass Elliptic Filter.

Figure B.4. Group Delay response of 4th Order Band Pass Elliptic Filter.

B.2. Design of 4th Order Band Pass Chebyshev II Filter

Design parameters are as follows,

Center Frequency = 912MHz

Pass Band Width = 10MHz

Stop Band Width = 114.6MHz

Stop Band Attenuation = 100 dB

Figure B.5. Schematic of 4th Order Band Pass Chebyshev II Filter.

Table B.2. Component Values for 4th Order Band Pass Chebyshev II Filter.

Device Name	Optimized Values	Device Name	Optimized Values
L1	608.5 nH	C1	50.03 fF
L2	51.9 pH	C2	586.8 pF
L3	14.92 nH	C3	2.342 pF
L4	13 nH	C4	2.041 pF
L5	125.7 pH	C5	242.3 pF
Rin	50 Ω	RL	50 Ω

Simulation Results for 4th Order Band Pass Chebyshev II Filter

Figure B.6. AC Response of 4th Order Band Pass Chebyshev II Filter.

Figure B.7. Phase Response of 4th Order Band Pass Chebyshev II Filter.

Figure B.8. Group Delay of 4th Order Band Pass Chebyshev II Filter.

Table B.3. Summary of Achieved Band Pass Filter Performance.

4 th Order Band Pass	Magnitude	Group Delay	Phase
Elliptic	-6.021 dB	44.2 nSec	-7.7 deg
Chebyshev II	-6.021 dB	83.2 nSec	-4.9 deg

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Thursday, 7 October, 2010, 6:38 PM

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To: girish_jadhav@yahoo.com

Cc: "Daniel Brenk" <brenk@lte.e-technik.uni-erlangen.de>

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"Ultra Low Power Oscillator for UHF RFID", Frequency Control Symposium, 2008 IEEE
International, Page(s) 418 – 421, 2008. Section Number: III. LOCAL OSCILLATOR
Figure Number: Fig. 2. Two variants of current-starved 3-stage ring oscillator (b) with capacitor
Page Number: 419

I don't know if there are any concerns with IEEE.

Greetings

Fatih

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Von: "Daniel Brenk"

Gesendet: 07.10.2010 07:25:41

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Hallo Fatih,

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Viele Grüße,

Daniel

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Von: girish jadhav [mailto:girish_jadhav@yahoo.com]

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Section Number: III. LOCAL OSCILLATOR

Figure Number: Fig. 2. Two variants of current-starved 3-stage ring oscillator (b) with capacitor

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Section Number: 9.2.4 Voltage regulator

Figure Number: Figure 9.4. Schematics of the proposed voltage regulator.

Page Number: 112

Section Number: 9.2.5 Demodulator

Figure Number: Figure 9.7. Amplifier circuit used in the demodulator

Page Number: 116

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