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30 GHz Adaptive Receiver Equalization Design Using 28 nm CMOS Technology

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30 GHZ ADAPTIVE RECEIVER EQUALIZATION DESIGN USING 28 NM CMOS TECHNOLOGY

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ABSTRACT

30 GHZ ADAPTIVE RECEIVER EQUALIZATION DESIGN

USING 28 NM CMOS TECHNOLOGY

by Gustavo T. Villanueva

This thesis consists of a 28 nm submicron circuit design for high speed transceiver circuits used in high-speed wireline communications that operate in the 60 Gb/s range. This thesis is based on research done on high speed equalizer standards for the USB 3.1 SuperSpeed Differential Channel Loss Receiver Equalizer or Peripheral Component Interconnect (PCI) Express® Base Specification Revision 3.0. As of 2015, USB 3.1 and PCI Express® 3.0 are technologies with possibilities to be implemented in emerging technology targeted to consumer applications that demand improvements in signal integrity for high speed serial data communication of baud rates above 20 Gb/s. This thesis proposes a circuit design for an adaptive equalizer capable of adjusting its voltage gain, bandwidth, and boost for high speed data communications. The proposed design is implemented with a novel variable gain amplifier (VGA), a digitally controlled continuous time linear equalizer (CTLE), and a digitally controlled decision feedback equalizer (DFE), which is believed to provide circuit power and signal integrity improvements in the differential receiver and equalization subsystem that operate at 60 Gb/s .

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This thesis is especially dedicated to my mother, Refugio Tostado Alejandre, a smart woman who inspired me with her exemplary knowledge, education, professionalism, and perseverance and who instilled in me the courage to write this thesis. I also dedicate this thesis to my two nephews, Román and Iñaki Villanueva in the

hope that one day they find the desire and inspiration to obtain any type of higher education so that they can also become a beacon of inspiration to others.

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1 Introduction

1.1 Historical Background

Since the advent of high speed serial digital communications, consumers have been able to transfer data from computers to a variety of electronic devices such as printers, fax machines, portable communication devices, and storage devices without the use of bulky cables. To date, the most recognized portable device interface among consumers worldwide is the Universal Serial Bus (USB) device interface. However, there are other types of similar serial communications. Perhaps the most recognized serial communication used between microcircuit devices is the PCI Express®. This thesis uses the fundamental theory used behind two well-known high speed serial communication standards.

Millions of USB consumer interface devices have been designed worldwide to communicate with portable computers, smart phones, portable music or data devices and most recently to communicate with luxury vehicle entertainment systems. In recent years, there has been an increasing demand to build electronic systems that contain microcircuit components that use the USB serial communication standard to transmit data, voice or video signals at an increasing transmission rate. The USB standard is commonly used to transmit information between two open system architectures—between two products used by a consumer. However, a common standard that is intended to enhance data communication between electronic components made by different vendors is the PCI Express® (a.k.a. PCIe®) because it provides high speed communications that are higher than what the USB standard offers. The PCIe®

communication standard allows point-to-point communication between microcircuit chips to minimize timing issues caused by multiple signal wires. Unlike the USB standard that is intended to have a maximum of three meters in length for link connections[1] between two USB devices, the PCIe® is designed to facilitate short length communication between two or more microcircuit devices within a printed circuit board which result in making a physical connection with a much shorter length.

Recently, the technological trend and challenge have been to design circuits that reduce the amount of power, jitter, and design area while increasing the single data signal[2] transmission speeds, data and signal reliability, and bandwidth. However, serial data transmission between USB or PCIe® devices is susceptible to the transmission line loss (hereon referred as "*channel loss*") which directly affects the signal integrity. To compensate for the channel loss, a USB or PCIe® receiver design rely on a receiver front end electronic circuit design called the differential deceiver and equalization subsystem—which is the focus of this thesis.

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[1] In standard network communication theory, a *link connection* is a point-to-point connection between two and independent physical ports. Each port belongs to a communication element in a network system.

[2] The term *single data signal* is also referred to as *serial data* which is information or data that travel in a single transmission line. When testing or probing data information on a single transmission line, data are displayed across a time or frequency domain—each datum becomes a bit or frequency depending on how the data signal is displayed. However, every bit, frequency, datum, or piece of information is stitched and displayed into a single signal which forms the *data signal*. Therefore, many authors, this thesis—and the industry in general—use the term *data* as if it were a singular term—instead of a plural term—because it refers to a singular concept which is the *data signal*—a singular term—traveling in a *single line*. The single term for a piece of information is a *datum*. Therefore, the term "*data"* is correctly applied as a singular term when the context refers to probing electronic data from a single line. A datum is a *bit of data* while *data* is just the voltage or frequency signal in a single metallic line that changes with time.

1.2 Fundamental Transmission Frequency (Nyquist Frequency) and the Unit Interval (UI)

Serial binary data communication between two devices can be accomplished electronically in many ways. The USB and PCIe® standards rely on communicating data using the *non-return-to-*zero (NRZ) line code. In binary serial communication, a data signal is sent through a wire by changing the voltage of the wire with respect to time. When a logical data signal is asserted or is true, the voltage in the wire is driven to the transmitter driver's highest possible voltage—the datum or bit of data is a logical one. Conversely, when the logical data is de-asserted or not true, the voltage in the wire is driven to the transmitter's lowest possible voltage—the datum or bit is a logical zero. As a result, the transmission line requires either a high voltage to represent a logical one or a low voltage to represent a logical zero. When using a differential transmission line (two-wire communication), a change in voltage in the transmission line always indicates a data bit transition and a data bit is always asserted or de-asserted for a predetermined period of time called the unit interval (UI) (Figure 1-1).

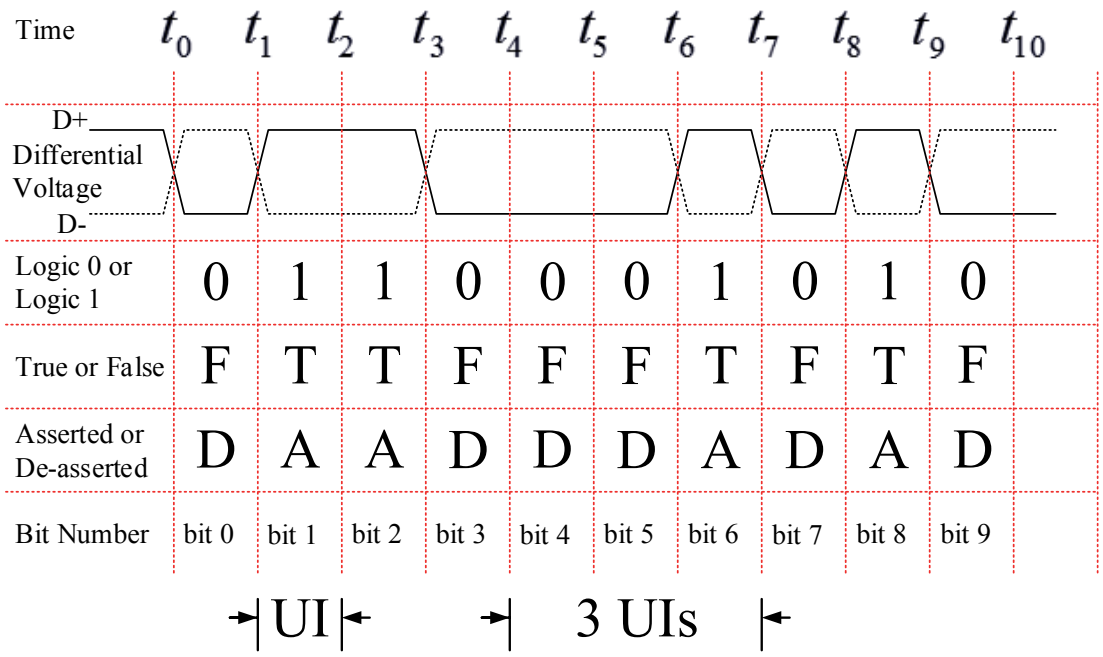


Figure 1-1 NRZ Differential Data Transmission

Baud rate refers to the speed at which logical ones and logical zeroes can be transmitted and detected over the line per a specified UI time interval. Baud rate is also known as the data signaling rate or simply bit rate. In the telecommunication industry, when describing a receiver's bit rate (baud rate), the bit rate is measured using the bit-per-second (b/s) standard.

Let us consider a scenario where four bits are transmitted over a data line in 400 ps. Therefore, each bit would require a time of 100 ps to be transmitted. In this scenario there are 2^4 or 16 combinations of *ones* and *zeroes* of possible combinations that are serially transmitting four bits in 400 ps. In other words, every 400 ps there are four serial bits that are transmitted. The receiver may receive the "0000" combination or a low voltage for a period of 400 ps, or the transmitter may send a combination of "0110"

which in this case it means that for the first 100 ps, the receiver sees a low voltage followed by a transition of a high voltage for 200 ps and ends with a transition of a low voltage for the last 100 ps (Figure 1-2).

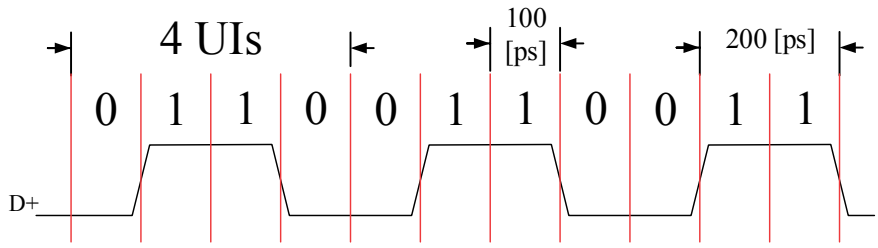


Figure 1-2 Serial Transmission of a 10 Gb/s Signal with Repeating Code "0110"

The unit interval for a 10 Gb/s is calculated by simply dividing one second by the number of bits in that second. Therefore, the unit interval for a 10 Gb/s receiver is 100 ps. The time interval for each bit in this example is 100 ps. The time interval for one bit in the data transmission is also known as the unit interval (UI). For example, in a differential transmission line where each bit is transmitted using NRZ line code at a baud rate of 10 Gb/s, the unit interval (UI) is calculated as follows:

$$UI_{10\frac{Gb}{s}} = \frac{1[b]}{10\left[\frac{Gb}{s}\right]} = \frac{1}{(10)(10^9)}[s] = 0.1 \times 10^{-9}[s] = 0.1[ns] \quad (1\text{-}1)$$

$$= 100[ps]$$

This means that in every 100 ps, the voltage signal could be a *logic one* or a *logic zero*. This also means that the receiver may see a series of logical zeroes ("0000…0000"), a series of logical ones ("1111111…11111"), a combination of zeroes and ones ("0110001110…00011100"), or simply a combination of ones and zeroes ("01010101…01010101") (Figure 1-3).

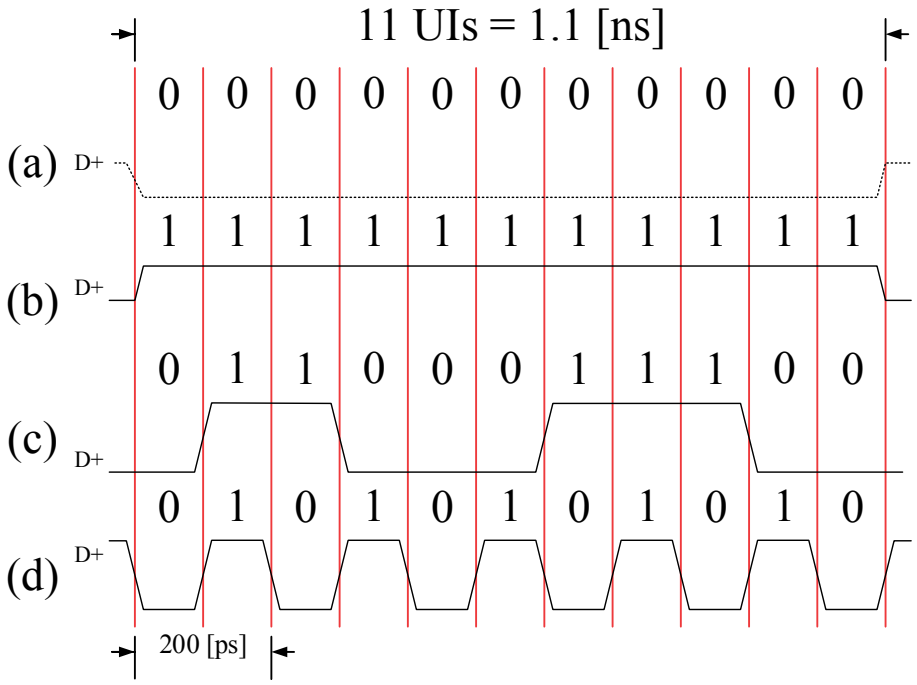


Figure 1-3 Transmission Examples of Serial Data at a Baud Rate of 10 Gb/s. (a) Transmission of *All-zeroes* in 11 UIs, (b) Transmission of *All-ones* in 11 UIs, (c) Transmission of "01100011100" Bit Data, and (d) Transmission of the Nyquist or Fundamental Frequency "010101010101010…)

If the UI for a 10 Gb/s is 100 ps, and the data signal transmitted is a combination of ones and zeroes ("01010101…0101010"), then the cyclic change or time period of the data pattern "01" occurs every 200 ps (Figure 1-3d). This means that the highest data frequency in terms of cyclic voltage change is 5 GHz which is known as the Nyquist frequency or fundamental frequency. In other words, the Nyquist frequency in a NRZ communication circuit is calculated by dividing the baud rate by two but the measure is in Hertz instead of bits-per-second.

Equalizer circuits are designs that take under consideration the Nyquist frequency. For USB 3.0 devices that transmit at a baud rate of 5 Gb/s, the Nyquist frequency is 2.5 GHz. For USB 3.1 devices that transmit at a baud rate of 10 Gb/s, the Nyquist frequency is 5 GHz. For the PCIe® 3.0 devices that transmit at a baud rate of 10 Gb/s, the Nyquist frequency is 5 GHz. This thesis proposes a design that works at a Nyquist frequency of 30 GHz. Therefore, the maximum transmission data rate of this thesis circuit is 60 Gb/s.

An important observation made is that if data is sent over a line with a baud rate of 60 Gb/s, the random data may take a form of any frequency of frequencies below 30 GHz.

1.3 Transmission Reliability, 8b/10b Data Symbols Coding, and Transfers per Second (T/s) Measurement

In PCIe® 3.0 or USB 3.0, for every 8 bits (1 Byte) transferred, an additional 2 bits are added to increase the reliability of the read data. This is done in an effort to increase the reliability of the transmitted data by encoding bytes in the following manner. A combination of 8 serial bits (one serial Byte) is known as a *data symbol*. The total number of combinations of data symbols in one transmitted Byte is 2^8 or 256 symbols. The symbols range from decimal values 0 to 255. However, there are symbols that may look similar to the receiver. For example, symbol “01010101” may be seen by the receiver as “10101010” or symbol “00100101” may be confused by the receiver as “01001010” or “10010010” if the receiver is reading the data signal at the wrong time. In

other words, if a receiver buffers serial data every nibble[3] is received, and if the serial data is a series of nibbles with the bit value of 5b or hexadecimal value of 5h, then by just shifting the data by one UI the receiver will buffer the data with the wrong bit value of 10b or hexadecimal value of Ah (Figure 1-4).

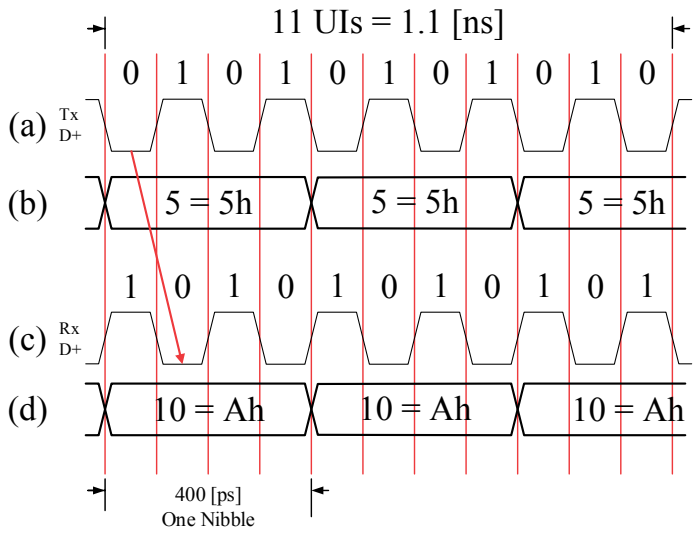


Figure 1-4 Example of Received Data if the Data Signal is Shifted by One UI. (a) Transmitted Data Example; (b) Decimal and Hexadecimal Values of Transmitted Data (a); (c) Example of Received Data Wrongly Shifted by One UI; and (d) Decimal and Hexadecimal Value of Buffered Data (c)

One way to minimize the error in the data received, or to increase the reliability of the data received, is by adding a couple of bits to the serial symbol to create a larger number of combinations which creates a total of 2^{10} or 1024 combinations instead of the

[3] A nibble is four bits or half a Byte. Data with nibble bits [0101b] has a bit value of 5 or a hexadecimal value of Ah. The letter "b" (bit power number) and letter "h"(hexadecimal power number) abbreviates the power number. No letter after the number indicates the number is the decimal power form.

256 valid data combinations. The probability of error is reduced by decreasing the possible valid outcomes from a universe of 1024 combinations.

The PCIe® 3.0 and USB 3.0 (Gen 1) architecture uses the 8b/10b data symbol coding per ANSI X3.230-1994 (also refereed as ANSI INCITS 230-1194) specification (see Table 1-1). As mentioned above, for every Byte of serial information, a couple of bits are added hence creating 1024 possible combinations whereby only 256 combinations are valid. Every Byte valid data combination is given a *data Byte name*. Every bit in the valid Byte is given a letter designation from letter "A" to letter "H." The encoder inserts a bit "L" between the letters "E" and "F" and inserts a bit "J" after the letter "H" to create the 10 bit.

For example, eight bits or one byte is represented by "$b_7b_6b_5b_4b_3b_2b_1b_0$" where b_7 is the most significant bit (MSB) and b_0 is the least significant bit (LSB). Each bit is assigned a capital letter: [$b_7b_6b_5b_4b_3b_2b_1b_0$] = [H G F E D C B A]. If most of the bits are zeroes, then the *Running Disparity* (RD) of the symbol sequence on a per-lane basis is considered negative; else, most of the bits are ones and the RD is positive; otherwise there are an equal amount of ones and zeroes which means that the RD is zero. Data are scrambled every two bytes using the linear feedback shift register (LFSR) algorithm with the 16th degree polynomial $x^{16} + x^5 + x^4 + x^3 + x^0$. This means that bits 0, 3, 4, 5, and 16 are inverted and shifted.

After LFSR is applied, a couple of bits are inserted betweenb_4 and b_5 and after b_7 to form: [$b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$] = [j h g f l e d c b a]—the inserted bits are represented

in red by lower case letters “j” and “l”. Here is an example of several data symbols transmitted using the 8b/10b data symbol coding (see Table 1-1).

Table 1-1 An 8b/10b Data Symbol Coding for Serial Data Transmitted over USB 3.X and PCIe® 3.0. This Table only Shows Eight Data Byte Names out of More than 256 Allowable Coded Symbols

Data Byte Name	Data Byte Value [hex]	Bits HGF EDCBA [binary]	Current RD- abcdeifghj [binary]	Current RD+ abcdei fghj [binary]
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100

The transfers per second (T/s) measure relates to the effective transfer rate of valid bits per second. In the 8b/10b data symbol coding, for every 10 bits transmitted, only 8 bits are valid. Therefore, the effective transmission rate is 8-bits in a time allocated for 10-bits. If the transmitter transmits at a rate of 5 Gb/s, the Transfers per second is calculated as follow:

$$\left(5\left[\frac{Gb}{s}\right]\right)\left(\frac{8\,[T]}{10\,[b]}\right) = 4\left[\frac{GT}{s}\right] \tag{1-2}$$

Perhaps the most important data Byte name in the 8b/10b data symbol coding is “D10.2.” Although its 8-bit input is “01001010b,” the 10-bit output is “0101010101b”

which is the Nyquist frequency. There is no other 8-bit symbol that can create the pattern "0101010101." In the event that the pattern is seen shifted as "1010101010," the receiver will shift the data by one UI and assume that the correct data was symbol "D10.2."

Although the 8b/10b data symbol coding is effective to increase the reliability of the received signal, the system slows down the rate at which useful data is transmitted. In the event that the 8b/10b data symbol coding is used in a 20 Gb/s transmission line, the actual transfer rate is 16 GT/s. Every second, 4 Gb are discarded. This represents 20% of the transmission time is used to pass invalid data.

The 8b/10b coding is normally used for data transfer rates of less than 5 Gb/s. USB 3.1 (Gen 2) uses a 128b/132b line encoding to transmit serial frames at a rate of 10 Gb/s which means that its Nyquist or fundamental frequency is 5 GHz. Each frame contains data and control information. Each frame is made of a 4-bit header and 12-bit payload. The 4-bit header identifies whether the frame is for data ("0011b")4 or control ("1100b"). As frames are received, data is aligned into 128 block; each block is made of 132 bits. Description of the transmission frame is beyond the scope of this thesis. However, it can be said that the effective data transfer to an application after the serial data has been decoded can be as high as 9.6 GT/s.

1.4 USB 3.1 Architecture Impact on Future Electronic Equipment

To understand the impact that USB and PCIe® have over the present electronic technology, a historical background is needed. Beginning with USB architecture, the USB serial interfaces replaced slow speed parallel interfaces used by printers and other

[4] The letter "b" at the end of the bit sequence indicates that this is a binary number.

parallel interfaced devices that connected to desktops or laptop computers. Since 1996, USB version 1.0 technology has allowed consumer electronics devices to become more portable because USB technology replaced the bulky parallel interfaces or ports. The 25 pin printer ports were quickly replaced by 4 pin USB ports. The USB version 1.0 technology only supported data transfer rates (also known as "*baud rates*") from 10 kb/s to 10 Mb/s.[5] As a result, the USB 1.0 technology could only be used by a limited array of consumer devices such as keyboards, game peripherals, e.g. joysticks, and audio devices. In other words, a 4 MB song or picture can be transferred between two USB 1.1 devices in 5.3 seconds but in contrast a 25 GB high definition (HD) movie would take about 9.3 hours to be transferred.

One of the most important attributes of the USB interface technology is its ease-of-use among portable device users because it allows the end user the capability of using plug-and-play devices capable of self-configuring when connecting to a computer. Older technology such as parallel interfaces required a more complex hardware and software implementation. The second most important attribute is its port physical size, cost, and device adaptation. The USB port expansion attribute allowed manufacturers to design and adapt devices that were considered low-speed devices such as a keyboard to use the same port interface of a mid-speed devices for instance a storage devices.

Nevertheless, innovations in technology, for example the invention of submicron technology,[6] enabled the possibility to design faster serial interfaces because such

[5] For purposes of this thesis, all data rates or baud rates are measured in bits per second (b/s). A small letter "b" represents bits while an upper letter "B" represents bytes.
[6] A submicron technology is a technology whereby the smallest transistor length is below 1 μm.

technology can operate with a higher frequency bandwidth. A USB version 3.0 interface allows devices to transfer a 4 MB song or picture in just 10 milliseconds or a 25 GB HD movie in just 70 seconds because under this standard revision the transmission bout rate can reach 5 Gb/s or 4 GT/s. As of 2014, USB version 3.0 gave the possibility to vide stream high definition video between two USB 3.0 devices. As a result, the higher speed serial communication that resulted from the USB 3.0 specification expanded its market opportunity to a variety of consumer devices such as digital cameras and camcorders, flash-based digital media and video players, smart phones, etcetera.

Because consumers are now constantly relying on portable devices such as smart phones, portable storage devices, and other portable devices, consumers have to recharge or power these devices. Under the USB 3.0 standard there is an added functionality to power devices that require power management. Power management is the ability to provide power to a device only when the device requires it, thus conserving energy.

Consumers value the importance of buying electronic devices that have the USB 3.0 interface with hardware applications that include having external mass storage devices used to stream high definition video.[7] As of 2014, the USB standard organization has projected a shipment of more than 4,250,000,000 USB devices worldwide. According to a Global Industry Analysts Inc. (GIA)[8] detailed market report, the USB 3.0

[7] Western Digital, a portable media drive manufacturer, markets a line of USB 3.0 portable hard drives of the size of a travel passport and capable to store up to 150 hours of high definition digital movies in 2TB capacity.

[8] According to MarketResearch.com, "Global Industry Analysts, Inc., (GIA) is a leading publisher of off-the-shelf market research. Founded in 1987, the company currently publishes more than 1300 full-scale research reports and analyzes 40,000+ market and technology trends while monitoring more than 126,000 Companies worldwide. GIA is recognized today as one of the world's largest and reputed market research firms serving over 9500 clients in 27 countries."

market is yet to render its full potential since its technology is predicted a global increase of sales of as many of 3 Billion USB 3.0 enabled devices by 2018 which will result in revenues in the tenths of trillions of dollars [1] Global Industry Analyst, Inc. *USB 3.0 – A Global Strategic Business Report.* March 2013.

The Universal Serial Bus 3.1 Specification was released by the USB Implementers Forum, Inc., on July 26, 2013. The SuperSpeed USB 3.1 delivers baud rates of 10 Gb/s. As of March 2014—when this thesis was written—no published or manufactured microcircuit components that would satisfy this standard were found. This specific standard offers a solution to users to exchange large files between devices in minutes while maintaining power management efficiency.

The USB 3.1 technology is still considered a deployed emerging technology with possibilities of implementation in new USB Flash Drives by 2015, USB Hub devices, on-the-fly Encryption for External USB devices, medical devices, automotive industry, etc. The fact that these implementations have yet to be created by 2014 suggests that there are still challenges in implementing the USB 3.1 that near the 10 Gb/s transfer rates.

1.4.1 USB Technology Transfer Rates

The USB standard is maintained and regulated by the nonprofit corporation called USB Implementers Forum, Inc. (www.usb.org). The corporation was formed by companies that developed the USB standard whose main goal is to promote the benefits of using USB peripherals in high speed serial communication. These companies are Hewlett-Packard (DBA HP), Intel Corporation, LSI Corporation, Microsoft Corporation,

Renesas Electronics, and STMicroelectronics. USB Implementers Forum, Inc., created and supports the following standards:

(a) SuperSpeed+ USB 3.1

(b) SuperSpeed USB 3.0

(c) Wireless USB (WUSB)

(d) On-The-Go Hi-Speed USB

(e) On-The-Go Basic-Speed USB

(f) Hi-Speed USB

(g) Basic-USB

(h) ExpressCard®[9]

USB version 1.0 was released providing two data speeds: 1.5 Mb/s and 12 Mb/s. USB 1.0 was limited to interface with keyboard, printers, and similar interface devices. As personal computers (PCs) became smaller and more portable, users demanded a wider range of interface connectivity which included portable storage media—commonly known as memory sticks or thumb drives. To address this demand, the USB Implementers Forum, Inc. released the USB 2.0 specification in the year 2000 that allowed not only backward-compatibility but also increased the serial transfer rate to 480 Mb/s. Five years later, in 2005, demand for free-of-all-wires wireless technology inspired the release of Wireless USB making the USB peripheral the most used and versatile PC peripheral in the world.

[9] The ExpressCard® standard was created by PCMCIA Association member companies formed by Dell, Hewlett Packard (DBA HP), IBM, Intel, Lexar Media, Microsoft, SCM Microsystems and Texas Instruments (DBA TI) with a collaboration and assistance of the USB Implementers Forum, Inc., and the collaboration of the Peripheral Component Interconnect-Special Interest Group (a.k.a. PCI-SIG).

The year of 2006 became the year where the world was entered the age of smart mobile technology. Products such as smart phones, the iPad, the notebooks, and book readers became an everyday household item. The word "USB" became a popular word and advances in network routing and communication were necessary to provide connectivity service to what was then 2 billion USB devices. USB 2.0 adopted network routing technology similar to what is used in Ethernet network communications to allow USB devices negotiate with one another for the purpose of self-setup and speed up communication in shared USB architectures. The On-the-Go USB communication relies on USB hosts, USB servers, and USB hubs that follow the 4 layer USB transmission protocol rules. By using a USB protocol, the communication capability extended the consumer market of the USB serial port to industrial applications and security systems.

By the year 2011, consumers were hungry for shared content products capable to video stream on demand, or store large amounts of information. High definition photography, HD camcorders, and similar devices required storage spaces that were in the tenths of Giga Bytes. Transmission rates of large amount of data required a faster than the available 480 Mb/s transfer rates. This was resolved by introducing SuperSpeed USB 3.0 to free users from the consuming process of transferring large amounts of information. The transmission rates of a SuperSpeed USB 3.0 connection can provide transfer rates of up to 5 Gb/s.

Currently, the State-of-the-Art communications demand faster transfer data rates for the USB interface. In August 2013, the USB Implementers Forum, Inc. completed the SuperSpeed+ USB 3.1 standard to enable transmission data rates of up to 10 Gb/s.

However, by the first quarter of 2014, the author was not able to find any manufacturer that had implemented a SuperSpeed+ USB 3.1 solution.

It is argued that if a SuperSpeed USB 3.0 architecture design has an adaptive receiver front-end implementation, then it is possible that the receiver may improve the common inter-symbol interference (ISI) created by the transmission line between the transmitter and the receiver.

1.4.2 The SuperSpeed USB 3.0 Standard

The SuperSpeed USB 3.0 standard [2] is compatible to earlier revisions of the USB standard. However, to support higher transmission rates, an additional 5 wires were added to the USB 3.0 transmission line. A USB 2.0 plug has 4 terminals while a USB 3.0 has 9 terminals.

The SuperSpeed (SS) USB 3.0 standard supports data rates of up to 5Gb/s. As of the first quarter of 2014, the SS USB3.0 standard is a deployed technology that has both software and hardware support for consumers. However, the USB Implementers Forum, Inc., recently introduced the new SuperSpeed+ USB 3.1 standard that supports up to 10GB/s transfer rates.

1.4.3 The SuperSpeed+ USB 3.1 Standard

The SuperSpeed+ USB 3. Standard [3] is a backward compatible standard that supports data rates of up to 10 Gb/s and enhanced data encoding efficiency. The standard allows data rated commonly found in Solid State Drives (SSDs) and High Definition (HD) displays. This standard introduces the term “Gen 1,” which is used to reference the receiver front end architecture and data requirements for the USB 3.0 standard to receive

a 5 Gb/s signal. The term "Gen 2" describes the receiver front end design for the SuperSpeed+ USB 3.1 that allows baud rates of 10 Gb/s or effective data rate of as high as 9.6 GT/s. The term "Gen X" refers to either Gen 1 or Gen 2 architectures.

1.4.4 USB 3.0 and USB 3.1 Specification Standard Documentation

This thesis project and proposal were inspired in part by the Universal Serial Bus 3.0 Specification which included errata and Engineering Change Notices (ECNs) through May 1, 2011, Revision 1.0, June 6, 2011 [2]. Detailed specifications for the equalizer design are described by the USB 3.0 SuperSpeed Equalizer Design Guidelines documentation and by the Universal Serial Bus 3.1 Specification provided by the USB Implementers Forum, Inc.

The authors of the USB 3.0 specification include the following companies: Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, NEC Corporation, ST-Ericsson, and Texas Instruments. The authors for the USB 3.1 specification include the following companies: Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, Renesas Corporation, ST-Ericsson, and Texas Instruments.

The USB 3.0 standard augments the basic architectural design of the USB 2.0 standard in functionality and data transmission rate. The USB 3.0 physical connection is backwards and forward compatible. The USB 3.1 equalizer specification is different for Gen 1 and Gen 2. The USB 3.0 and USB 3.1 standard defines a composite cable whereby four of the lines are dedicated to support backwards compatibility to USB 2.0 and an additional five lines are used to provide the extended functionality of the USB 3.0 interface.

1.4.5 USB 3.0 and 3.1 Physical Interface Architecture

The USB 3.0 and USB 3.1 has adopted standard network communication terminology and similar design organization as used in more mature and stable technology such as Ethernet Communication Networks. The USB 3.0 communication is arranged with a *star topology*. This means that *point-to-point* communications between USB *ports* require that one port act as a *host port* while the other port act as a *peripheral device port*.[10] USB *hubs* may be used to drive and route communications between a USB host and a USB peripheral device (Figure 1-5).

[10] The terms "star topology," *"host,"* and *"point-to-point"* are common technical terms used in the network communication industry and definition and description of these terms are outside the scope of this thesis. To have a better technical understanding of these terms, the reader is advised to read recommended training material from the Computing Technology Industry Association (CompTIA) at www.comptia.org. The term *"peripheral device port"* is a term compatible to the term *"user port"* as commonly used between network communication designs that is based on layered protocol architecture.

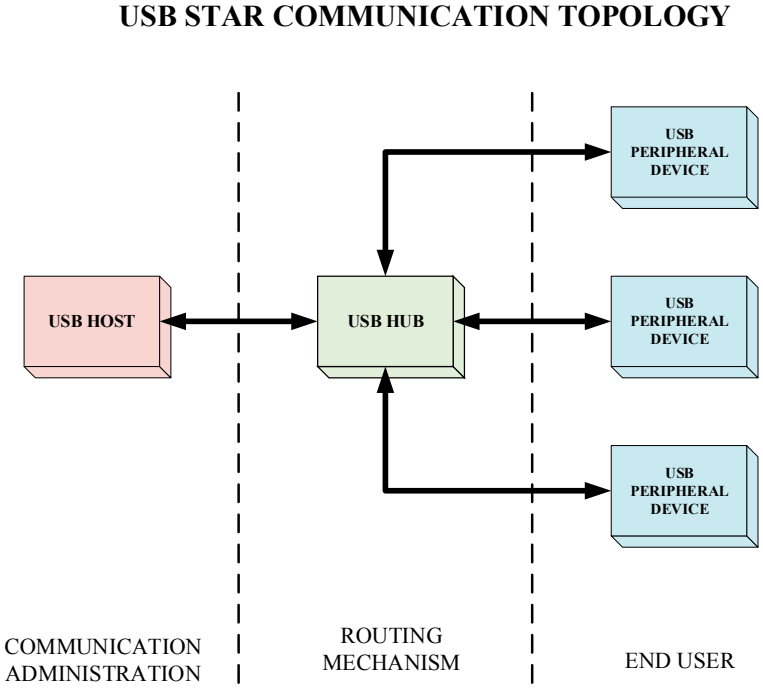


Figure 1-5 Overall Block Diagram for the USB 3.0 Physical Layer Design

1.4.6 Standard Definition of the USB 3.0 Transmission Channel, the Full Link Channel Model

When two electronic devices use a USB wire interface, they must be interconnected directly through USB connectors (hereon referred as a "short channel")—without a cable—or via USB connectors and a differential cable that is no longer than 3 meters long (hereon referred as "long channel"). The front end design must be able to either meet the short channel design specifications or meet both the short and long channel specifications.

A short channel interface consists of the wires from the USB transmitter to the die pads, the connection from the die pad to the mother board—these connections pertain to

the component package—followed by the Printed Circuit Board (PCB) connections to the USB connector, the connector and its mate, the PCB wire connection from the mate connector to the receiver component package, the component package connections to the receiver die pads, and the connection between the die pad to the USB receiver (Figure 1-6).

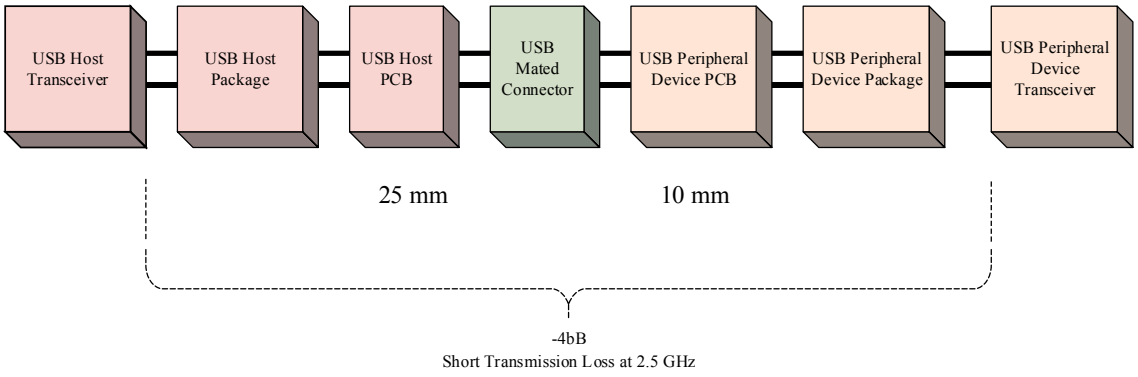


Figure 1-6 USB 3.0 and USB 3.1 Short Channel Application Range

The USB 3.0 standard specifies a maximum attenuation of -4dB between the USB Host Transceiver to the USB Peripheral Device Transceiver at the fundamental transmission frequency of 2.5 GHz.

A detailed representation of the USB transmission for a short channel is defined as *the full link short channel model* (Figure 1-7).

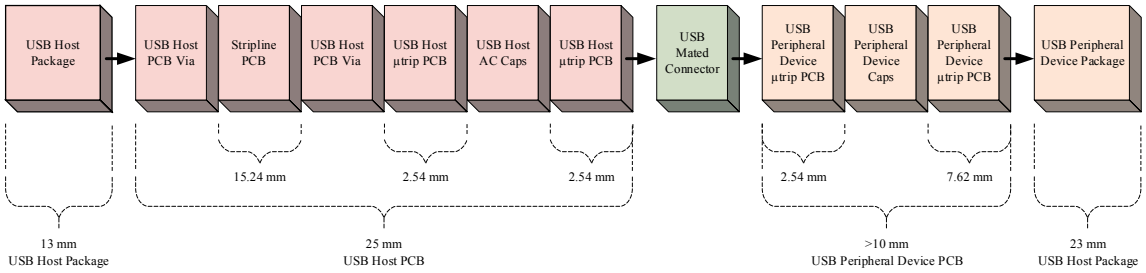


Figure 1-7 Full Link Model for Short Channel Application Range on USB 3.0 and USB 3.1

As mentioned above, a long channel model includes a three meter connector and a device connector the host connector and the device. The long channel full link model PCB striplines[11] are longer than the striplines used in the short channel (Figure 1-8).

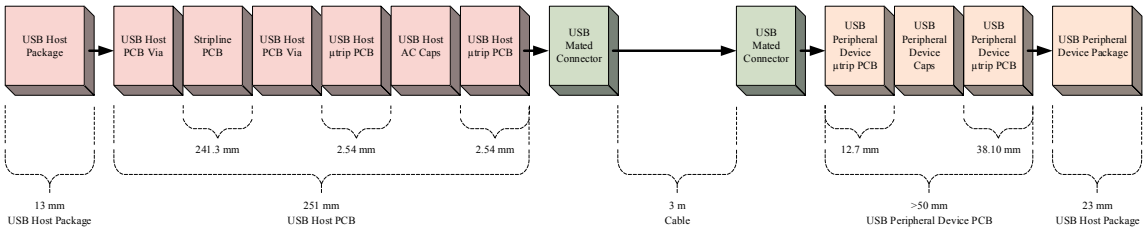


Figure 1-8 Full Link Model for Long Channel Application Range on USB 3.0 and USB 3.1

[11] The term *stripline* refers to a type of transmission line used in PCB designs whereby the transmission line is contained within the PCB substrate and sandwiched between two ground planes to minimize electromagnetic interference (EMI) or white noise.

1.5 2014 State of the Art Circuits in Analog Front-End Design for Gb/s Wireline Receivers

Front-end design refers to the transmitter or receiver end of the microcircuit design. This thesis concentrates on the receiver front-end microcircuit design. According to the International Solid-State Circuits Conference (ISSCC), a group of the Institute of Electrical and Electronics Engineers (IEEE), the highest Nyquist frequency in fast speed communication between devices is 30 GHz [4]. However, stable designs in the industry achieve Nyquist frequencies of no more than 2.5 GHz. For example, the Texas Instruments (TI) DS125BR820 is a low-power 12 Gbps 8-channel liner repeater with equalization, the TI TLK2711-SP is a 1.6 Gbps to 2.5 Gbps Class V Transceiver, the TI DS100BR111A is an ultra-low power 10.3 Gbps 2-channel repeater with input equalization. Fujitsu reported at the annual ISSCC conference to have achieve the world's fastest transceiver of 32 Gbps for inter-processor data communication on February 18, 2013 [5].

1.5.1 Technology Challenges

Signal degradation increases as the transmission rate increases because the channel attenuation increases due to an increase in channel impedance. As a result, equalizer circuits are needed to compensate for the loss in the signal.

Semiconductor technology has limitations as to the highest frequency it can amplify. Equalizers must be able to match the loss of the signal by amplifying its signal. This thesis will describe how to determine the highest frequency for the 28 nm complementary metal-oxide semiconductor (CMOS) technology. Amplifiers have a

limited frequency bandwidth for amplification which is limited by the smallest intrinsic length property of the CMOS transistor.

Power consumption increases as the Nyquist frequency increases. Power dissipation and minimum power limitations may dictate the maximum baud rate.

The loss of the signal is increased as the transmission line length is increased because the overall resistivity of the signal is increased. Signal crosstalk and reflections are minimized by shielding the line and terminating the line with the correct impedance matching respectively. However, for USB technologies, the length of the transmission wire is variable while the impedance matching at the receiver end is fixed.

1.5.2 State of the Art Equalizer Circuits

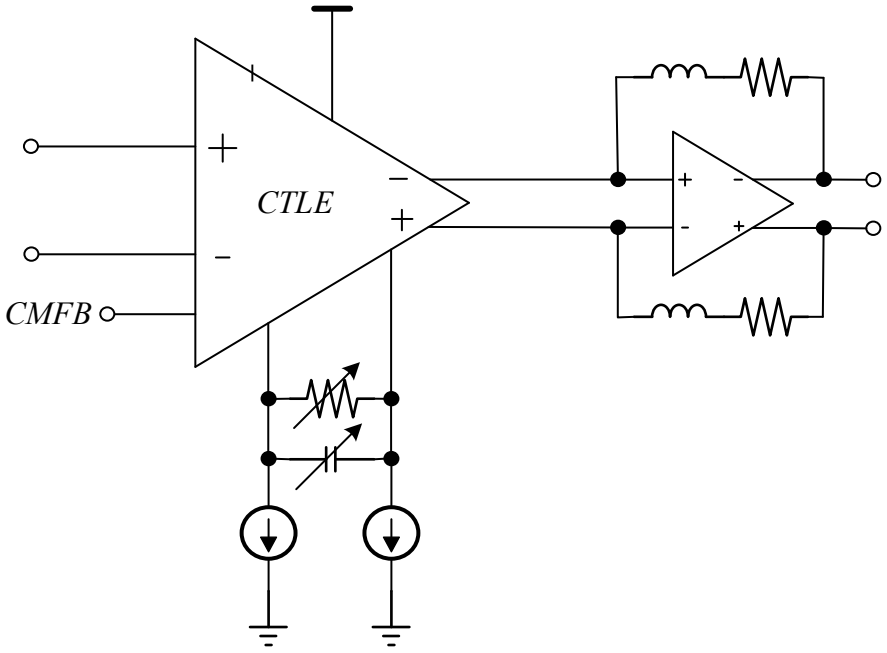
This section illustrates the latest advances in equalizer circuitry. Most of the circuits described here were demonstrated at the 2014 International Solid-State Circuits Conference held every year in San Francisco, California.

1.5.2.1 28 Gbps 560 mW Multistandard Equalizer in 28 nm CMOS

This is a high-speed Continuous Time Linear Equalization-only (CTLE) equalizer [6] that operates at transmission baud rate of 28 Gbps or at a maximum Nyquist frequency of 56 Ghz in a 28 nm CMOS technology.

The analog front end (AFE) design is a comprised of a CTLE and a second stage amplifier with inductive bust. It is not clear from the paper how the resistance and the capacitance is varied in the CTLE circuit bit this type of circuit creates a boost at the Nyquist frequency (Figure 1-9).

Figure 1-10 shows the transimpedance gain[12] of a little bit less than 15 dB for the AFE design at a Nyquist frequency of 10 Ghz. However, it is not clear from the white paper as to what is the effective amplification of a Nyquist signal at 56 GHz.



CMFB: common-mode feedback

Figure 1-9 Analog Front End (AFE) Design of a Receiver CTLE Equalizer. Figure Adapted by Author from **[6]**

It is important to note that this design relies on the fact that 28 nm CMOS technology allows for the amplification of frequencies as high as 60 GHz. This thesis will show how this frequency is measured.

[12] The transimpedance gain is the relationship between the system output voltage with respect to the system input current. This is also known as the Y-parameter.

It is assumed that the insertion loss of the channel is 36 dB at Nyquist frequency of 56 GHz. The insertion loss is typically given as a voltage loss. The equalizer is assumed to amplify the signal loss created by the channel. Ideally, the amplification of the AFE should have been given in terms of voltage amplification terms rather than a transimpedance gain to see if the equalizer is compensating for the loss.

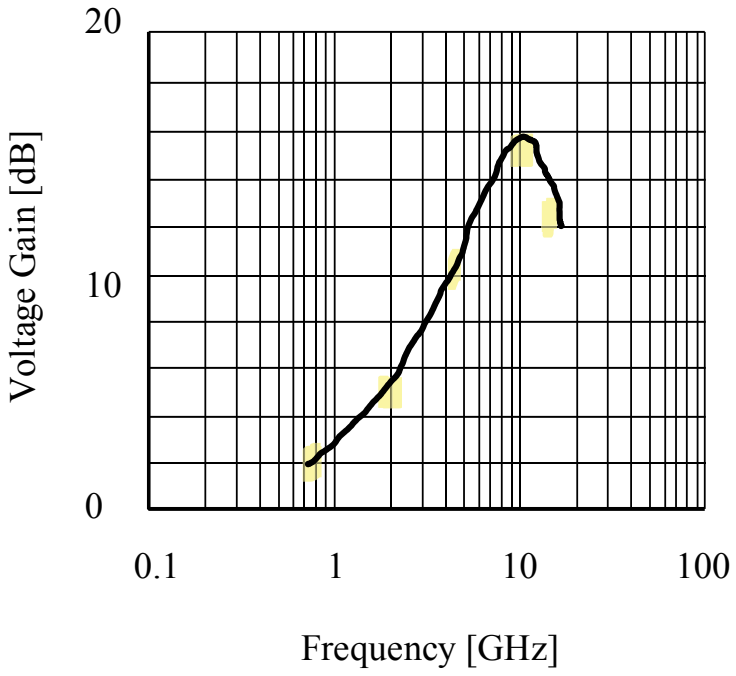


Figure 1-10 Transimpedance Gain. Frequency Response for the AFE. Figure Created by Author from Data in **[6]**

1.5.2.2 25 Gbps 5.8 mW CMOS Equalizer in 45 nm CMOS

This design was made in part by Professor Behzad Razavi, a worldwide well-recognized CMOS design instructor at the University of California. Won Jung and Razavi's approach was to create an AFE design [7] powered by a 1 V power supply. The AFE consists of a CTLE that feeds to a linear de-multiplexer (DMUX) that has sufficient

bandwidth to operate at the Nyquist frequency of 50 GHz. The CTLE equalizer is clamed to boost 8 dB at high frequency though inductive peaking.

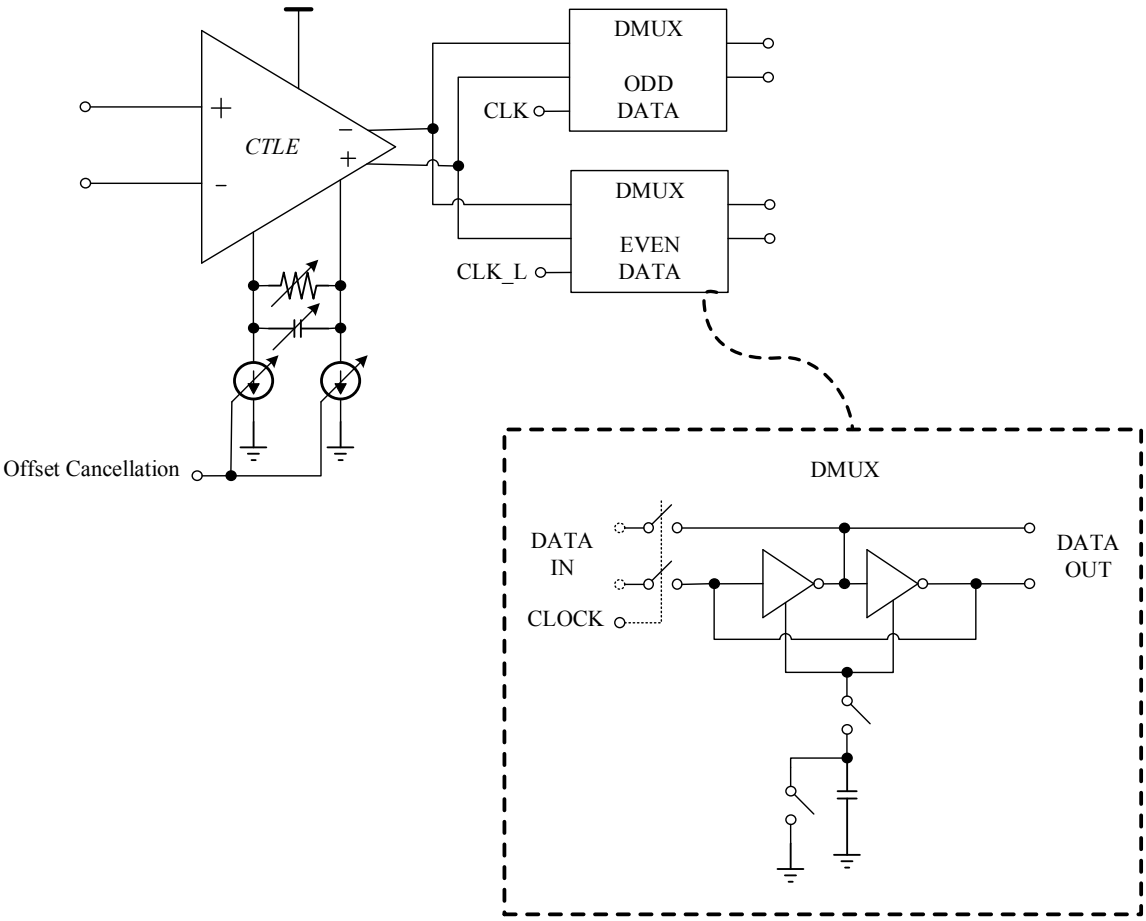


Figure 1-11 Transimpedance Gain. Frequency Response for the AFE. Figure Adapted by Author from [7]

1.5.2.3 16 Gbps 4 mW CMOS Desition Feedback Equalizer in 65 nm CMOS

This circuit claims to "improve the energy efficiency of power-constrained systems" [7] Won Jung and Razavi, *A 25 Gb/s 5.8 mW CMOS Equalizer*. (Reference [4] Session 2.4) [8] by incorporating a low voltage charge-based latch and a charge-based sample-and-hold (S/H) (Figure 1-12). This particular circuit depends on a switching

clock (CK) to sample the transmitted signal UI. The implications are that the clock must be aligned to the input signal. The switching clock must be detected using a clock recovery circuit which is not represented by this system.

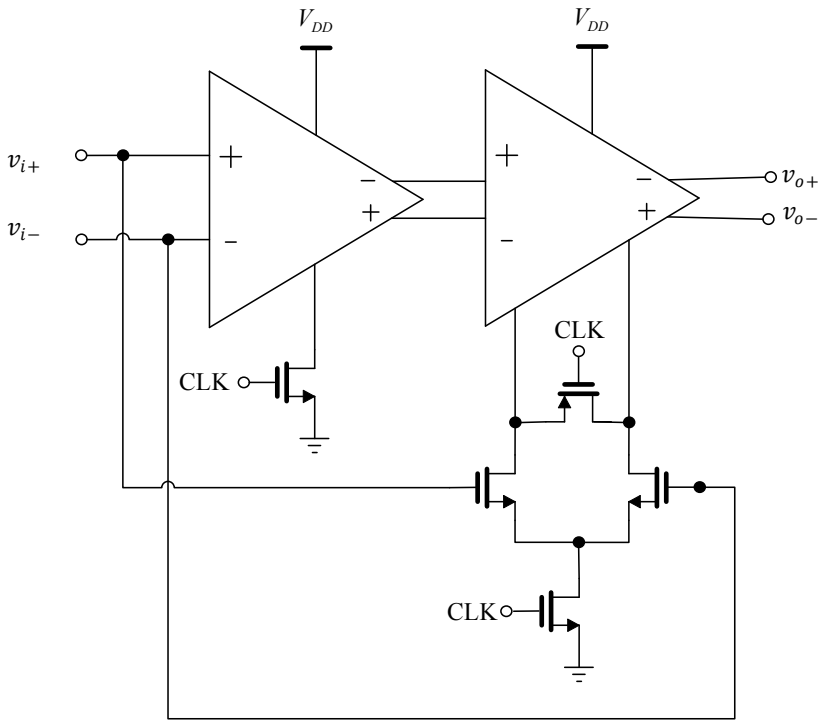


Figure 1-12 Charge-Based Sample-and-Hold (S/H) with Clocked Adaptive Loads. Figure Adapted by Author from [7]

1.5.2.4 25 Gbps 90 mW Power-Scalable with Tunable Active Delay Line Equalizer in 28 nm CMOS

This section describes a cost effective adaptive equalizer circuit design to compensate for the channel loss variations found commonly in multi-mode fiber (MMF) channels. Figure 1-13 illustrates a common source transimpedance amplifier or active circuit with peaking inductors [9]. This circuit is capable to program its bandwidth and

gain dissipation. The CMOS gain (g_m/g_{ds}) for the common source transistors (M_{n1} and M_{n2}) is approximately 5.

Negative resistance is applied to the output by circuits with transistors M_{n3}, M_{n4}, M_{n5}, and M_{n6} to cancel the output inductance. As a result, it allows the circuit to have a 2.5 times trans-resistance result with half times the input noise.

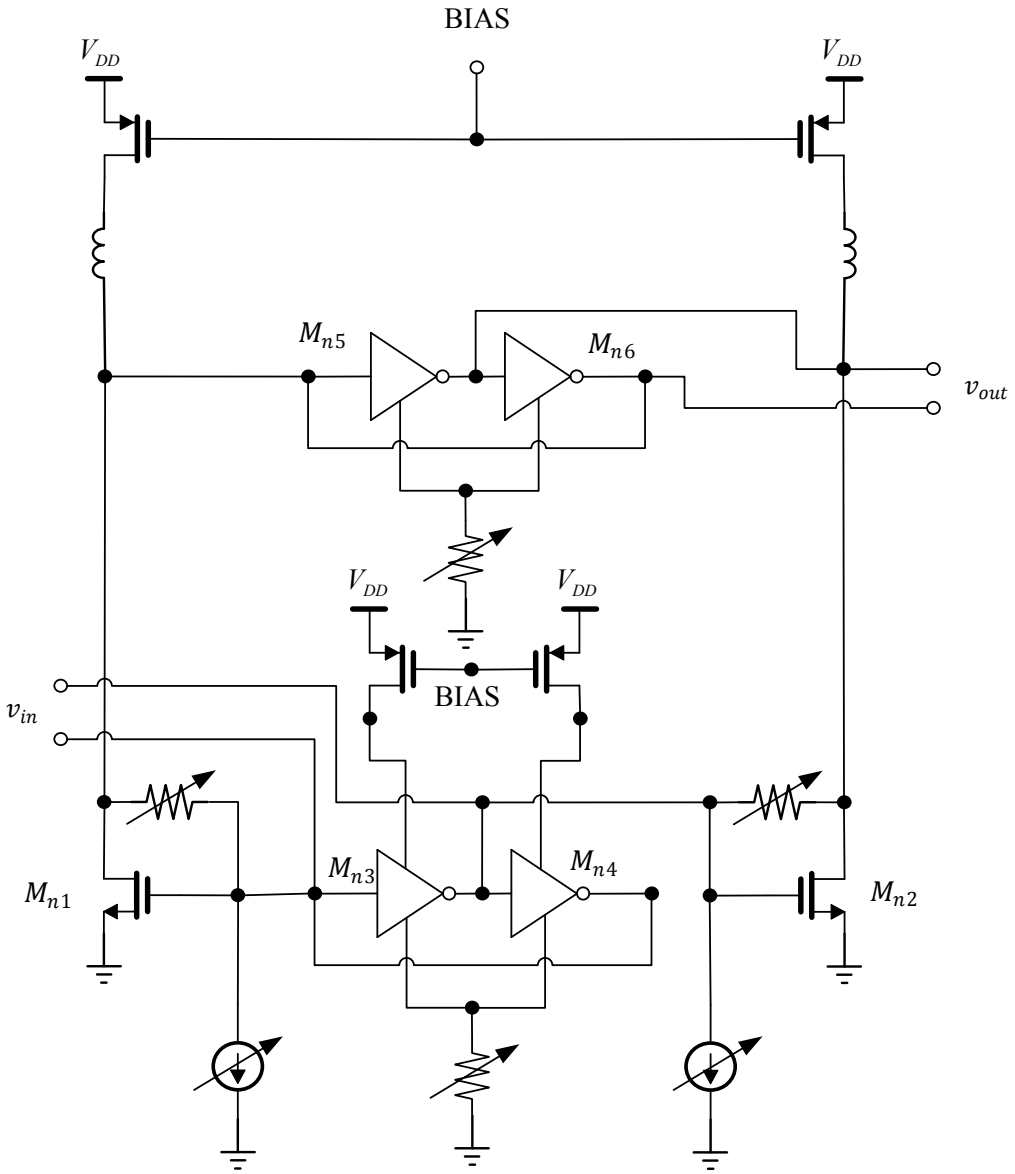


Figure 1-13 Trans-Impedance Equalizer. Figure Adapted by Author from [9]

1.5.2.5 28 Gbps 28.8 mW Trans-Inductance Amplifier (TIA) Equalizer in 28 nm CMOS

A CMOS TIA equalizer circuit [10] allows for high signal gain with a low power supply. However, this circuit is sensitive to supply noise due to its high gain (Figure 1-14). The circuit shows a push-pull TIA with series-peaking inductors (L_{IN}). The source current tail (I_B) makes the transconductance gain (g_m) of transistors M_1, M_2, M_3, and M_4 refer to the bias current as a substitute of the supply voltage which allows for a better noise reduction. Transistor M_7 and M_8 act as a common-source amplifier that provides negative voltage gain through the feedback resistor (R_F). Transistors M_5 and M_6 act as an active variable capacitor and controlled by the feedback voltage (V_F).

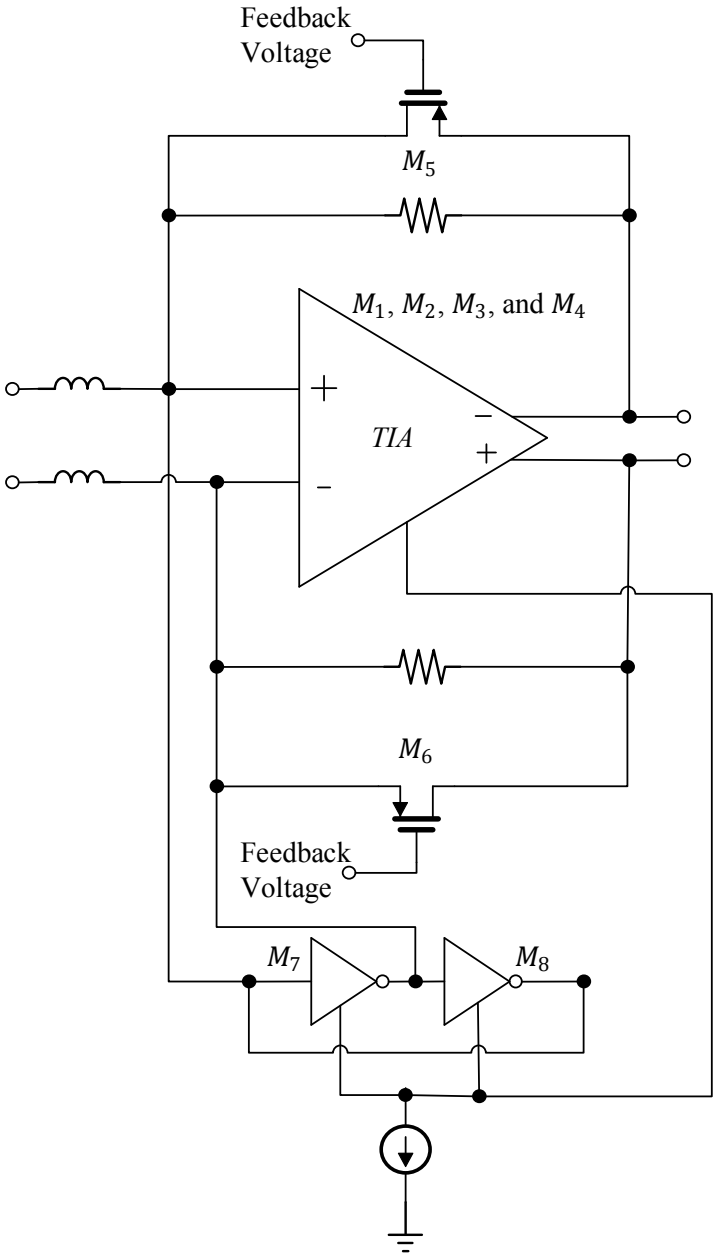


Figure 1-14 Pseudo-Differential CMOS Push-Pull Trans-Impedance Equalizer. Figure Adapted by Author from [10]

1.5.2.6 20 Gbps 0.9 mW Trans-Admittance Stage (TAS) Trans-Inductance (TIA) CTLE in 28 nm CMOS

The TAS-TIA single stage CTLE circuit (Figure 1-15) [11] allows low impedance at the TIA input and output. The circuit gain is approximately the TAS transconductance gain ($g_{m,TAS}$) multiplied by the CTLE resistance feedback (R). The reported gain peaking at 8.5 GHz is 8 dB. The TAS acts as a first stage source-degenerated PMOS circuit that provides the main boosting at Nyquist frequency. The receiver CTLE is programmable by controlling the input voltage to the TIA (V_X). The CTLE boosts high frequency signals to compensate for the channel loss. Low output impedance to the TAS is achieved by an active-shunt load controlled by a CMOS inverter feedback (CMFB).

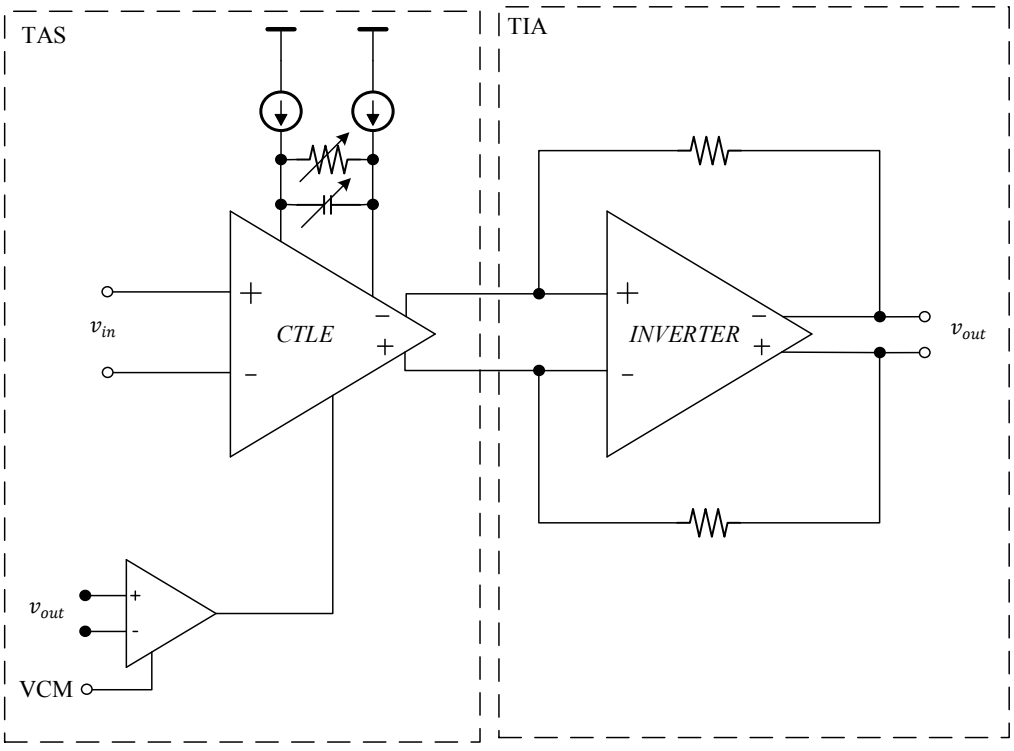


Figure 1-15 TAS-TIA CTLE. Figure Adapted by Author from [11]

2 Channel Model

The communication link between a transmitter and a receiver is called the *transmission line* or *communication channel*. In the case of the USB 3.1 or PCIe® standards, the connection between the transmitter and the receiver is called the *transmission channel* or simply "the channel". The channel is composed of many parts as described in section 1.4.6 herein, but a more simplistic model can be modeled to test the design as proposed in this thesis.

2.1 Types of Printed Transmission Lines

There are six commonly used basic types of printed transmission lines used in the industry and each basic type has respective modifications:

(a) Microstrip lines

    (1) Suspended microstrip line

    (2) Inverted microstrip line

    (3) Shielded microstrip line

(b) Striplines

    (1) Double-conductor stripline

(c) Suspended striplines

    (1) Shielded suspended stripline

    (2) Shielded suspended double-substrate stripline

(d) Slotlines

    (1) Antipodal slotline

    (2) Bilateral finline

(e) Coplanar waveguides

(1) Shielded coplanar waveguide

(f) Finlines

(1) Bilateral slotline

(2) Antipodal finline

(3) Antipodal overlapping finline

Each type of transmission line differs from one another based on their dimensional parameters and electrical properties. For purposes of modeling a transmission line, this thesis will focus on the microstrip lines which have a single transmission line geometry made of a single conductor trace separated from a ground plane by a dielectric substrate (Figure 2-1).

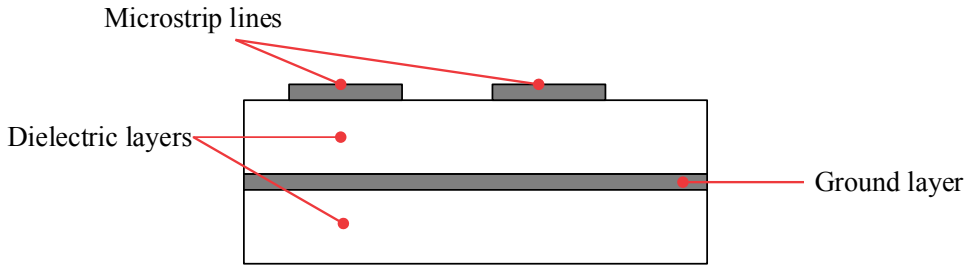


Figure 2-1 Typical Microstrip Line Configuration for Differential Transmission Lines

Assuming the connection between the transmitter and the receiver is a single straight microstrip line with 10 mm length, and the microstrip material is cupper, then it can be assumed that the microstrip line has a resistance associated with the resistivity of the material. The resistivity coefficient of copper is $168 \times 10^{-18} \frac{\Omega}{m}$. Therefore, every millimeter of microstrip line has a resistance of $16.8 \times 10^{-12}\ \Omega$ (Equation **(2-1)**.

$$(1)[mm](168)(10^{-18})\left[\frac{\Omega}{m}\right]\frac{(1)[m]}{(1000)[mm]} = 16.8 \times 10^{-12}\ [\Omega] \tag{2-1}$$

However, the microstrip line has an interelement capacitance between the stripline and the ground plane and an interelement capacitance between the microstrip lines (Figure 2-2). As a result, the interelement capacitance creates a system whereby its impedance is affected by the signal frequency. At low frequencies or d.c. voltage, the interelement capacitance is negligible. However, at data rates where signals approach the 10 GHz or above, the interelement capacitance increases the impedance of the transmission line to such extent that the signal is greatly attenuated.

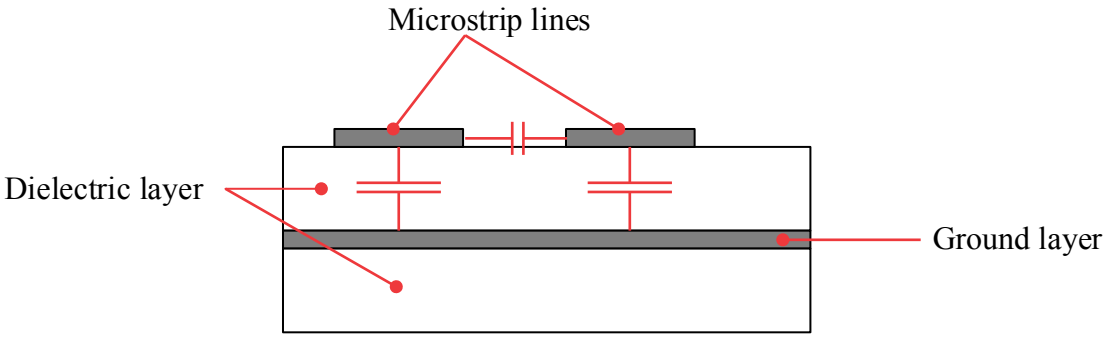


Figure 2-2 Microstrip Lines Interelement Capacitance

The interelement capacitance and resistivity of the microstrip material have an impedance that varies with the voltage frequency of the signal. The capacitance depends on the geometrical factors of the microstrip line and the dielectric permittivity between metals. As a result, creating a precise model for the microstrip line in a computer aided design (CAD) tool is outside the scope of this thesis. However, a simple model can be created by comparing the measured results of microstrip lines.

2.2 The FR4 Microstrip Wire Line

One of the most popular printed circuit board (PCB) microstrip wirelines available is the FR4 dielectric-material wireline. This section describes the transmission line loss as measured in this type of wirelines and the effect that the FR4 wireline has on the transmitted signal due to its inherent design. The FR4 wireline is simply a wire strip that connects two microcircuit devices. On one end, there is a transmitter, while on the other end is the receiver. The FR4 strip line can have different lengths depending on how far are the microcircuit devices. The length of the stripline introduces a higher resistivity in the wireline between the end points due to the FR4 stripline conductivity electrical parameters. As a result, a longer stripline will add loss or higher attenuation on the transmitted signal.

To minimize the effects of signal noise, the transmitter is design to deliver as much power as possible. The receiver on the other hand must be able to amplify the signal that was lost by the transmission channel. However, the loss of the signal is not uniform as the frequency of the signal increases due to the wireline interelement capacitance properties. Figure 2-3 shows how data is connected from one microcircuit device to another via an FR4 microstrip channel.

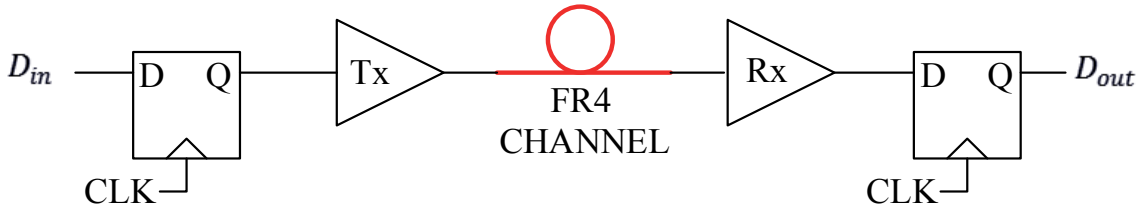


Figure 2-3 FR4 Channel Interconnection

The FR4 channel is not only susceptible to the signal frequency but also to external signal noise from adjacent wires or radio frequency electromagnetic waves from far away. As a result, the signal response at the receiver is deteriorates at such extent that it needs to be equalized to its original magnitude—the magnitude of the transmitter—Figure 2-4.

The transmission line loss profile depends on the trace length and how the connection is made. What this means is whether the transmission line is point to point, or whether the transmission line in a PCB is done using vias or circuit board striplines that are located between dielectric layers (Figure 2-5). Depending on the complexity of a PCB design, transmission lines may be as simple as a point to point connection, or a transmission line may contain multiple vias that may or may not have a via stub component. Therefore, every transmission line transfer function is unique and difficult to model.

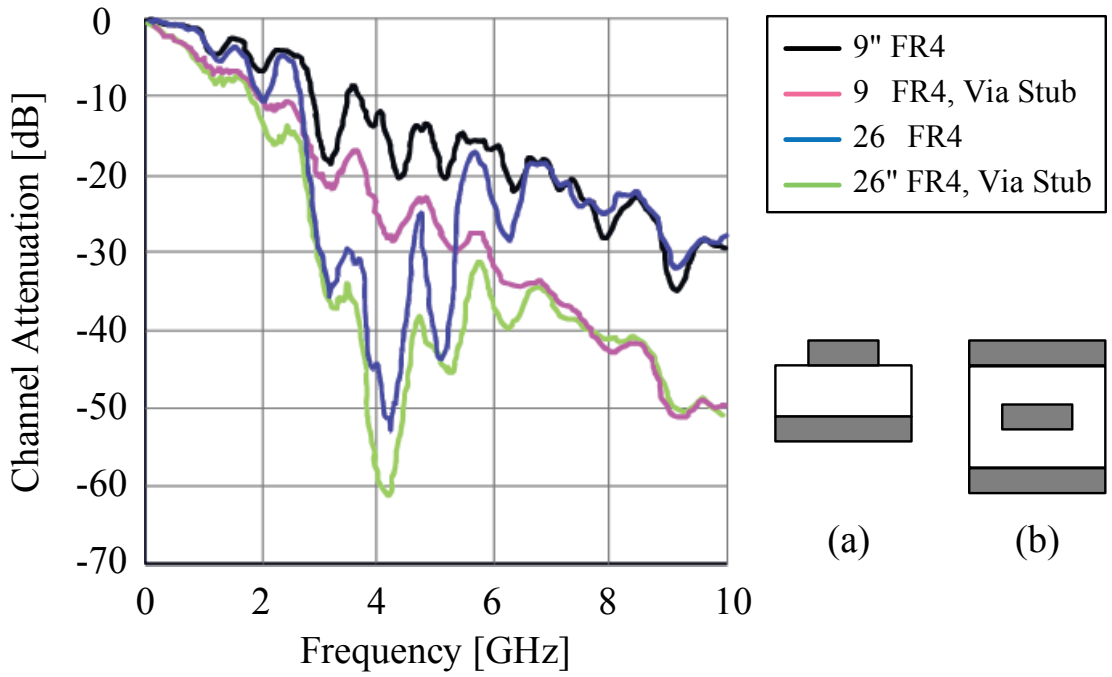


Figure 2-4 FR4 Channel Loss for 9" (22.86 cm-long) and 26" (66.04 cm-long) Wirelines. (a) Cross Section of an FR4 Microstrip Wireline; (b) Cross Section of a Stripline Wireline. Frequency is Displayed in Linear Form[13]

To compensate for the varying channel loss attenuation, the receiver front end designs employ a variety of systems that shape the received signal by controlling the receiver's slew-rate. However, these systems are difficult to design and have limitations as to how much the signal can be shaped. A combination of analog and digital equalization is normally employed on high frequency transmission. For USB transmission lines were changing flexible cable dimensions, the equalizer must be able to check if the received signal is valid. This is called "*signal training*" because the receiver

[13] The source of this graph was obtained from the IEEE, ISSCC tutorial lecture by Instructor Elad Alan. Tutorial held on February 2014 in San Francisco, California. Course title "*Analog Front-End Design for Gb/s Wireline Receivers*." Data adapted by Author.

compares the received signal with a series of known and expected digital values. If the signal does not match, an error signal is generated and used to digitally adjust the receiver front-end equalizer.

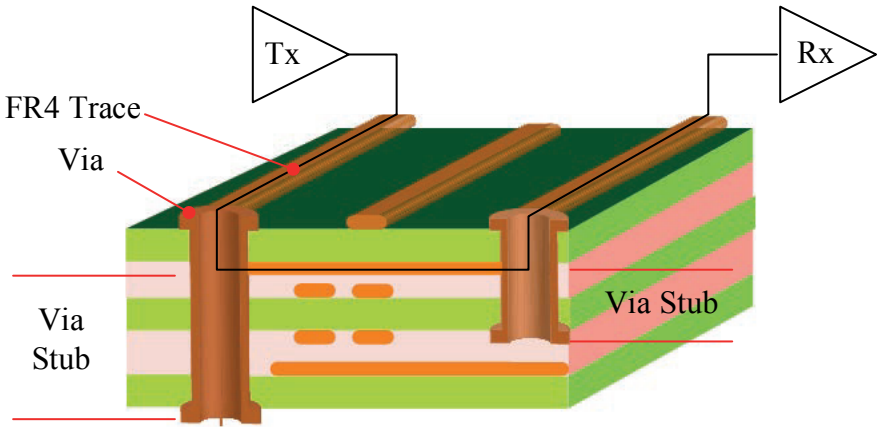


Figure 2-5 PCB Layout of an FR4 Microstrip and Stripline Wirelines Connected Using Vias. Via Stubs Create Additional Interelement Capacitances

Some authors have determined that a 25 cm-long FR4 strip lines is capable to transmit a 100 mV signal with frequencies as high as 100 GHz [12]. This means that it is possible to use FR4 wirelines to reach transmission rates as high as 200 Gb/s. This is significant because the highest proven transmission rate between two devices is no more than 60 Gb/s based on state-of-the-art designs published in 2014.

2.3 Channel Capacity

Channel capacity is defined as the highest possible frequency that can be transmitted reliably [12]. The channel capacity is primarily a function of three system parameters: (a) the channel transfer function ($H(f)$); (b) the spectral power density (SPD) of a source noise ($S_n(f)$); and (c) the SPD of the transmitted signal ($S_{Tx}(f)$).

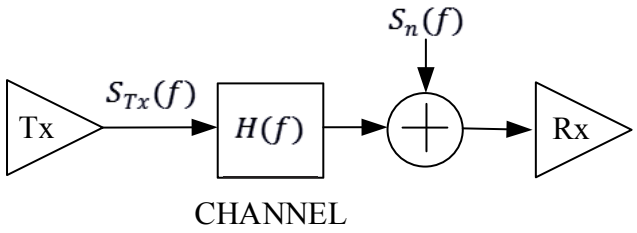


Figure 2-6 Channel Capacity System Model

The average transmit power (P_s) is calculated as follow:

$$P_s = E_{Tx}[{x_{Tx}}^2(t)] = \int_0^\infty S_{Tx}(f)\, df\ [W] \tag{2-2}$$

Considering that for a specific fixed channel with a specific noise source, it can be predicted that there are an infinite number of possible input power spectral densities with a corresponding capacity. The waterpouring method [13] is used to calculate the maximum channel capacity (C) for a given fixed total input power as follow:

$$C = \int_{f \in F_L} log_2 \left[1 + \frac{S_{Tx}(f)|H(f)|^2}{S_n(f)}\right] df\ [bits/s] \tag{2-3}$$

Whereby the frequency band (F_L) depends on the solution of the "L" constant,

$$P_s = \int_{f \in F_L} \left[L - \frac{S_n(f)}{|H(f)|^2}\right] df\ [W] \tag{2-4}$$

$$L \geq \frac{S_n(f)}{|H(f)|^2} \tag{2-5}$$

$$S_{Tx} = \begin{cases} L - \dfrac{S_n(f)}{|H(f)|^2} \; ; \; f \in F_L \\ \\ 0 \; ; \; f \notin F_L \end{cases} \tag{2-6}$$

Note that in order to obtain the channel capacity (*C*), Equation (2-5) must be solved first.

2.4 Modeled FR4 PCB Traces of 1-oz Microstrip Lines

Modeling, calculating, or measuring the channel capacity of a transmission line is important because it gives the circuit designer the ability to know the transmission limits of the system described in Figure 2-6. Figure 2-7 shows that channel capacity is inversely proportional to the length of the channel [12]. Disregarding the effects of external channel noise, a 1-oz microstrip wireline approximately doubles the channel capacity if the length of the wireline is cut by half. Therefore, an ideal design that requires point-to-point communication between two microcircuit devices benefits if the distance between the devices is as short as possible.

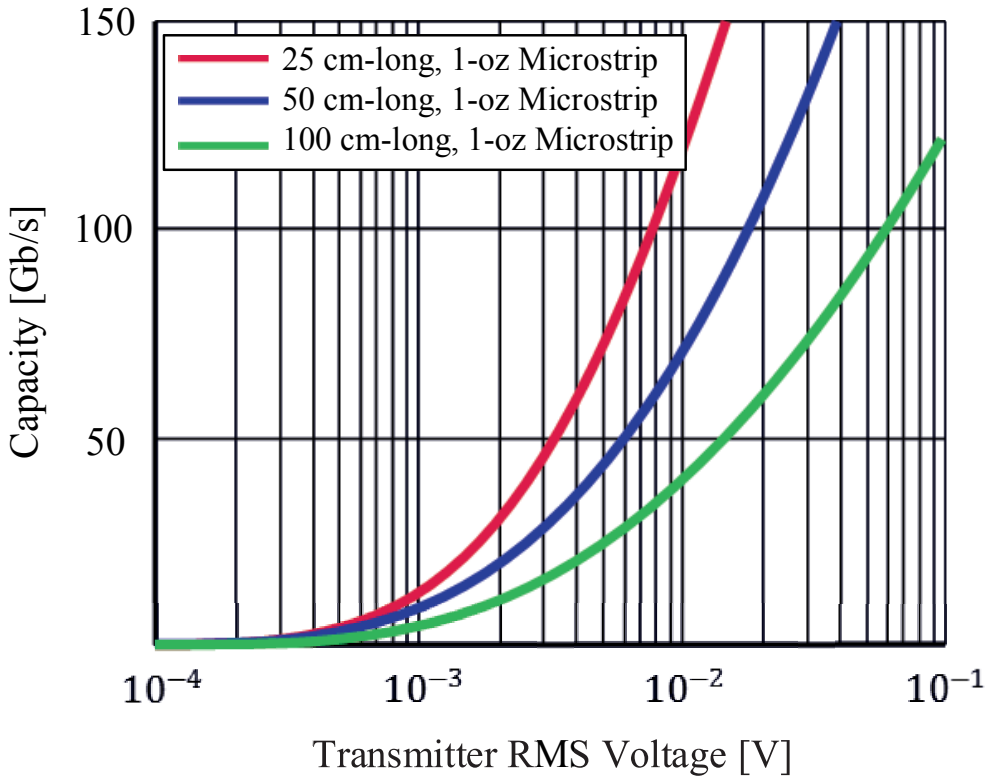


Figure 2-7 Channel Capacity for Various Lengths of 1-oz Microstrip Wirelines with Noiseless Environment. Data Adapted by Author from [12]

However, when noise is inserted into the system, the channel capacity is substantially degraded as shown in Figure 2-8. This demonstrated the importance that needs to be given to the trace layout of a PCB. For high frequency channels, it is critical to make sure that the line is shielded from external ambient electromagnetic noise that may be induced through adjacent signal channels or through unwanted radio frequency (RF) noise.

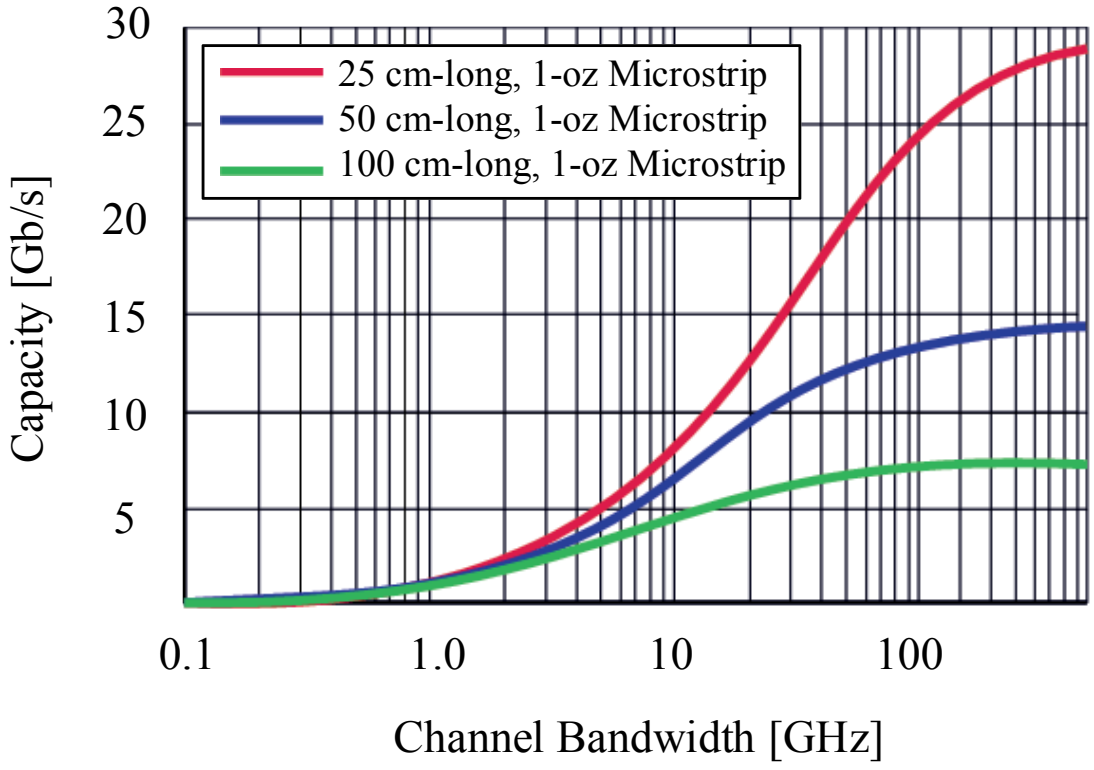


Figure 2-8 Channel Capacity for Various Lengths of 1-oz Microstrip Wirelines with Noise Environment Caused by Signal Crosstalk and Ambient Electromagnetic Noise. Data Adapted by Author from [12]

2.5 Simplified Circuit Model for FR4 Microstrip Channel

Based on the arguments presented in previous sections, it can be argued that is it not possible to predict with absolute certainty as to how the microstrip channel wireline will behaves unless it is measured with instrumentation. However, it is possible to model a simple circuit that would help simulate a channel of a specific length. Some author have measured the frequency response of FR4 channels commonly used in PCB designs.

This section takes under consideration already published measurements and simulations performed on FR4 microstrip channels. Based on mathematical calculations

of the FR4 microstrip line, the channel loss is approximately -25 dB loss for a 100 cm-long, 1-oz microstrip (Figure 2-9). It was also shown that measured 26" (66.04 cm-long) microstrip wireline attenuate signals as much as -50 dB (Figure 2-4). Although there is a difference between what is calculated versus what is measured, the measurement and simulations show that wirelines act as a simple low pass filter. Wirelines also show that attenuation of a signal is predictable with the length of the wire.

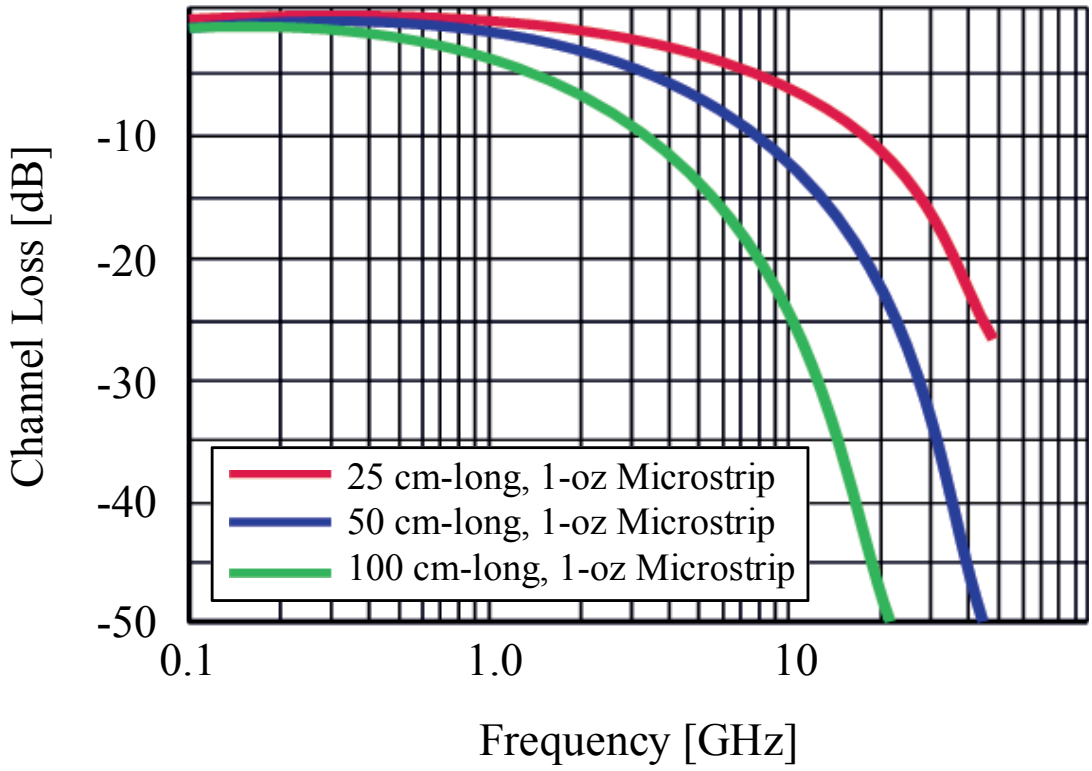


Figure 2-9 Modeled Channel Transfer Function Response ($|H(f)|$) of a 56Ω Impedance Noiseless FR4 Microstrip or Stripline. Data Adapted by Author from [12]

This thesis proposes a simple approach regarding the simulation of a wireline based on Figure 2-4 and Figure 2-9. The proposed circuit makes simple assumptions

such as assuming that a microstrip channel or wireline is made of copper. Copper has a linear resistivity (ρ_{Cu}) at a temperature of 300 K is of 17.1 nΩ-m. Assuming the worst case scenario, a 66.04 cm-long microstrip has a measure loss of -50 dB. Therefore, the resistance of a wire made of copper with this length can be calculated as follow:

$$R_{Cu,66.04\ cm} = \frac{\rho_{Cu}}{66.04\ [cm]} \tag{2-7}$$

$$R_{Cu,66.04\ cm} = \frac{17.1\ [\text{n}\Omega][\text{m}]}{66.04\ [cm]}\frac{100\ [cm]}{[m]} \tag{2-8}$$

$$R_{Cu,66.04\ cm} = 25.89\ [\text{n}\Omega] \tag{2-9}$$

The next step is to assume that the microstrip loss curve can be simulated with a low pass filter (Figure 2-10). The transfer function for the circuit can be found as follow:

$$H(s) = \frac{v_{Rx,in}}{v_{Tx,out}} \tag{2-10}$$

$$= \frac{\frac{1}{sC}}{\frac{1}{sC} + R} \tag{2-11}$$

$$= \frac{1}{1 + sRC} \tag{2-12}$$

$$H(s)|_{s=j\omega} = \frac{1}{1 + j\omega RC} \tag{2-13}$$

$$H(j\omega)|_{\omega=2\pi f} = \frac{1}{1 + j2\pi fRC} \tag{2-14}$$

$$|H(f)| = \frac{1}{\sqrt{1^2 + (2\pi fRC)^2}} \tag{2-15}$$

$$|H(f)|_{dB} = 20\ log_{10}\left(\frac{1}{\sqrt{1+(2\pi fRC)^2}}\right) = -50\ [dB] \tag{2-16}$$

$$-\frac{50}{20} = log_{10}\left(\frac{1}{\sqrt{1 + (2\pi fRC)^2}}\right) \tag{2-17}$$

$$10^{-\frac{5}{2}} = \frac{1}{\sqrt{1 + (2\pi fRC)^2}} \tag{2-18}$$

$$\sqrt{1 + (2\pi fRC)^2} = \frac{1}{10^{-\frac{5}{2}}} \tag{2-19}$$

$$1 + (2\pi fRC)^2 = \left(\frac{1}{10^{-\frac{5}{2}}}\right)^2 \tag{2-20}$$

$$(2\pi fRC)^2 = \frac{1}{10^{-5}} - 1 \tag{2-21}$$

$$2\pi fRC = \pm\sqrt{\frac{1}{10^{-5}} - 1} \tag{2-22}$$

$$C = \left| \frac{\pm\sqrt{\frac{1}{10^{-5}} - 1}}{2\pi fR} \right| \quad ; R = 25.89\ n\Omega \quad ; f = 10\ GHz \tag{2-23}$$

$$C = \left| \frac{\pm\sqrt{\frac{1}{10^{-5}} - 1}}{2\pi(10)(10^{9})(25.89)(10^{-9})} \right| = 194.395\ \text{mF} \tag{2-24}$$

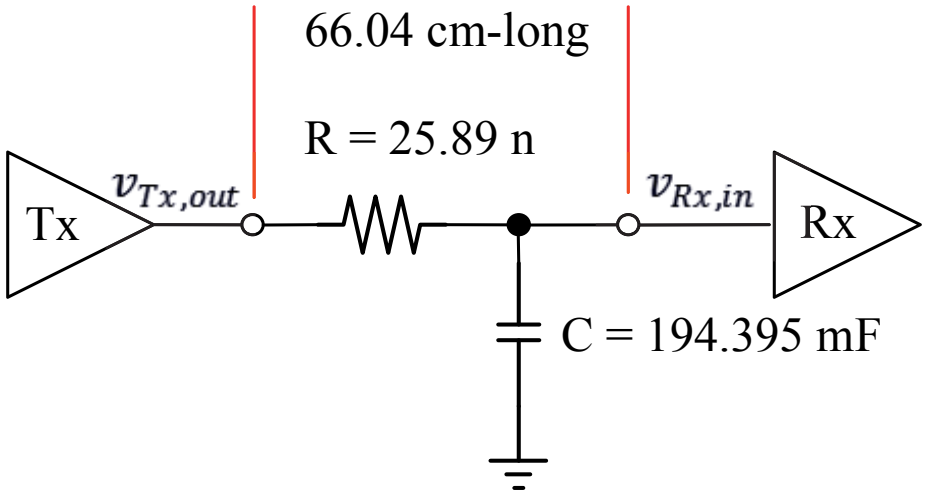


Figure 2-10 Modeled Channel Transfer Function Response ($|\boldsymbol{H(f)}|$) of a 66.04 cm-long Copper Microstrip that has a -50 dB Response at 10 GHz

Assuming that the capacitance of the circuit is uniform across the line, a delta-model or pi-model can be created by dividing the capacitance in half and place the capacitor on each end (Figure 2-11)

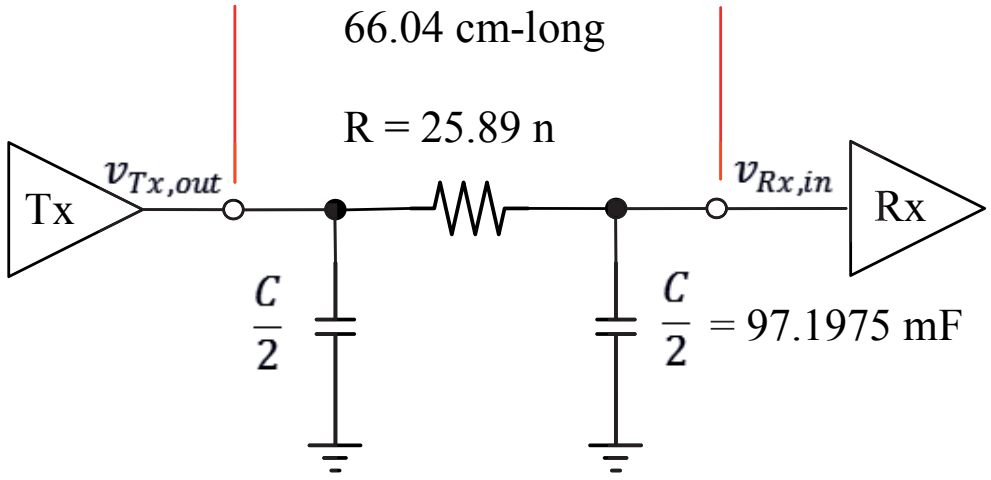


Figure 2-11 Simplified Pi-Model for Channel Transfer Function Response ($|\boldsymbol{H}(\boldsymbol{f})|$) of a 66.04 cm-long Copper Microstrip that Has a -50 dB Response at 10 GHz

In order to model a centimeter of microstrip line, the pi-model is subdivide into equal parts whereby the resistance (R) represents the resistance of one centimeter. The centimeter resistance can be mathematically calculated as follow:

$$\frac{R_{1\ cm,Cu}}{1\ [cm]} \propto \frac{25.89\ [n\Omega]}{66.04\ [cm]} \tag{2-25}$$

$$\therefore R_{1\ cm,Cu} = \frac{25.89\ [n\Omega][cm]}{66.04\ [cm]} = 392.035\ [p\Omega] \tag{2-26}$$

However, to calculate the capacitance of a circuit with n segments become difficult because the total transfer function results in a polynomial of n-segments. For example, if the channel has only two segments, the transfer function becomes:

$$H_{n=2}(f) = \frac{\frac{2}{sC}}{R+\left(R\left\|\frac{1}{sC}\right.\right)+\frac{2}{sC}} \tag{2-27}$$

$$H_{n=2}(f) = \frac{\frac{2}{sC}}{R+\frac{R}{1+sRC}+\frac{2}{sC}} \tag{2-28}$$

$$H_{n=2}(f) = \frac{s2C^3R+2C^2}{C^2R^2+4sCR+2} \tag{2-29}$$

On the other hand, the transfer function for a three segment results in,

$$H_{n=3}(f) = \frac{\frac{2}{sC}}{\frac{1}{sC}\left\|\left(R+\left(R\left\|\frac{1}{sC}\right.\right)\right)+\frac{2}{sC}\right.} \tag{2-30}$$

$$H_{n=3}(f) = \frac{2(s^2C^2R^2+3sCR+1)}{3s^2C^2R^2+8sCR+2} \tag{2-31}$$

Therefore, calculating the value for the capacitor for a large number of segments would result in an arduous mathematical evolution. Instead, the value of the capacitor is derived by using a computer model whereby the capacitance is varied until the -50 dB at 10 GHz curve is obtained. The obtained value for the capacitance for 66 segments was around 680 μF.

Then each pi-model for each centimeter results by dividing each capacitor by half as shown in the example for Figure 2-11. A true channel exhibits a linear decay in gain as frequency is increased—the frequency axis is displayed in linear mode. Note that by adding several segments to the model, the proposed model closer resembles the measured value (Figure 2-13).

To improve the channel, the resistance of each segment should be as low as possible. It was observed that this simple channel model approximates measured results when the resistance for each segment is in the pico-ohm range. However, when comparing the model results in Figure 2-13 to the measured results in Figure 2-4, it can be said that this model is valid for simulation purposes.

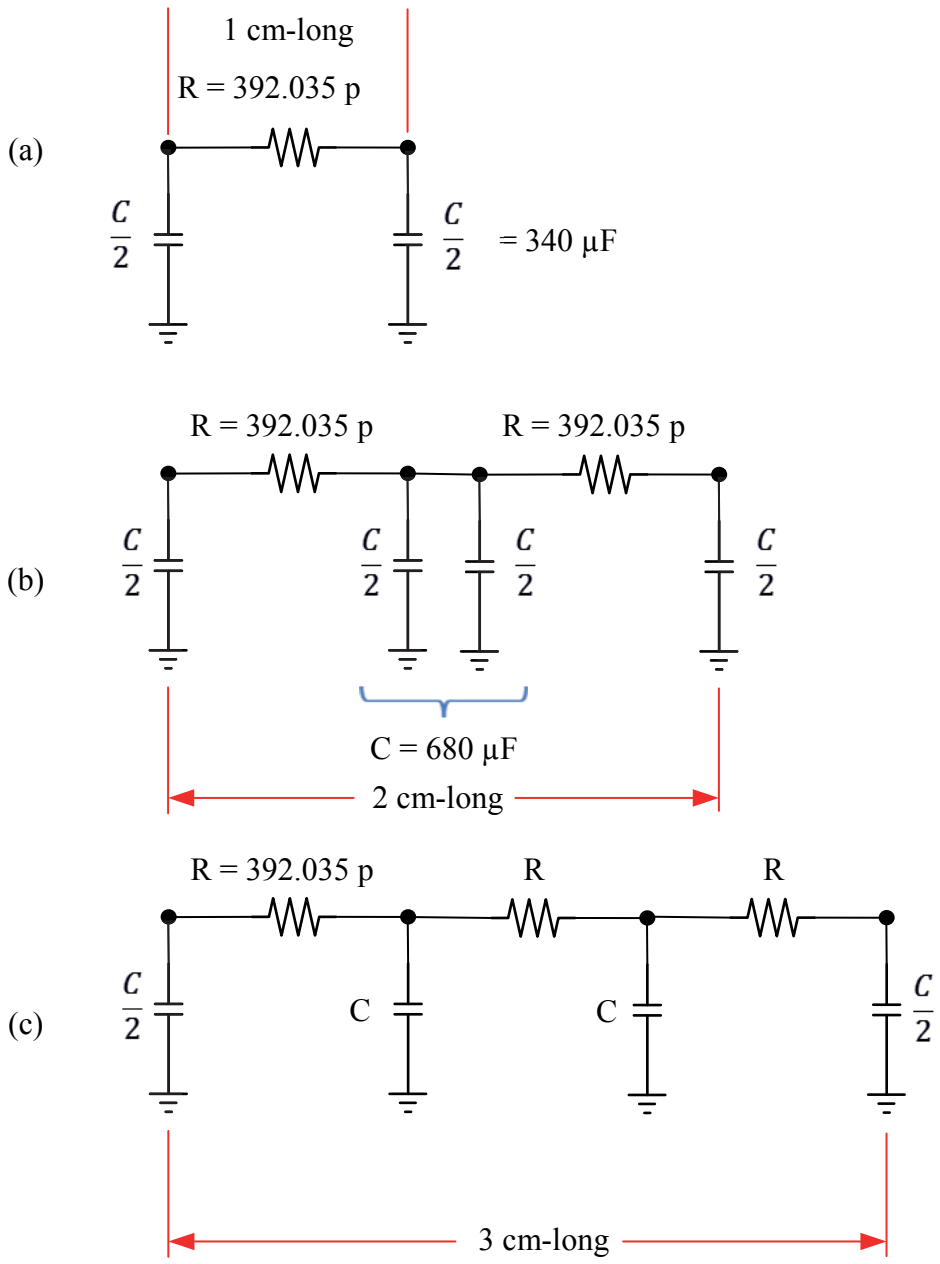


Figure 2-12 Simplified Pi-Model for Channel Transfer Function Response ($|\boldsymbol{H}(\boldsymbol{f})|$) of 1 cm-long Copper Microstrip Segments. (a) Simplified 1 cm-long Channel Segment; (b) Combination of Two Simple Segments to Increase the Length of the Channel; (c) Model of a 3 cm-long Channel Using the Simple Channel Model

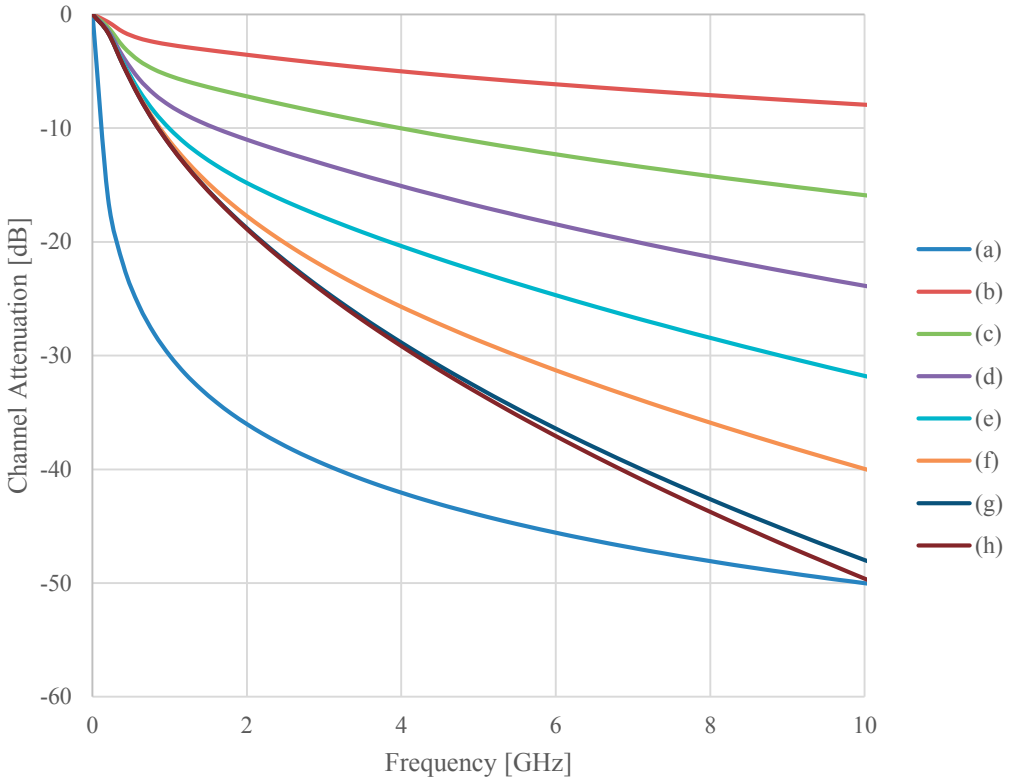


Figure 2-13 Channel Attenuation Results for Proposed Simple Model. (a) Channel Attenuation for One Segment Pi-model; (b) 10 cm-long Channel; (c) 20 cm-long Channel; (d) 30 cm-long Channel; (e) 40 cm-long Channel; (f) 50 cm-long Channel; (g) 60 cm-long Channel; and (h) 66 cm-long Channel

3 Equalizer Design

An equalizer is a device that amplifies the signal loss due to the effects of the transmission channel. Since a channel has a linear loss, an amplifier should also behave an inverse linearity. Designers tend to display the channel loss in a linear way, while displaying the equalizer response in a logarithmic way. Figure 3-1 shows two ways to display the channel loss. Equalizers that are able to regenerate the loss occurred by the channel are commonly called *linear equalizers*.

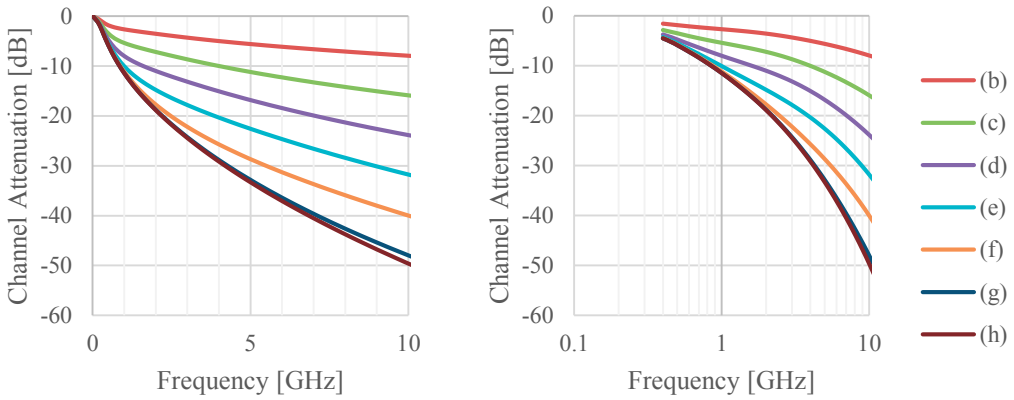


Figure 3-1 Channel Attenuation Results for Proposed Simple Model. The Graph on the Left X-axis Has a Linear Display while the Graph on the Right has a Logarithmic Display. (b) 10 cm-long Channel; (c) 20 cm-long Channel; (d) 30 cm-long Channel; (e) 40 cm-long Channel; (f) 50 cm-long Channel; (g) 60 cm-long Channel; and (h) 66 cm-long Channel

The idea behind a linear equalizer is to regenerate or *boost* the signal that was lost due to the transmission line electrical characteristics. If the channel is assumed to be ideal—meaning that it has no induced noise, signal cross talk, or other interelement capacitances that may disturb the signal—then an equalizer is designed to simply amplify the signal attenuation that was loss by the channel . However, amplifiers are inherently a

low pass filter that have a flat frequency response from low frequencies to the cut-off frequency. The amplifier must be modified in such a way that it would ramp up the gain as frequency increases.

The system model of an ideal equalizer is nothing more that the inverse of the channel transfer function (Figure 3-2).

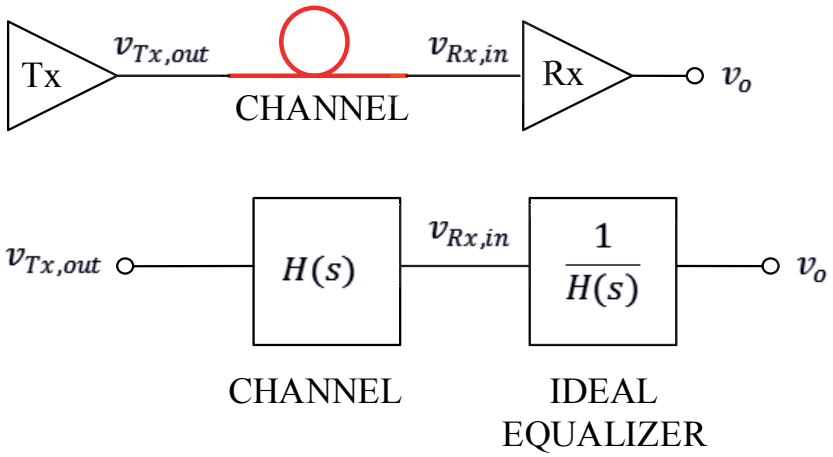


Figure 3-2 System Model for an Ideal Equalizer

An ideal equalizer must be able to inverse the transfer function of the channel to obtain the following results:

$$v_o = v_{Rx,in}\frac{1}{H(s)} = v_{Tx,out}H(s)\frac{1}{H(s)} = v_{Tx,out} \tag{3-1}$$

This can be illustrated graphically as follow:

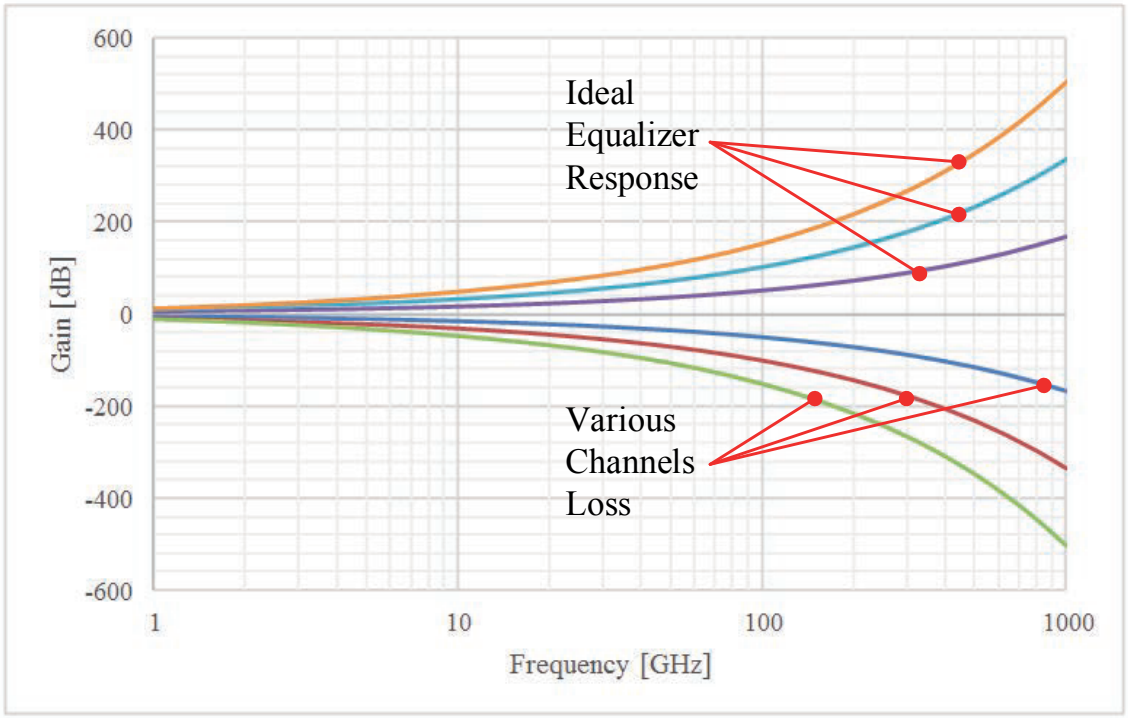


Figure 3-3 Ideal Equalizer Response

Equalizers must be able to adapt its amplification properties if the channel is changed. For example, if a signal is transmitted at 30 GHz, a 20 cm-long channel may attenuate the transmitted signal by -28 dB while a 60 cm-long channel may attenuate the same signal by -83 dB. In other words, the amplifier must be have variable gain.

3.1 Equalizer Bandwidth Limitations

Equalizers have a bandwidth limitation based on its inherent CMOS technology. CMOS transistors behave as a low pass filter when its input is connected to its gate and the output is connected to its drain. For high speed communications, it is imperative to know precisely the limits of the technology used. This thesis is focused on the 28 nm CMOS technology. One way to determine the bandwidth of a NMOS transistor is by

measuring its transit frequency which is defined as the frequency where the transistor is capable to start amplifying. The following sections establish the basis to calculate and know the bandwidth limits of a CMOS transistor.

3.2 Transit Frequency (f_T) and Transit Time (τ_T)

The transit or cut-off frequency of an NMOS transistor helps measure the ultimate intrinsic speed of the transistor without any external limitations and is defined as the frequency which absolute small signal current gain results in unity [14]. The transit frequency delimits the maximum frequency that the MOS transistor functions as a small signal current amplifier. To minimize any external limitations, the transistor must be in saturation mode and the drain of the transistor is short circuited to the supply voltage.

$$\left|\frac{I_d}{I_g}\right|_{f=f_T} = 1 \quad \left[\frac{A}{A}\right] \tag{3-2}$$

There are two popular circuit models that help extract the transit frequency and both models are described herein. This section describes in detail the circuit model test that will be used for the extraction of the transit time and transit frequency [14][15]. However, the mathematical calculations of this circuit model have been purposely modified to employ the new and proposed design method. The second circuit model setup to extract the transit frequency will be described in subsequent sections.

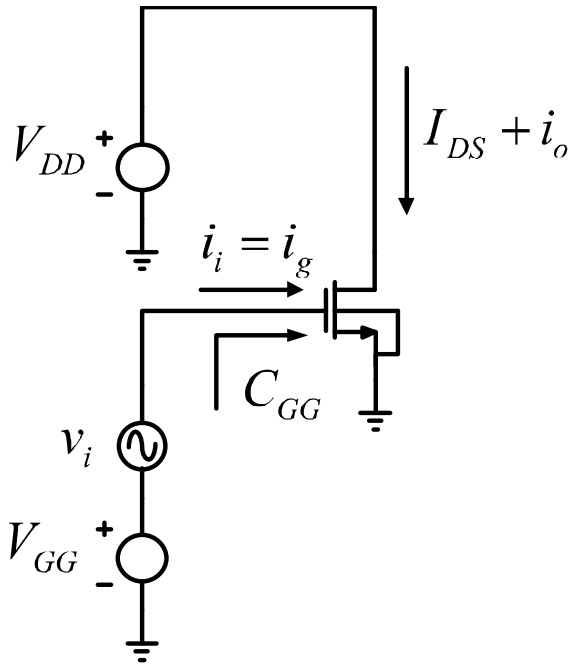


Figure 3-4 Circuit Model Setup to Measure the Transistor's Transit Frequency

The original circuit model requires a small signal input controlled by a sinusoidal current source. The new method changes the sinusoidal current source for a sinusoidal voltage source. This section demonstrates that this change does not affect the results of the model but is critical to the new mathematical model proposed in this paper because the voltage source acts as the desired input voltage of the targeted design.

It can be observed that the current to the gate is only affected by the small signal input while the drain current is a function of the gate voltage bias (V_{GG}), the source voltage (V_{DD}), and the small change in input voltage (v_i).

$$I_{GG} = I_{g,d.c.} + i_g(\omega) \tag{3-3}$$

$$= 0 + i_g(\omega) \tag{3-4}$$

$$= \frac{v_i}{Z_g} \tag{3-5}$$

$$I_{DD} = I_{DS} + i_d(\omega) \tag{3-6}$$

Under this setup, the drain d.c. current (I_{DS}) is the short circuit current—this represents the maximum drain current if a load is considered infinitesimally small or negligible. The small change in d.c. drain current can only be present if there is a small change in the gate voltage. Moreover, the small input current at the gate is present because the input impedance seen at the gate depends in the small input current ($i_g(\omega)$) which is a function of frequency.

Under this setup, the drain d.c. current (I_{DS}) is the short circuit current—this represents the maximum drain current if a load is considered infinitesimally small or negligible. The small change in d.c. drain current can only be present if there is a small change in the gate voltage. Moreover, the small input current at the gate is present because the input impedance seen at the gate depends in the small input current ($i_g(\omega)$) which is a function of frequency.

In the event that the NMOS is used as a common source amplifier, a small current input ($v_i(\omega)$) change causes a small input current ($i_g(\omega)$) change at the gate of the

transistor. Moreover, the small input voltage change results in a change in small drain current ($i_d(\omega)$) which is the output of the circuit test model.

The equivalent input impedance is a function of the gate equivalent capacitance (C_{gg}). As the input frequency increases, the input impedance decreases which results in the small input current to increase.

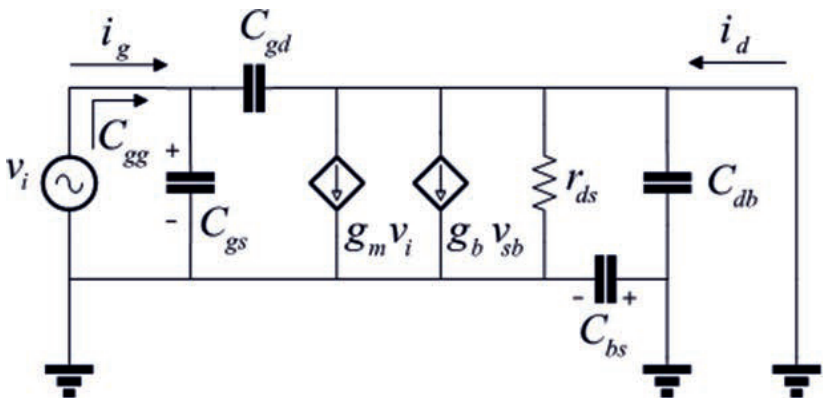
$$i_g = v_i s C_{gg} \tag{3-7}$$

$$= j v_i \omega C_{gg} \tag{3-8}$$

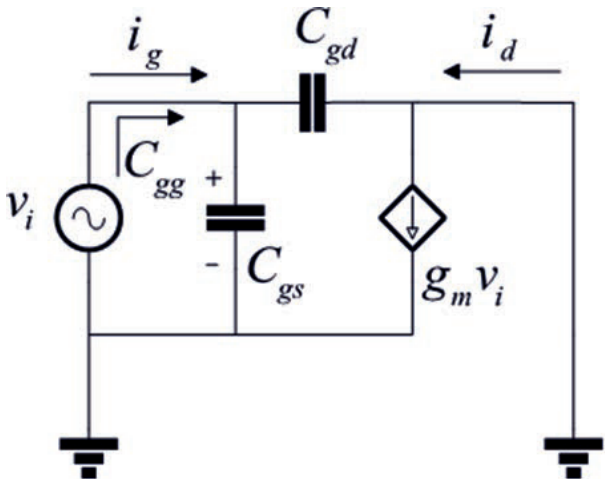
$$= j v_i 2\pi f C_{gg} \tag{3-9}$$

As a result, the small signal output current gain ($|h_{21}|$) decreases when the frequency increases.

$$|h_{21}| = \left|\frac{i_d}{i_g}\right| \tag{3-10}$$



(a)



(b)

Figure 3-5 Small Signal π-Model for Circuit Model to Measure Transit Frequency. (a) All Intrinsic Transistor Components Shown, and (b) Intrinsic Transistor Elements Affected by the Circuit Test Model (Simplified)

$$i_g = v_i s\left(C_{gs} + C_{gd}\right) = v_i s C_{gg} \tag{3-11}$$

$$i_d = v_i\left(g_m - sC_{gd}\right) \tag{3-12}$$

$$|h_{21}| = \left|\frac{i_d}{i_g}\right| = \left|\frac{g_m - sC_{gd}}{s\left(C_{gs} + C_{gd}\right)}\right| \tag{3-13}$$

$$= \left|\frac{g_m}{C_{gs}+C_{gd}} \frac{\left(1+\frac{s}{\frac{g_m}{C_{gd}}}\right)}{s}\right|_{s=j\omega} \tag{3-14}$$

$$= \left|\frac{g_m}{C_{gs}+C_{gd}} \frac{\left(1+j\frac{\omega}{\frac{g_m}{C_{gd}}}\right)}{j\omega}\right|_{\omega=2\pi f} \tag{3-15}$$

$$= \frac{g_m}{C_{gs}+C_{gd}} \left|\frac{\left(1+j\frac{2\pi f}{2\pi\frac{g_m}{C_{gd}}}\right)}{j2\pi f}\right| \tag{3-16}$$

$$= \frac{g_m}{\left(C_{gs} + C_{gd}\right)} \frac{\sqrt{1 + \left(\frac{f}{\frac{g_m}{C_{gd}}}\right)^2}}{2\pi f} \tag{3-17}$$

Equation (3-17) takes the form of the following current gain formula,

$$|h_{21}| = \left|A_o \frac{1 + j\frac{f}{f_0}}{jf}\right| [\frac{A}{A}] \tag{3-18}$$

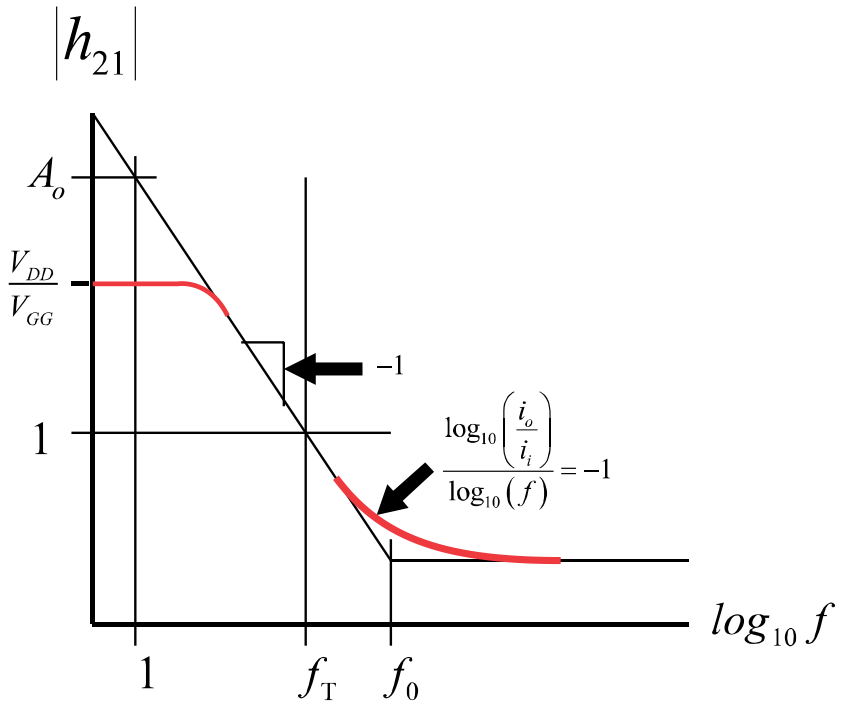


Figure 3-6 Bode Plot for Equation (3-18)

The Bode plot of equation (3-18) as seen in Figure 3-6 shows that the NMOS transistor acts as an amplifier if the current gain ($|h_{21}|$) is more than one. Therefore, the intrinsic amplification only occurs when the frequency is less than the transit frequency (f_T) which is much smaller than the frequency (f_0) at which the transistor small current gain becomes constant. When working with Bode plots, it is important to note that the gain of the frequencies represent the -3dB points of such frequency. For example, the current gain of the transit frequency is not unity but rather $\frac{1}{\sqrt{2}}$. The gain of a frequency that points at a Bode plot with a current gain of 2 is actually $\frac{2}{\sqrt{2}}$. The current gain from equation (3-17) relates to the transistor's intrinsic properties if transistor is setup as shown in Figure 3-4.

$$A_o = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{3-19}$$

$$f_0 = \frac{g_m}{2\pi C_{gd}} \tag{3-20}$$

$$f_{T,-3dB_{(|h_{21}|=1)}} \ll f_o \tag{3-21}$$

At unity gain,

$$|h_{21}| = 1 = \left|\frac{g_m - j2\pi f_T C_{gd}}{j2\pi f_T\left(C_{gs} + C_{gd}\right)}\right| \tag{3-22}$$

$$= \frac{\sqrt{(g_m)^2 + \left(2\pi f_T C_{gd}\right)^2}}{\sqrt{\left(2\pi f_T\left(C_{gs} + C_{gd}\right)\right)^2}} \tag{3-23}$$

$$\left(2\pi f_T\left(C_{gs} + C_{gd}\right)\right)^2 = {g_m}^2 + 4\pi^2 {f_T}^2 {C_{gd}}^2 \tag{3-24}$$

$$4\pi^2 {f_T}^2\left(C_{gs} + C_{gd}\right)^2 - 4\pi^2 {f_T}^2 {C_{gd}}^2 = {g_m}^2 \tag{3-25}$$

$${f_T}^2 4\pi^2\left[\left(C_{gs} + C_{gd}\right)^2 - {C_{gd}}^2\right] = {g_m}^2 \tag{3-26}$$

$$f_T = \frac{g_m}{2\pi\sqrt{\left(C_{gs} + C_{gd}\right)^2 - {C_{gd}}^2}} \tag{3-27}$$

$$f_T = \frac{g_m}{2\pi\sqrt{{C_{gs}}^2 + 2C_{gs}C_{gd}}} \tag{3-28}$$

In this example, it is assumed that the CMOS is in the saturation region and the drain resistance (r_{ds}) is negligible. Therefore, the transconductance gain,

$$g_m = \frac{\partial i_d}{\partial v_i} \tag{3-29}$$

$$= \frac{\partial}{\partial v_i}\left\{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_i - v_{th})^2\right\} \tag{3-30}$$

$$= \mu_n C_{ox}\frac{W}{L}(v_i - v_{th}) \tag{3-31}$$

Where,

μ_n : N-Channel Carrier Mobility (fixed) (3-32)

C_{ox} : Channel Oxide Capacitance (fixed) (3-33)

W : Intrinsic Width (variable) (3-34)

L : Intrinsic Length (variable) (3-35)

v_{th} : Threshold Voltage (variable) (3-36)

That results in the following transit frequency equation proposed in this thesis,

$$f_T = \frac{\mu_n C_{ox} \frac{W}{L}(v_i - v_{th})}{2\pi\sqrt{{C_{gs}}^2 + 2C_{gs}C_{gd}}} \tag{3-37}$$

Moreover, when the transistor is in the saturation region,

$$C_{gs} = \frac{2}{3}WL \gg C_{gd} \tag{3-38}$$

This results in the following approximation for the transit frequency when transistor is in high inversion or saturation region,

$$f_T \cong \frac{3\mu_n C_{ox}(v_i - v_{th})}{4\pi L^2} \tag{3-39}$$

Equation (3-39) suggests that increasing the width (W) of the intrinsic transistor has little effect in the behavior of the transit frequency; an increase in the length (L) of

the intrinsic transistor results in a decrease of the transit frequency which results in a smaller bandwidth. Equation (3-39) also suggests that decreasing the threshold voltage (v_{th}) results in an increase of the transit frequency—the threshold voltage is a negative voltage and should be compared with the small voltage input signal (v_i). If the input signal is much larger than the threshold voltage, the threshold voltage becomes negligible.

Since the intention of this circuit is to find out the possible design limits of the intrinsic transistor, the length of the transistor in a 28 nm technology is set to its minimum intrinsic length to maximize the transit frequency. However, the width of the transistor is set to it most minimum value of 30 nm to maintain the lowest possible power—the intention of this circuit is to find out the intrinsic limitations of a transistor targeted towards specific design specifications. It was assumed that the power of the target circuit should be kept to its minimum. Power is directly proportional to the drain current which is in turn directly proportional to the transistor's intrinsic width.

The Bode plot of the circuit above shows that if the small current gain ($|h_{21}|$) is increased, the intrinsic bandwidth properties of the transistor decrease. It also shows that there is a direct relationship between the gain (A_o) of the transistor at 1Hz, the transit frequency (f_T) at unity gain, and any given frequency (f_o) along the graph with a slope of negative one.

$$A_o = -\frac{A_o - 1}{f_T - 1}(1) + k \qquad A_o = -\frac{A_o - 1}{f_T - 1}(1) + k \tag{3-40}$$

$$1 = -\frac{A_o - 1}{f_T - 1}(f_T) + k \tag{3-41}$$

$$\therefore k = \frac{A_o f_T - 1}{f_T - 1} \tag{3-42}$$

$$|h_{21}| = -\frac{A_o - 1}{f_T - 1} f + \frac{A_o f_T - 1}{f_T - 1} \tag{3-43}$$

$$= \frac{A_o f_T - A_o f + f - 1}{f_T - 1} \tag{3-44}$$

$$f_{T,-3dB} \gg f \gg 1 \; and \; A_0 \gg 1 \tag{3-45}$$

$$\Rightarrow |h_{21}| \cong A_o \left(1 - \frac{f}{f_T}\right) + \frac{f}{f_T} \tag{3-46}$$

$$\cong \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}\left(1 - \frac{f}{f_T}\right) + \frac{f}{f_T} \tag{3-47}$$

$$i_i \propto v_i \; and \; i_o \propto v_o \tag{3-48}$$

$$\Rightarrow |h_{21}| = \left|\frac{i_o}{i_i}\right| = \left|\frac{v_o}{v_i}\right| \tag{3-49}$$

In the event that a bandwidth is desired with a cutoff frequency which experience no attenuation, equation (3-46) can be modified as follow:

$$\frac{A_o}{\sqrt{2}} \cong A_o\left(1-\frac{f_{0dB}}{f_G}\right)+\frac{f_{0dB}}{f_G} \tag{3-50}$$

$$\frac{A_o}{\sqrt{2}} - A_o\left(1-\frac{f_{0dB}}{f_G}\right) \cong \frac{f_{0dB}}{f_G} \tag{3-51}$$

$$A_o\left(\frac{1}{\sqrt{2}} - \left(1-\frac{f_{0dB}}{f_G}\right)\right) \cong \frac{f_{0dB}}{f_G} \tag{3-52}$$

$$A_o\left(\frac{f_{0dB}}{f_G} + \frac{\sqrt{2}}{2} - 1\right) \cong \frac{f_{0dB}}{f_G} \tag{3-53}$$

$$A_o \cong \frac{2f_{0dB}}{2f_{0dB} + f_G\left(\sqrt{2}-2\right)} \tag{3-54}$$

$$f_G \cong \frac{f_{0dB}(A_o-1)\left(\sqrt{2}+2\right)}{A_o} \tag{3-55}$$

The method proposed in this thesis is intended to find the frequency (f_G) for a desired low frequency gain (A_o) and a bandwidth that experiences no attenuation at that gain (f_{0dB}). For example, this thesis will show the that the bandwidth of an amplifier using the 28 nm CMOS technology can be set higher than 30 GHz with a voltage gain that would be able to boost high frequency signals. An IC designer can use Equation

(3-55) to find the needed cutoff frequency of an amplifier while maintaining a voltage gain higher than 1 V/V. It will be shown in the proceeding sections the results obtained using the 28 nm CMOS technology using the Cadence Design Systems (CDS) simulation tools.

The minimum intrinsic transit time (τ_T) of the transistor measures the maximum intrinsic speed of the transistor which is the inverse of the transit frequency. In this example, it was observed that the transistor operates faster in the amplification region if the length of the transistor is kept as short as possible. However, this creates an increase in the drain current and therefore an increase in the power consumption of the circuit.

$$\tau_T = \frac{1}{f_T} \cong \frac{4\pi L^2}{3\mu_n C_{ox}(v_i - v_{th})} \tag{3-56}$$

Since the width of the transistor has little effect in changing the speed of the transistor or adjust the transit frequency, this parameter should be used to adjust the drain current which affects the transconductance gain (g_m) of the transistor.

It is important to point out that the transit frequency is a function of the small input current which in turn is a function of frequency. The small input current (i_i) that depends on the input voltage (v_i) must have a magnitude which is dependent not on the transistor's intrinsic properties, but rather in the specifications set by the designer. A small input current of zero magnitude has no meaning because it would result in no change in drain current which will result in the analysis of a transit frequency that would also have no meaning.

The small current input is directly proportional to the small input voltage ($i_i \propto v_i$). Therefore, to test the limitations of a targeted design, the requirements of the input voltage will make an affect in the transit frequency of the transistor because the limiting gate voltage bias is defined by Equation (3-57). This d.c. voltage is commonly referred as the common mode (CM) gate voltage.

$$\mathrm{V_{GG,max}} = \mathrm{V_{dd}} - \frac{v_i}{2} \tag{3-57}$$

Reducing the gate voltage bias (V_{GG}) results in reducing the transit frequency. Figure 5 shows a family of curves that demonstrates how a change in the gate voltage bias results in a shift of transit frequency. The transistor size is unchanged as well as the magnitude of the input voltage which is a design dependent variable.

As mentioned above, the transit frequency of a CMOS device is dependent on the device dimensional parameters such as the transistor's length and the common mode voltage if the transistor acts as an amplifier and such amplifier is connected as a common source amplifier. The most ideal situation is when the transistor is set up to have its most minimum value. For the 28 nm CMOS technology, the smallest intrinsic length is not 28 nm but rather 30 nm while the smallest intrinsic transistor's width is 80 nm.

Figure 3-7 shows the profiles for different current gains. Note that the current gain response depends on how the gate voltage is set. Note that the current gain is not necessarily directly proportional to the increase of the drain current. Note that at low frequencies, the highest current gain possible is when the device's common mode voltage (gate voltage) is around 0.7 V d.c. However, this observation I not the same at high

frequencies. The drain current measured at 30 GHz is 74.48 µA while the current gain is 6.99 A/A for a gate voltage of 0.7 V. On the other hand, the drain current measured at 30 Ghz is 110.48 µA while the current gain is 9.69 A/A for a gate voltage of 0.9 V (Figure 3-8).

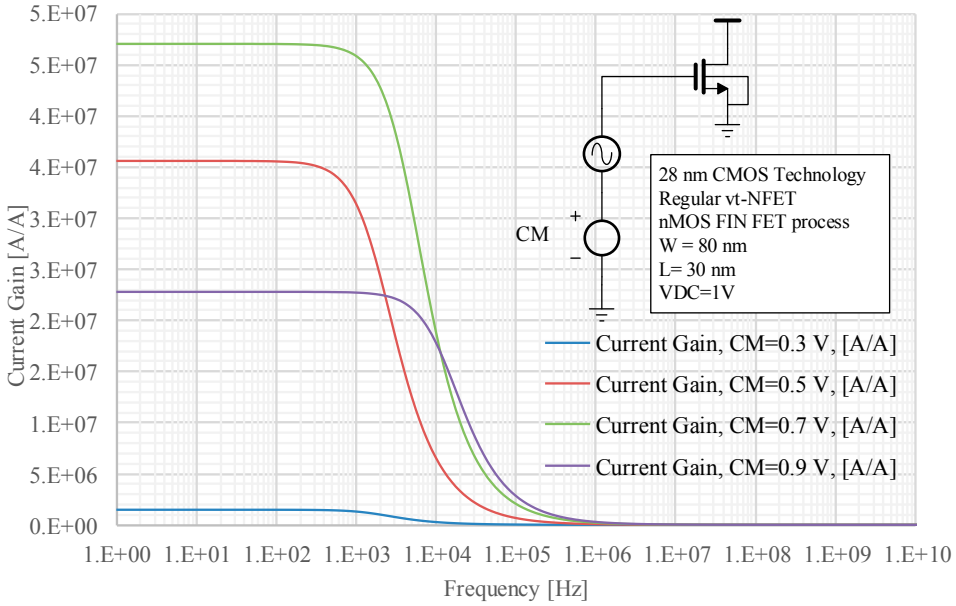


Figure 3-7 Current Gain for a 28 nm NMOS. Voltage Gate bias Creates Different Current Gain Profiles

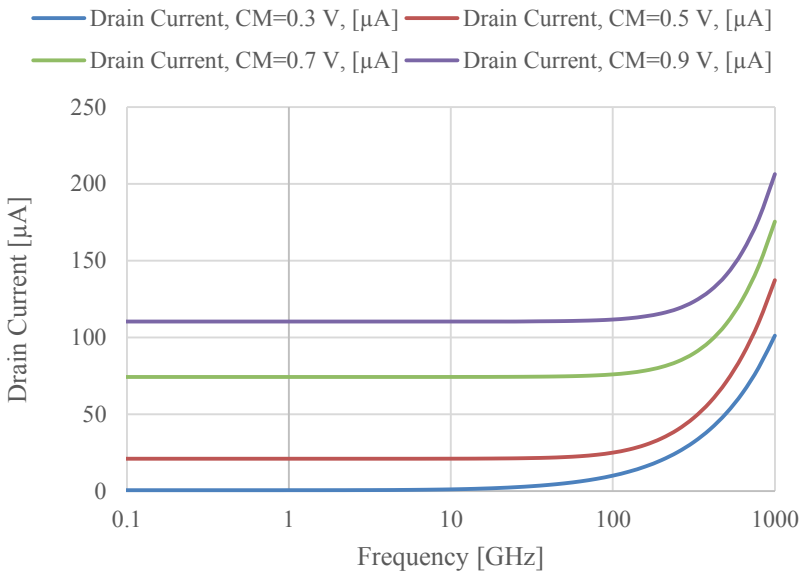


Figure 3-8 Drain Current for a 28 nm NMOS. Voltage Gate Bias Creates Different Current Gain Profiles

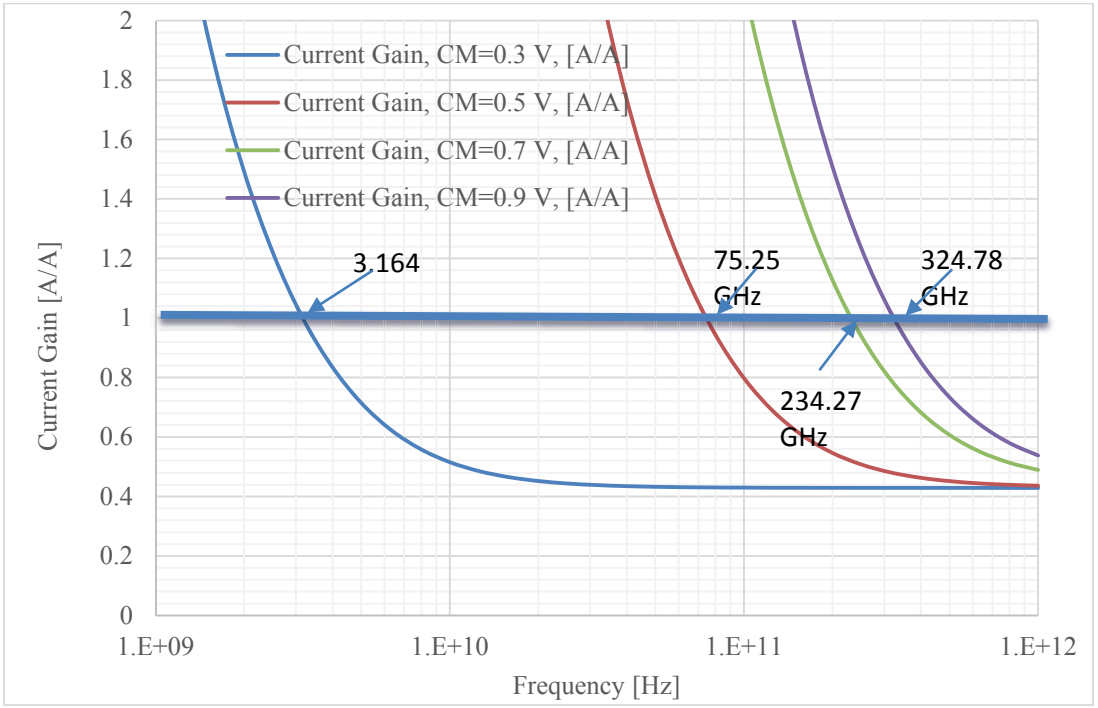


Figure 3-9 Transit Frequency. Current Gain for a 28 nm NMOS. Transit Frequency is the Frequency that Intersect the Gain of 1 A/A

In order to achieve maximum transistor performance, the common mode voltage is selected in such a way that maximum bandwidth for the application is attained while conserving power by decreasing the drain current. For example, if the design application asks for a 3 GHz bandwidth, then the common mode voltage should me selected at 3 V d.c. which will result in a drain current of no more than 3.11 μA. However, for applications that demand a higher bandwidth, the drain must be increased up to over 110 μA.

Knowing the transfer function of a transistor greatly increases the ability to predict and set the maximum and minimum gate bias voltage that is needed for the design. The small current input is directly proportional to the small input voltage ($i_i \propto v_i$). Therefore, to test the limitations of a targeted design, the requirements of the input voltage will make an affect in the transit frequency of the transistor because the limiting gate voltage bias is defined by Equation **(3-53)**.

Reducing the gate voltage bias (V_{GG} or CM voltage) results in reducing the transit frequency. Figure 3-9 shows a family of curves that demonstrates how a change in the gate voltage bias results in a shift of transit frequency. The transistor size is unchanged as well as the magnitude of the small input voltage which is a design dependent variable.

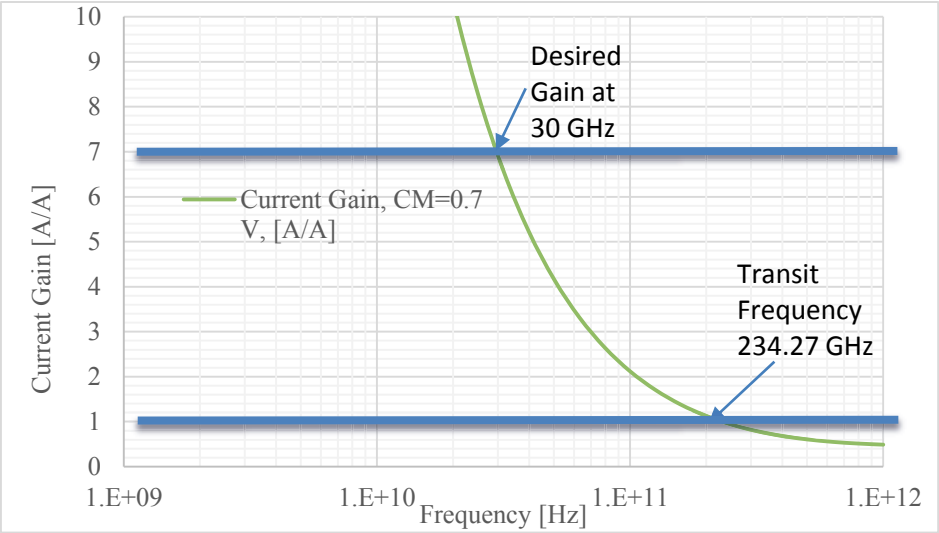


Figure 3-10 Current Gain for a 28 nm NMOS. Common Mode Voltage ($\boldsymbol{V_{GG}}$) set at 0.7 V. Transit Frequency at Current Gain of 1 A/A is 234.27 GHz. Desired Current Gain at 30 GHz is Around 7 A/A. Drain Current at Desired Design Frequency of 30 GHz is 74.48 µA

For example, Figure 3-10 shows that—for a given wanted current gain—the transistor's current should be high enough to achieve the desired gain—in this example the desired gain is 7 A/A. But the drain current must be small enough to sustain the bandwidth of 30 GHz. Therefore, the maximum transconductnce efficiency ($\frac{g_m}{I_D}$) for the example expressed herein is shown in Figure 3-10. To maintain maximum speed for the transistor, the minimum length for the 28 nm technology is 30 nm. Varying the width parameter would not affect much the speed of the transistor. From the figure above, it can be observed that the amplifier should be set with a gate-to-source voltage at 0.7 V d.c. To control the common source amplifier's transconductance, the width of the transistor can vary above 80 nm. However, doing so will decrease the amount of current needed to attain the needed results. As a result, for high speed or high transmission

rates, the most optimum size for the active amplifier is that that has the intrinsic transistor's width and length.

3.3 Transit Frequency Using the NMOS Diode Setup Model

This section describes the second method used to extract the transit frequency parameter. This section describes possible error assumptions for the extraction of the transit frequency which is ultimately used in the $\frac{g_m}{I_d}$ method [16]. This method is the most popular method for extraction of CMOS technology parameters[14].

An NMOS transistor gate is shorted as illustrated in Figure 3-11 to its drain and a variable voltage is applied to these pins. The source and bulk terminals of the transistor are connected to ground. This configuration test model is known as the diode configuration mode and allows for the extraction of not only the transit frequency (f_T) but also the extraction of the transistor's threshold voltage (V_{th}), the transonductance gain (g_m), and the transistor's technology dependent parameters ($\mu_n C_{ox}$). However, other models are needed to extract the drain-to-source resistance (r_{ds}), and the intrinsic gain ($g_m r_{ds}$).

[14] "Aim: Design of MOS amplifier using gm/Id method." Retrieved from http://discovery.bits-pilani.ac.in/discipline/eee/agupta/microelectronic-circuits/spice-online/online-2/gm-id-examples.pdf on February 22, 2013.

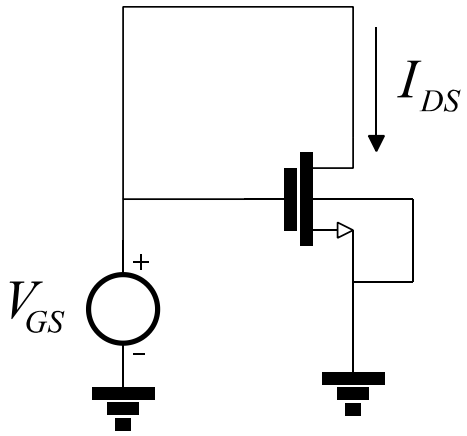


Figure 3-11 NMOS Diode Configuration to Extract Transistor Technology Parameters

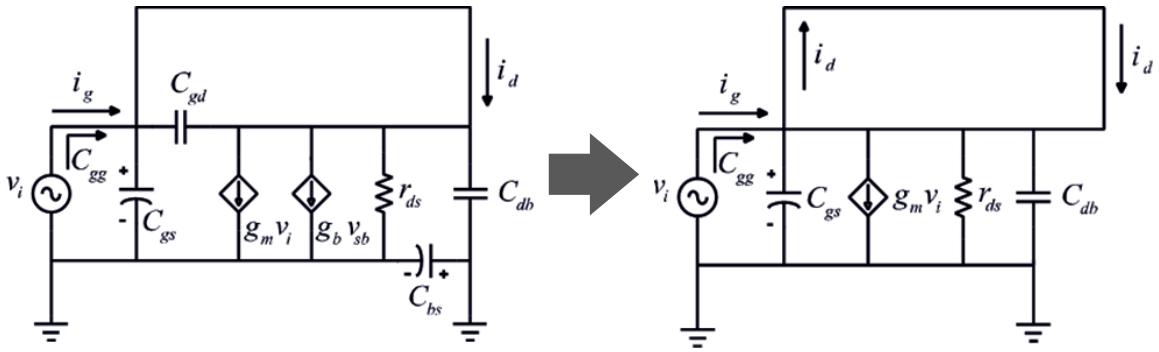
Figure 3-11 shows the setup for simulation circuit where it can be observed that the transistor is set in the diode configuration. This is done primarily to set the gate voltage (V_{GS}) equal to the drain voltage (V_{DS}).

The simulation is set up to vary the gate voltage (V_{GS}) from -0.1V d.c. to 1V d.c. The negative voltage is needed by Spectre®, the software simulation tool, to simulate derivatives of drain current when the gate value is zero volts. As a result, plotting the drain current (I_{DS}) versus the drain-to-source voltage (V_{DS}) is the same as plotting the drain current versus the gate voltage (V_{GS}).

The gate-to-source voltage is considered the input voltage while the drain-to-source voltage is considered the output voltage. Under these conditions, the system's voltage gain is at all times unity because these voltages are always the same.

$$\frac{V_{DS}}{V_{GS}} = A_o = 1\ [\frac{V}{V}] \tag{3-58}$$

The small signal model for the circuit described in this section is shown in Figure 3-12.



(a) (b)

Figure 3-12 NMOS Diode Configuration. (a) Small Signal Model for Figure 3-11 Circuit. (b) π-Model for NMOS Diode Configuration

It can be observed that changes in the circuit test model yields a significant change in how the equivalent gate capacitance is calculated (C_{gg}).

$$i_g + i_d - i_d + i_{ds} = 0 \tag{3-59}$$

$$\Rightarrow i_g = -i_{ds} \tag{3-60}$$

$$= -v_i\left[g_m + s\left(C_{gs} + C_{db}\right)\right] \tag{3-61}$$

$$= v_i s C_{gg} \tag{3-62}$$

$$\Rightarrow s C_{gg} = -g_m - s\left(C_{gs} + C_{db}\right) \tag{3-63}$$

$$= -\mu_n C_{ox} \frac{W}{L} v_i - s\left(C_{gs} + C_{db}\right) \tag{3-64}$$

The transit frequency in this case is extracted by assuming the small signal voltage gain ($|A_o|$) is directly proportional to the small signal current gain ($|h_{21}|$).

$$|A_o| = \left|\frac{V_{DS}}{V_{GS}}\right| = \left|\frac{i_d s C_{dd}}{i_g s C_{gg}}\right| = |h_{21}| \left|\frac{C_{dd}}{C_{gg}}\right| \tag{3-65}$$

$$1 = |A_o| \propto |h_{21}| \tag{3-66}$$

As a result, the small voltage gain results in a direct proportionality of current gain,

$$|A_o| \propto |h_{21}| \tag{3-67}$$

Many authors[15] [16][17] implement the transconductance efficiency ($\frac{g_m}{I_{ds}}$) model with the assumption that the transit frequency is,

$$f_T = \frac{1}{2\pi C_{gg}} \tag{3-68}$$

And some of these authors [17] define the gate capacitance as,

$$C_{gg} \triangleq C_{gs} + C_{gd} + C_{db}; \textit{ assumed by some authors} \tag{3-69}$$

In the event that the transistor is arbitrarily set in saturation mode [15], the input capacitance can be approximated by,

$$C_{gg} \cong C_{gs}; \textit{ in saturation mode only} \tag{3-70}$$

It has been demonstrated in the previous section that the gate capacitance is not what determines the transit frequency but rather what determines the transit frequency is a combination of:

(a) The circuit test model setup;

(b) The small input frequency to the gate of the transistor;

(c) The length parameter of the transistor;

(d) The gate bias voltage;

---

[15] Ardalan. *Analog CMOS Design:* $\frac{g_m}{I_{ds}}$. Lecture Notes. San Jose State University; Fall 2012. See also Foot note 14 herein.

(e) The supply voltage; and

(f) The way the transit frequency is measured in Spectre® using the Cadence Design Suite (CDS) software simulator.

For the circuit described in this section, the transit frequency is commonly extracted by assuming that,

$$f_T = \frac{g_m}{C_{gs}} \tag{3-71}$$

$$f_T = \frac{1}{C_{gs}} \frac{\partial I_{DS}}{\partial V_{DS}} \tag{3-72}$$

In order to plot the transit frequency, Equation **(3-72)** by swiping the gate voltage using the dc analysis in CDS Virtuoso® using the 45 nm from a standard General Process or Cadence® Design Kit (GPDK) library. The following mathematical formula was entered into the Virtuoso® Visualization & Analysis XL Calculator to plot the transit frequency of the schematic model as suggested by some authors:

deriv(IS("/NM1/D"))/(2*pi*OPT("/NM1","cgs"))

Such formula yields a curve with negative frequencies which suggests that there is something fundamentally wrong with Equation (3-71).

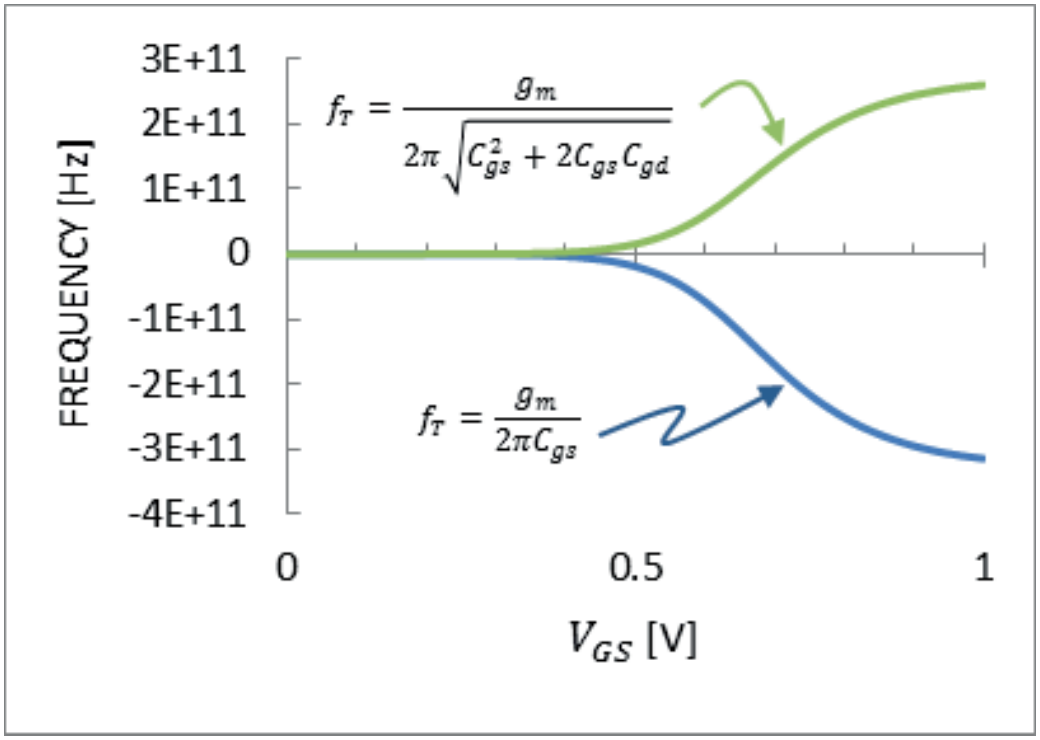


Figure 3-13 Difference Between Classic Transit Frequency—Shown with Negative Frequencies—and Transit Frequency Proposed in this Paper—Shown with Positive Frequencies

However, this paper proposes to measure the transit frequency as calculated in equation (3-37), which results in a transit frequency is positive which suggests that the calculation derived in this paper is valid for the calculation of transit frequencies (Figure 3-13).

Figure 3-13 indicates that since the voltage gain is always unity no matter what the gate voltage is, the current gain is assume to be unity also (see Equation (3-67)) and the graph represents a transit frequency of a transistor as long as it is saturated. Therefore, the graph is only valid for input gate voltages, and transistor sizing that is consistent of setting the transistor in the saturation region. As a result, the transit

frequency graph—when extracted by the diode method—is not appropriate for transistors that are set below the saturation region.

For example, it was found that the maximum transit frequency for the 45nm technology is 260.5609 GHz when L=45 nm, W=120 nm, and the circuit test model is set in the diode mode at V_{GS}=1V.

For the 28 nm CMOS technology described herein, the result for transit frequency can be calculated in many ways. One way is by using Virtuoso® by sweeping the gate voltage on a NMOS transistor wired in the diode configuration (Figure 3-11). Table 3-1 shows the calculated values for the transfer frequency using three different formulas. As it can be seen, there is a significant variation between the formulas result. This may imply that there may not be a precise consensus as to what is the best way to measure the transit frequency of a MOS device.

Table 3-1 Transfer Function Results for a 28 nm NMOS Capacitor using Cadence® Virtuoso® Tools.

Equation Reference	Transit frequency Equation	28 nm Transit Frequency [THz]
(3-71) Simplified from [16][17]	$f_T = \frac{g_m}{C_{gs}}$	282.6240
(3-68) [16][17]	$f_T = \frac{g_m}{2\pi C_{gg}}$	44.9810
(3-37) This thesis	$f_T = \frac{g_m}{2\pi\sqrt{{C_{gs}}^2 + 2C_{gs}C_{gd}}}$	25.9698

It is noted that the transit values expressed above are based on the constant value results that Virtuoso® outputs. In order to accurately measure the transit frequency, it is necessary to find a different way to measure the transistor capacitances because Virtuoso® outputs only one capacitance value for all the possible values of the gate voltage.

In order to calculate the capacitance for the gate or drain given an specific voltage across the capacitance, a transient analysis must be performed. Capacitance can be calculated as follow:

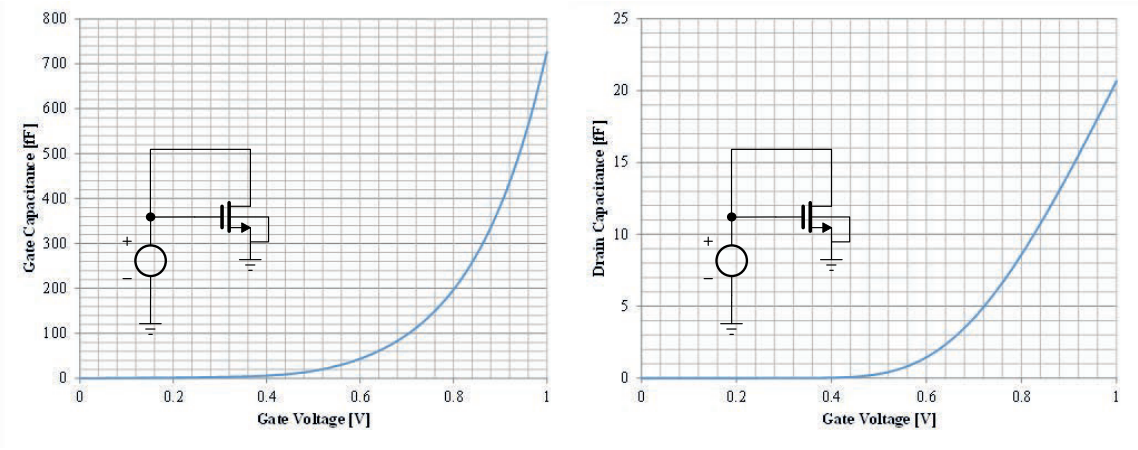
$$C(t) = \frac{dQ(t)}{dV(t)} \tag{3-73}$$

$$\frac{C(t)}{dt} = \frac{1}{dt}\frac{dQ(t)}{d(v)} \tag{3-74}$$

$$C(t) = \frac{I(t)dt}{dV(t)} \tag{3-75}$$

$$C(t) = \frac{I(t)}{\left(\frac{dV(t)}{dt}\right)} \tag{3-76}$$

Equation **(3-76)** can be used to calculate the gate and drain capacitance for the circuit from Figure 3-11.



(a) (b)

Figure 3-14 28 nm NMOS Technology. (a) Gate Capacitance; (b) Drain Capacitance

Based on the calculated capacitances from Figure 3-14, the transfer function can be plotted. To do this, it was necessary to first calculate the transconductance gain (g_m) can be calculated by sweeping the gate voltage as follow:

$$g_m = \frac{i_D}{v_G} \tag{3-77}$$

$$= \frac{\partial I_D}{\partial V_G} \tag{3-78}$$

$$g_m(t) = \frac{\left(\frac{\partial I_D(t)}{\partial t}\right)}{\left(\frac{\partial V_G(t)}{\partial t}\right)} \tag{3-79}$$

Figure 3-15 shows the transconductance gain as voltage is swept from 0 V to 1 V and then from 1 V to 0V. Note that there is a hysteresis behavior on the transconductance result.

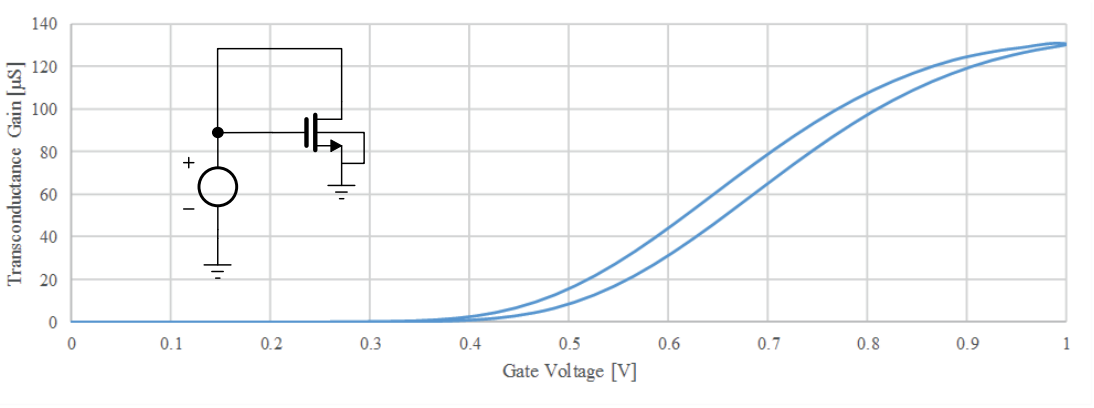


Figure 3-15 28 nm NMOS Technology. Transconductance Gain (g_m) for NMOS Connected in the Diode Configuration.

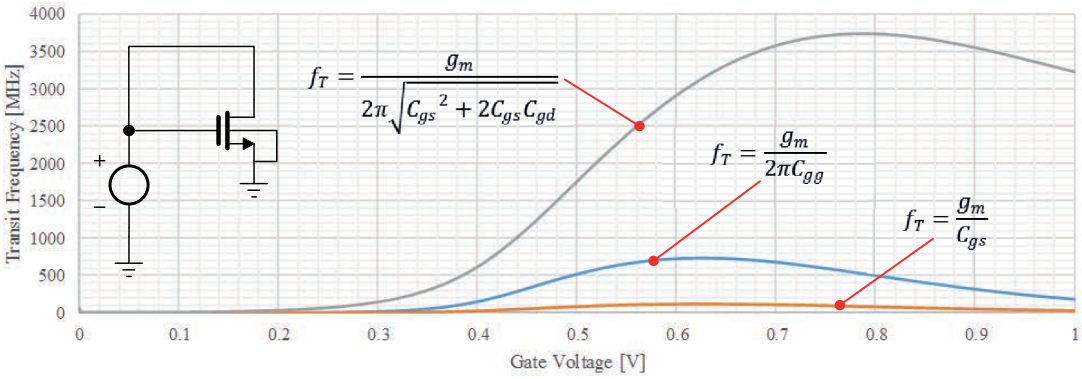


Figure 3-16 28 nm NMOS Technology. Different Derivations Comparison for Transit Frequency when the NMOS is Connected in the Diode Configuration.

Figure 3-16 shows the calculated transit frequency (f_T) from two popular formulas and this thesis proposed formula. Note that the transit frequency measurements for the NMOS connected in the diode configuration does not correspond to the measured and more accurate model as shown in Figure 3-4 and Figure 3-9. Therefore, measurement results for transit frequency is highly dependent on how the circuit is connected. In this case, a diode configuration circuit provides a sort of transconductance gain with a bandwidth amplification that is between 3.5 GHz and 4 GHz.

3.4 Important NMOS Parameters Needed to Design an Amplifier

Based on Figure 3-4, some of the most absolute maximum values for small signal parameters in the 28 nm NMOS device can be obtained by the following equations by sweeping the gate voltage as a function of time ($V(t)$):

$$C_G(t) = \frac{I_G(t)}{\left(\frac{\partial V_G(t)}{\partial t}\right)} \tag{3-80}$$

$$i_G(t) = \frac{v_G(t)}{z_G(t)} \tag{3-81}$$

$$= \frac{\left(\frac{\partial V_G(t)}{\partial t}\right)}{\left(\frac{\partial Z_G(t)}{\partial t}\right)} \tag{3-82}$$

$$i_G(t) = \frac{\left(\frac{\partial V_G(t)}{\partial t}\right)}{\left\{\frac{\partial\left(\frac{V_G}{I_G}\right)(t)}{\partial t}\right\}} \tag{3-83}$$

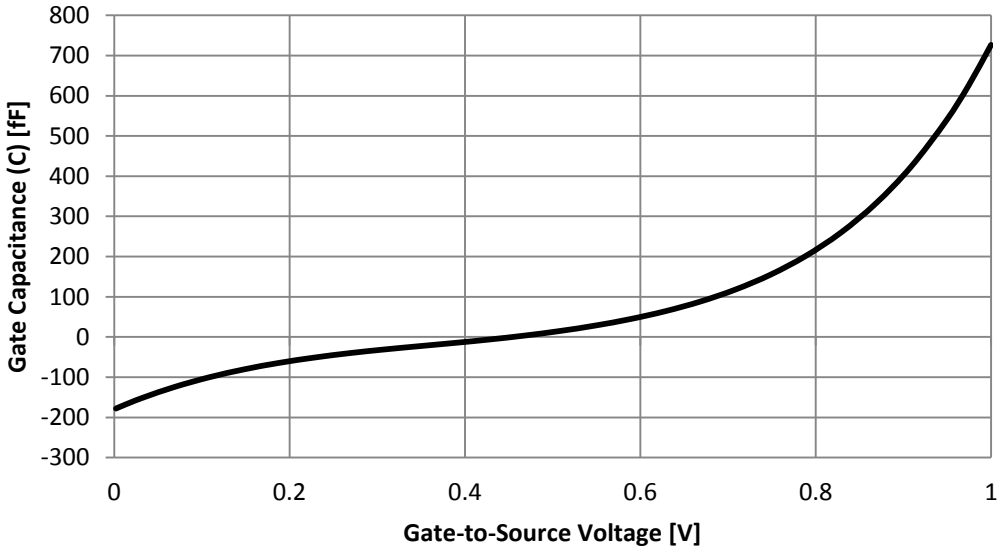


Figure 3-17 Gate Capacitance for 28 nm NMOS Technology. Small Signal Parameter

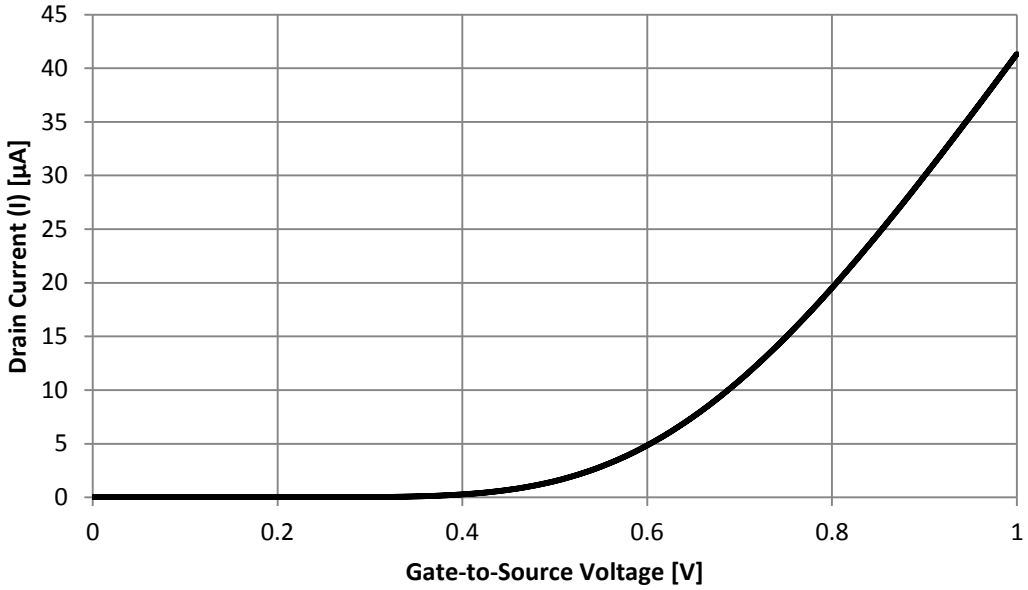


Figure 3-18 Maximum Drain Current for 28 nm NMOS Technology. Large Signal Parameter. NMOS Intrinsic Transistor Sized to 30 nm Width and 80 nm Length

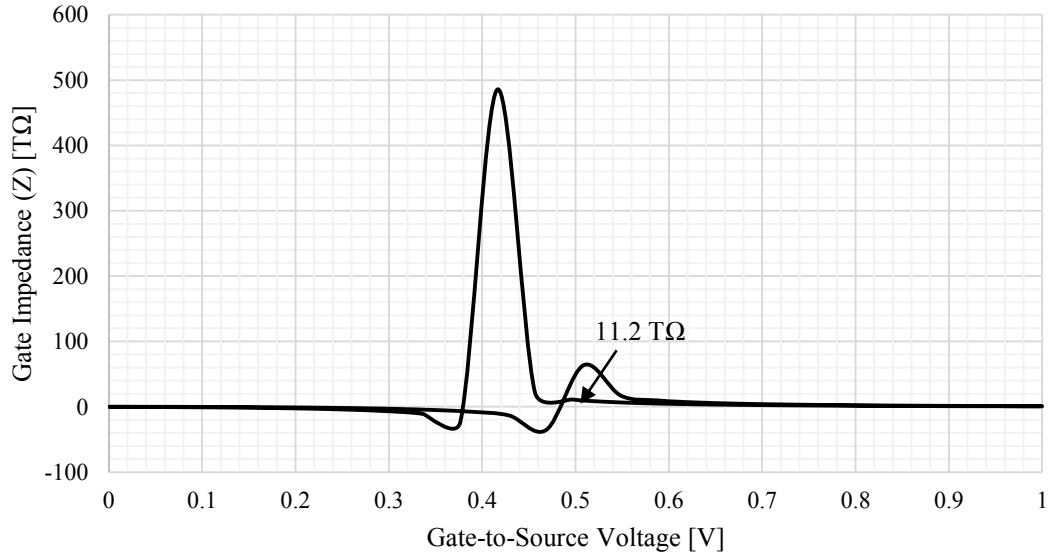


Figure 3-19 Hysteresis Gate Impedance for 28 nm NMOS Technology. Large Signal Parameter

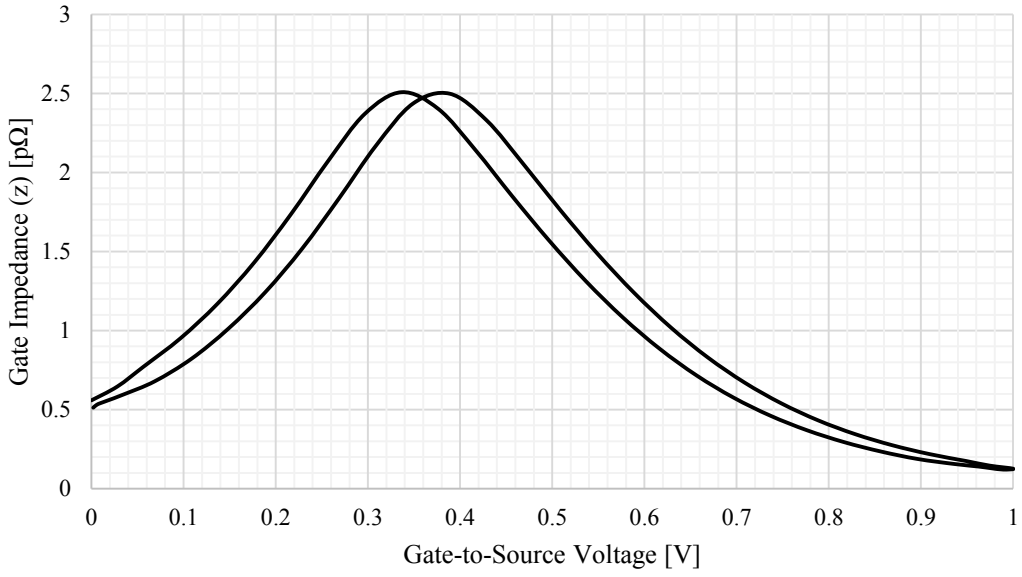


Figure 3-20 Hysteresis Gate Impedance for 28 nm NMOS Technology. Small Signal Parameter

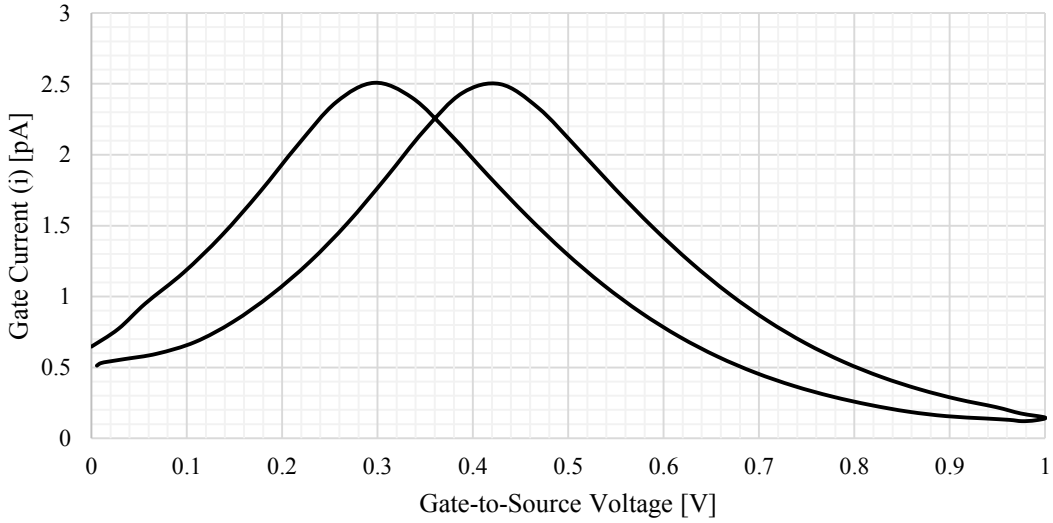


Figure 3-21 28 nm NMOS Technology. Different Derivations Comparison for Transit Frequency when the NMOS is Connected in the Diode Configuration

3.5 Current Sources

As indicated in the previous section, the drain current of a transistor increases as the bandwidth and current gain requirements increase. In the case of the 28 nm NMOS transistor, the absolute maximum current biased with a gate-to-source voltage (V_{GS}) of 0.7 V is 10 µA. Therefore, a current source (I_S) needs to be designed to deliver such current. Figure 3-22 illustrates a current mirror circuitry that will be set to provide a maximum of 10 µA. The current source (I_S) can be adjusted or programed by the PMOS transistor (P1) by with a control bias voltage ($V_{BIAS\ CONTROL}$). Current output can be adjusted by adjusting the width of transistor N2. It was found that for the 28 nm technology, the drain current ratio between transistors N1 and N2 is around 2. To improve the layout of the circuit, a transistor parameter called "*number of gate fingers*" parameter was varied on transistor N2. The number of gate finger parameter value is multiplied the gate width parameter to increase the overall transistor's gate width. In order to minimize circuit power consumption, the width parameter for transistors N1 and N2 were set to 80 nm while their length parameter were set to 30 nm. To adjust the desired current, the finger parameter for transistor N1 was set to unity while the transistor N2 finger parameter was incrementally increased to measure the drain current of N2. The control voltage ($V_{BIAS\ CONTROL}$) was set to zero volts to saturate PMOS transistor P1. The width and length parameters for transistor P1 were also set to 28 nm and 80 nm respectively with a unity finger parameter.

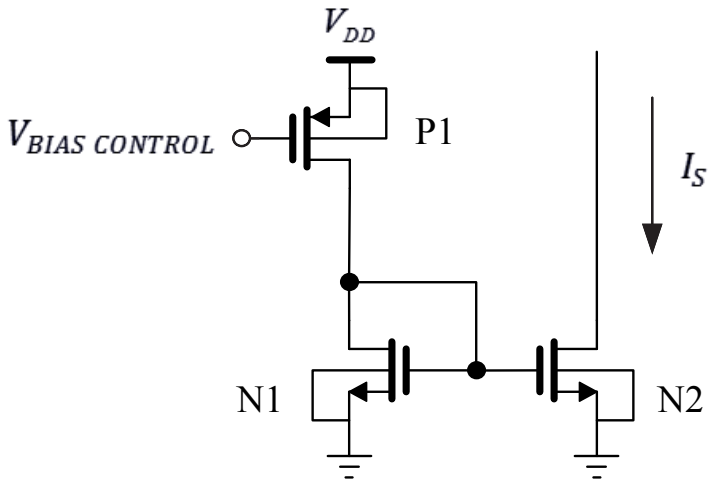


Figure 3-22 Programmable Current Mirror to Provide a Source Current (I_S)

The results for the current mirror can be seen in Figure 3-23. The voltage control is turned off after 25 ms. The drain terminal for transistor N2 is connected to the source voltage without d.c. filtration. As a result, there is a ringing voltage when the control turns on the current mirror circuit.

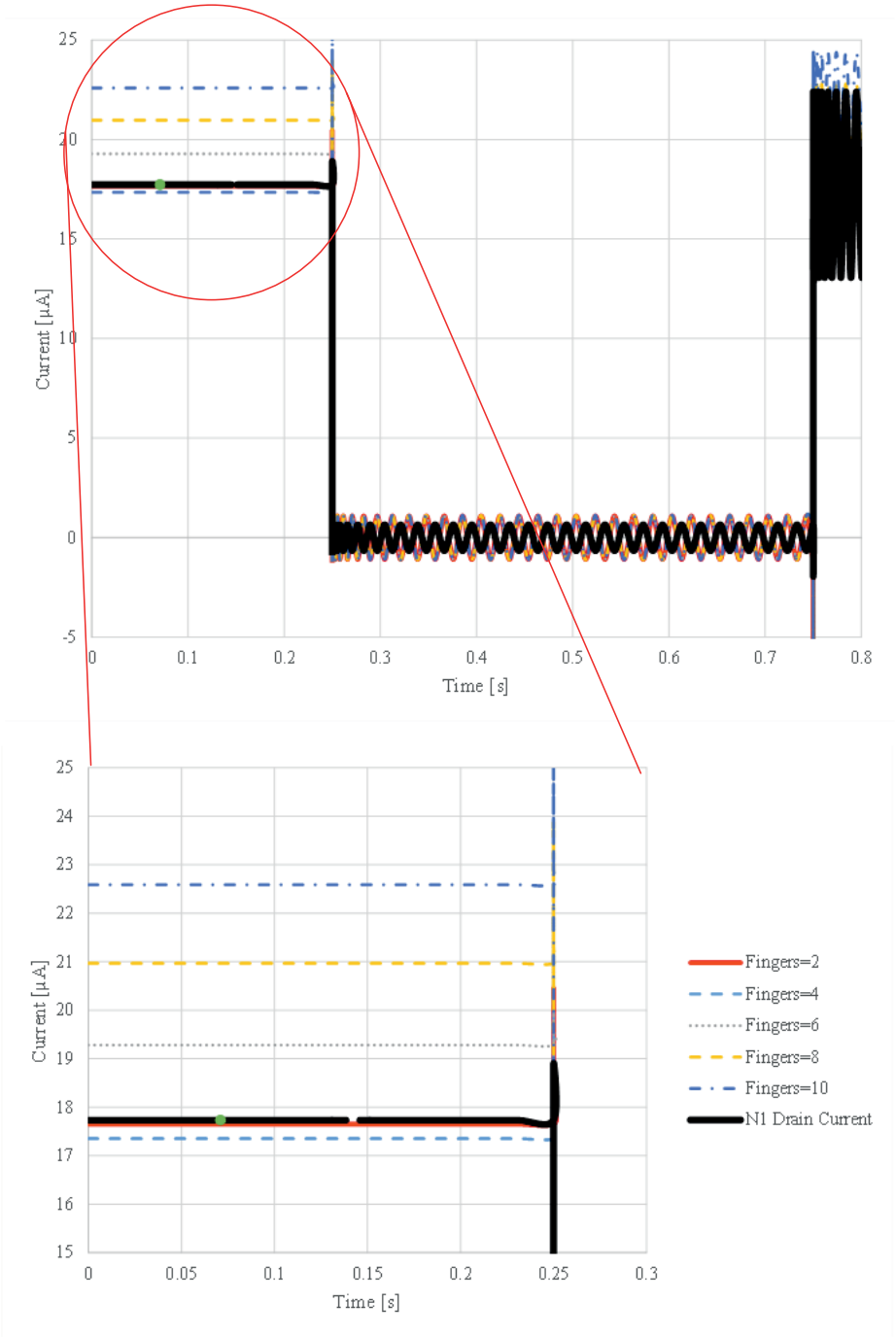


Figure 3-23 Current Mirror Measurements. Current Source (I_S) is Adjusted by Increasing the Number of Gate Fingers Parameter in the N2 Transistor

3.6 Basic Amplifier

The basis of an equalizer is an amplifier with wide bandwidth. Figure 3-24 shows a common source NMOS differential amplifier. To derive the transfer function for this type of amplifier, the circuit is simplified by dividing the circuit in two.

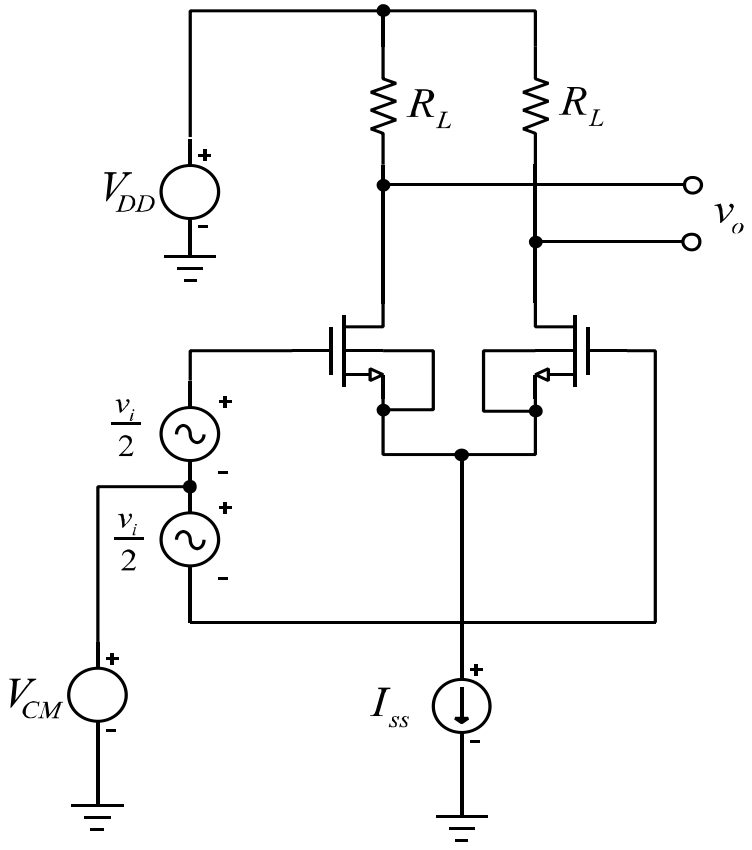


Figure 3-24 Common Source NMOS Differential Amplifier

Note that a differential amplifier is composed of two identical mirror circuit legs that share the same current source (I_{SS}). Figure 3-25 represents the simplified circuit leg. The differential voltage gain and the simplified circuit voltage gain are identical. As a result, the amplifier can be modeled and designed from a simplified version which reduces the amount of hours spent doing circuit analysis.

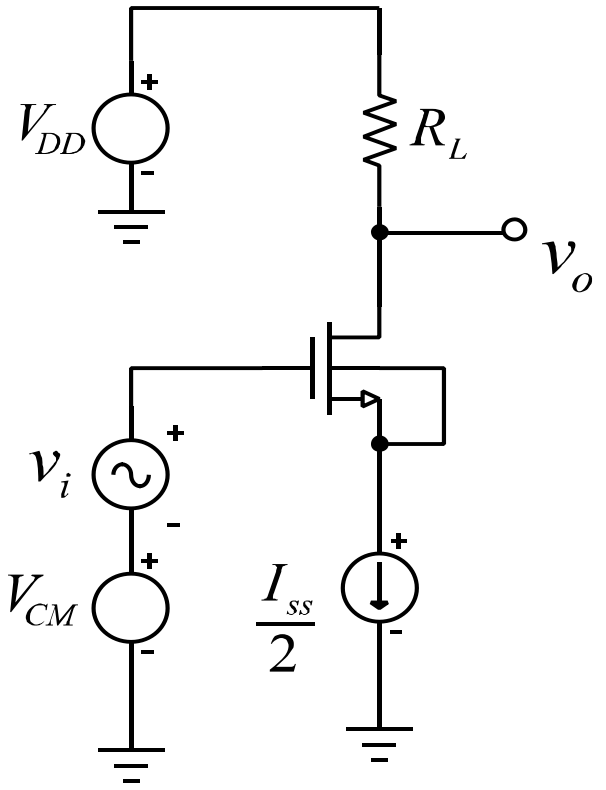


Figure 3-25 Simplified Common-source NMOS Circuit Leg for a Differential Amplifier

To implement this circuit using a design tool, the current source (I_{SS}) is replaced by a current mirror circuit (Figure 3-26). The current control ($V_{I_{SS},BIAS}$) is set to zero volts to maximize the amount of current created by the current mirror circuit. The capacitance seen at the gate of the NMOS transistor is affected by the capacitance of the current mirror drain capacitance. As a result, the circuit transit frequency and other electrical parameters change. Therefore, it is important to set the source current circuitry first before continuing making analysis and measurements.

It was already established, that if a high bandwidth circuit of 30 GHz with a current gain above 5 A/A is desired, the common mode voltage must be set above 0.7 V.

It was also established that the drain current of the amplifier must be around 74.48 µA. And it was also established that the current source analysis for one leg is of the differential amplifier is half of what is required for the entire circuit.

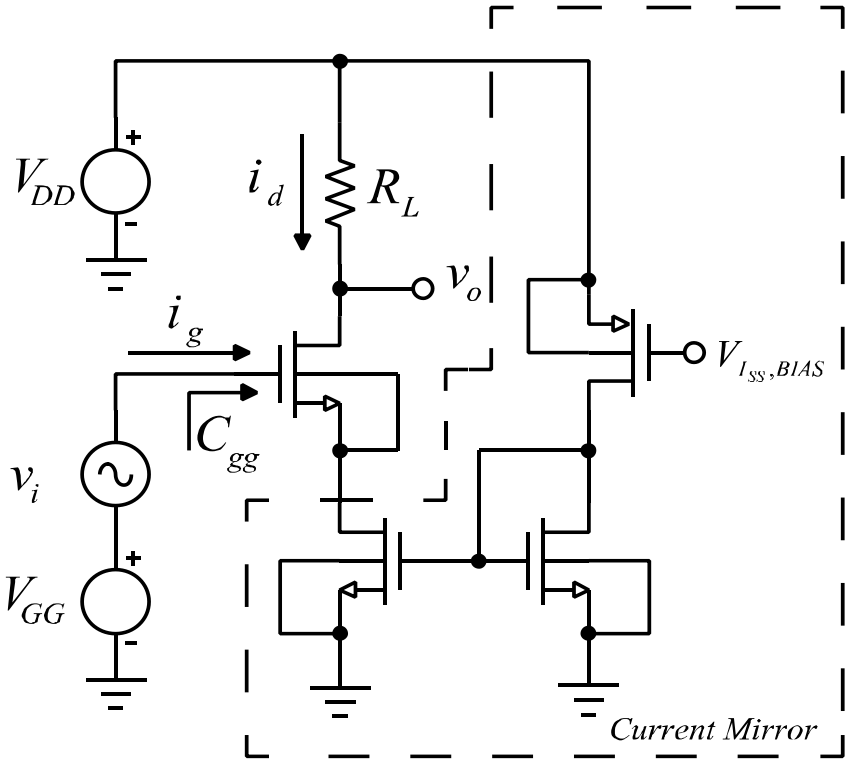


Figure 3-26 Common Source NMOS Differential Amplifier

In order to increase the source current to the amount needed, the number of gate fingers parameter must be increased to 170 fingers which generate a current of 149.1955 µA (Figure 3-27). This means that the intrinsic width parameter is increase from 80 nm for one finger to 12 µm for 150 fingers. As a result, the capacitance seeing at the gate of the amplifier is affected by the current source capacitance. This capacitance is critical to attain high bandwidth in the amplifier.

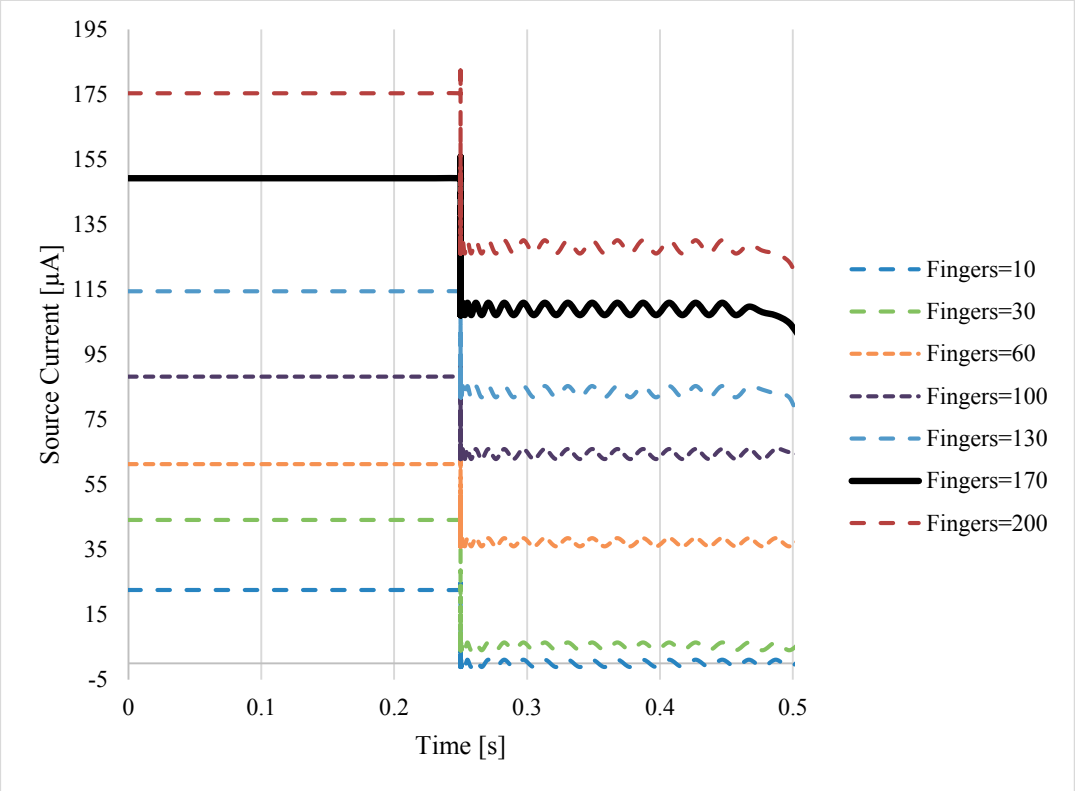


Figure 3-27 Amplifier's Source Current. Solid Line Represents Desired Finger Size

Note that the current control is not capable to bring down the current to zero Amps. To fix this, a programmable load is added to the circuit to regulate the current (Figure 3-28

Once the current mirror fingers has been set to provide the desired current source, the current is half by adjusting the current mirror control voltage ($V_{I_{SS},BIAS}$). In other words, each differential NMOS transistor acting as the amplifier must have a bias current leg of 74.5 µA to ensure that all quiescent points are set for maximum bandwidth.

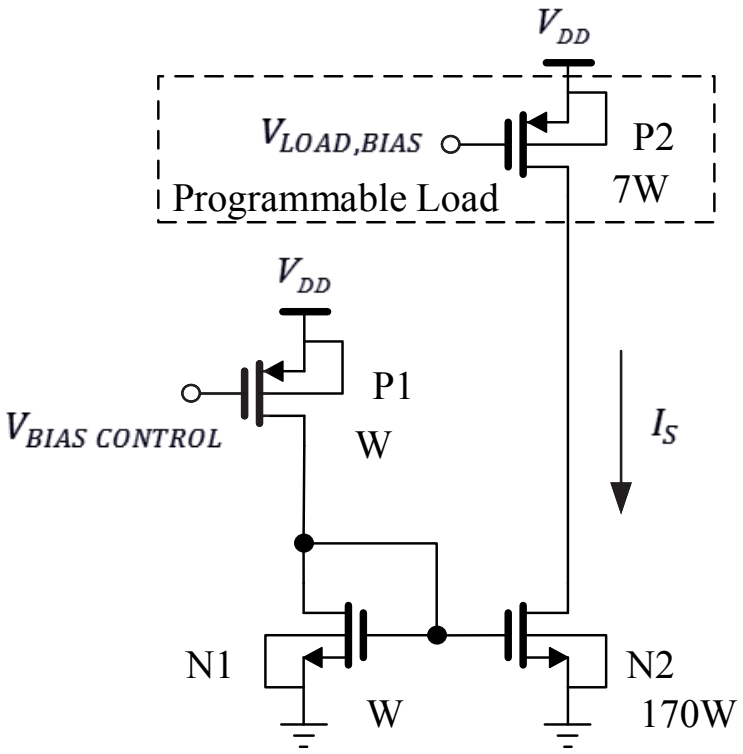


Figure 3-28 Amplifier Circuit Current Source

The current source is active or reduced by the current mirror control ($V_{BIAS\ CONTROL}$) while the programmable load is controlled by PMOS P2 gate voltage ($V_{LOAD,BIAS}$).

Figure 3-29 shows the complete circuit for a simple high-bandwidth common source amplifier. The voltage load ($V_{LOAD,BIAS}$) is adjusted to the most optimum output gain. The input common voltage is the gate bias voltage for the amplifier.

Figure 3-30 shows the different voltage gain curves or frequency response for the amplifier in Figure 3-29. This design is capable to amplify frequencies higher than 30 GHz if the load voltage bias is set to 0.42 v.

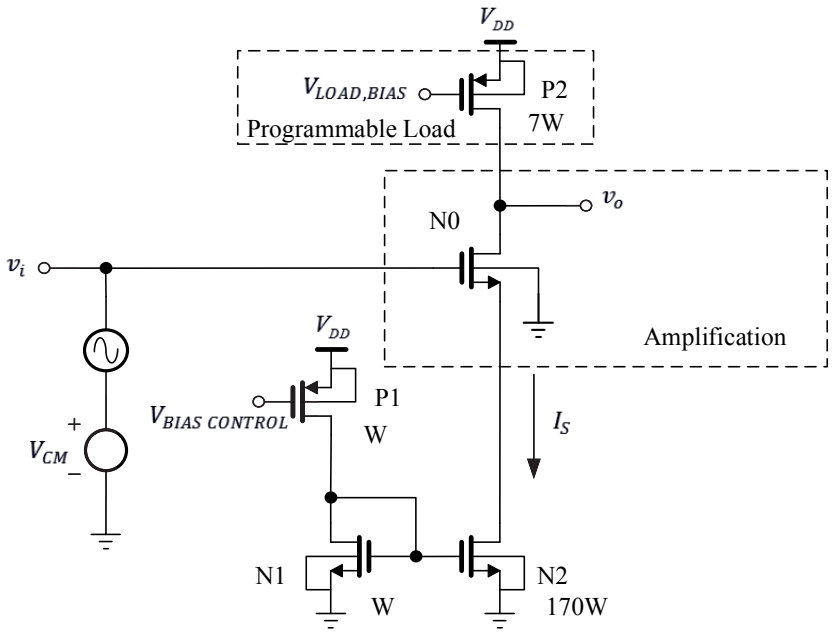


Figure 3-29 High-bandwidth Common Source Amplifier with Programmable Load and Current Source Control. Common Mode Voltage is Setup at 0.7 V

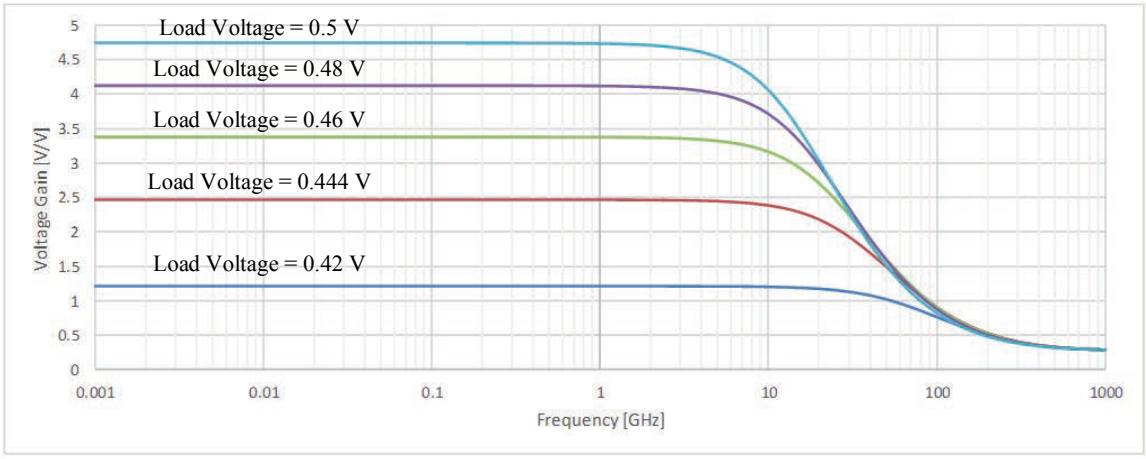


Figure 3-30 High-bandwidth Amplifier Design with Various Voltage Gain Outputs

Figure 3-29 shows the configuration of an open loop common source NMOS amplifier connected to a current mirror to adjust the source current (I_{SS}) which is controlled by the PMOS voltage gate bias ($V_{BIAS\ CONTROL}$).

It was observed that the current mirror impedance affects the overall bandwidth of the circuit. By introducing the design of a current mirror to the amplifier, the IC designer can size to an existing predefined design.

Figure 3-31shows the small signal analysis for the common source amplifier with load R_L.

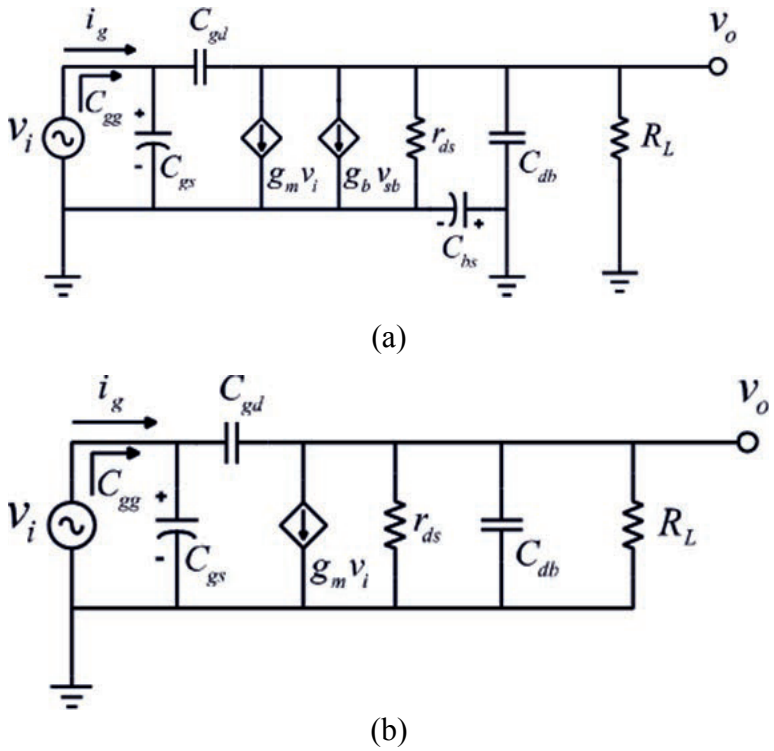


Figure 3-31 Small Signal Model for Simplified NMOS Amplifier. (b) Simplified Small Signal Model for NMOS Amplifier.

The small signal transfer function for voltage gain is obtained as follow,

$$\frac{V_o}{V_i} = -\frac{sC_{gs} + g_m}{\frac{1}{r_{ds}\|R_L} + sC_{db}} \tag{3-84}$$

Equation (3-84) is manipulated to find the critical frequencies. Therefore Equation (3-84) should take the form of,

$$\frac{V_o}{V_i} = -A_v \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \tag{3-85}$$

As a result, Equation (3-84) results in,

$$\frac{V_o}{V_i} = -g_m(r_{ds}\|R_L)\left[\frac{1 + \frac{s}{\left(\frac{g_m}{C_{gs}}\right)}}{1 + \frac{s}{\left(\frac{1}{(r_{ds}\|R_L)C_{db}}\right)}}\right] \tag{3-86}$$

Where,

$$\omega_z = \frac{g_m}{C_{gs}} \text{ [rad/s]} \tag{3-87}$$

$$\omega_p = \frac{1}{(r_{ds}\|R_L)C_{db}} \text{ [rad/s]} \tag{3-88}$$

$$A_v = g_m(r_{ds}\|R_L) \text{ [V/V]} \tag{3-89}$$

Equations (3-85) to (3-89) allow analysis of the common source NMOS amplifier using the bode plot. Setting the low frequency voltage gain (A_v) to be equal to an specified voltage gain—this could vary from design to design and circuit implementation, this example uses a gain of 2—and changing the frequency scale from radians per second to Hz, we can plot a Bode plot with the following critical points:

$$f_{z,-3dB} = \frac{\omega_z}{2\pi} = \frac{g_m}{2\pi C_{gs}} \text{ [Hz]} \tag{3-90}$$

$$f_{p,-3dB} = \frac{\omega_p}{2\pi} = \frac{1}{2\pi(r_{ds} \| R_L)C_{db}} \text{ [Hz]} \tag{3-91}$$

$$A_v = 2 = g_m(r_{ds} \| R_L) \text{ [V/V]} \tag{3-92}$$

$$\left|\frac{V_o}{V_i}\right|_{dB} = 20log_{10}\left(\left|-A_v \frac{\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)}\right|\right) \tag{3-93}$$

$$s = j\,\omega \tag{3-94}$$

$$\left|\frac{V_o}{V_i}\right|_{dB} = 20log_{10}\left(\left|-A_v \frac{\left(1+j\frac{\omega}{\omega_z}\right)}{\left(1+j\frac{\omega}{\omega_p}\right)}\right|\right) \tag{3-95}$$

$$\left|\frac{V_o}{V_i}\right|_{dB} = 20log_{10}\left(\left|-A_v\frac{\left(1+j\frac{f}{f_z}\right)}{\left(1+j\frac{f}{f_p}\right)}\right|\right) \tag{3-96}$$

Seting the 3dB cut off frequency to 30GHz.

$$f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi(r_{ds}\|R_L)C_{db}}\text{=30GHz} \tag{3-97}$$

The zero-frequency (f_z) was set much larger than the pole frequency (f_p).

$$f_p \ll f_z \tag{3-98}$$

$$\frac{1}{2\pi(r_{ds}\|R_L)C_{db}} \ll \frac{g_m}{2\pi C_{gs}} \tag{3-99}$$

The IC designer has two options to make when deciding how to size or bias the circuit above. The first option is to assume that the drain-to-source resistance (r_{ds}) is much larger than the load resistance (R_L) to allow him or her to control both the gain and the bandwidth with a parameter that is linear such as the impedance of the load (R_L). As a result, the impedance of the amplifier (r_{ds}) becomes irrelevant for the designer to set the bandwidth of the circuit. The second option is to allow the load resistance to be larger than the drain-to-source resistance and use the new method proposed in this paper that allows the load resistance adjust the drain current of the circuit.

The first option is what is assumed when using the $\frac{g_m}{I_d}$ method. Therefore, the following sets of equations assume the first option and the reader can just replace the load resistance for the drain-to-source resistance for the method proposed by this thesis.

$$R_L \ll r_{ds} \tag{3-100}$$

$$r_{ds} \| R_L \cong R_L \tag{3-101}$$

$$A_v = 2 \cong g_m R_L \text{ [V/V]} \tag{3-102}$$

As a result, Equation (3-99) can be arranged as follow:

$$\frac{1}{R_L C_{db}} \ll \frac{g_m}{C_{gs}} \tag{3-103}$$

$$\Rightarrow 1 \ll \frac{g_m R_L C_{db}}{C_{gs}} \tag{3-104}$$

From Equation **(3-97**), **(3-89**), and **(3-104**) become the critical points to meet the design specifications.

$$\frac{1}{2\pi R_L C_{db}} = (30)(10^9) \tag{3-105}$$

$$g_m R_L = 2 \tag{3-106}$$

$$\Rightarrow g_m = \frac{2}{R_L} \tag{3-107}$$

$$\Rightarrow 1 \ll \frac{g_m R_L C_{db}}{C_{gs}} = \frac{2 R_L C_{db}}{R_L C_{gs}} = 2\frac{C_{db}}{C_{gs}} \tag{3-108}$$

$$\Rightarrow \frac{1}{2} \ll \frac{C_{db}}{C_{gs}} \tag{3-109}$$

The meaning of Equation (3-109) is important since it assures to choose the size of the NMOS transistor such that the ratio $\frac{C_{db}}{C_{gs}}$ is larger than 0.5. This is difficult to accomplish even when the $\frac{g_m}{I_d}$ method is used.

Another design point of interest for a common source amplifier is the zero-frequency. This frequency—if the design is used in analog designs—affects the stability of the entire circuit when the loop is closed, and sets the minimum attenuation of a signal thus becoming a factor of amplification swing. In the event that the zero-frequency needs to be defined as the frequency where the gain is zero dB, the following equation is derived.

$$\left|\frac{V_o}{V_i}\right|_{dB} = 20log_{10}\left(\left|-A_v \frac{\left(1 + j\frac{f}{f_z}\right)}{\left(1 + j\frac{f}{f_p}\right)}\right|\right) = 0 \tag{3-110}$$

$$log_{10}\left(\left|-A_v\frac{\left(1+j\frac{f}{f_z}\right)}{\left(1+j\frac{f}{f_p}\right)}\right|\right)=0 \tag{3-111}$$

$$10^0=\left|-A_v\frac{\left(1+j\frac{f}{z}\right)}{\left(1+j\frac{f}{f_p}\right)}\right| \tag{3-112}$$

$$1=A_v\sqrt{\frac{1+\left(\frac{f}{f_z}\right)^2}{1+\left(\frac{f}{f_p}\right)^2}} \tag{3-113}$$

$$\left(\frac{1}{A_v}\right)^2=\frac{1+\left(\frac{f}{f_z}\right)^2}{1+\left(\frac{f}{f_p}\right)^2} \tag{3-114}$$

$$f_z=f \tag{3-115}$$

$$\left(\frac{1}{A_v}\right)^2=\frac{2}{1+\left(\frac{f_z}{f_p}\right)^2} \tag{3-116}$$

$$1+\left(\frac{f_z}{f_p}\right)^2=2{A_v}^2 \tag{3-117}$$

$$\left(\frac{f_z}{f_p}\right)^2=2{A_v}^2-1 \tag{3-118}$$

$$f_z|_{@0dB} = \pm\sqrt{2{A_v}^2{f_p}^2 - {f_p}^2} \tag{3-119}$$

Where,

$$f_p = 30GHZ \tag{3-120}$$

$$A_v = 2 \tag{3-121}$$

$$\Rightarrow f_{z,0dB} = \pm 30 \times 10^9 \times \sqrt{7} \tag{3-122}$$

$$f_{z,0dB} \cong 79.37GHz \tag{3-123}$$

Therefore, from Equations (3-98) and (3-122), the following identity is derived,

$$(30 \times 10^9) \ll \left(30 \times 10^9 \times \sqrt{7}\right) \tag{3-124}$$

$$\frac{1}{2\pi R_L C_{db}} \ll 30 \times 10^9 \times \sqrt{7} \tag{3-125}$$

$$\frac{1}{2\pi 30 \times 10^9 \times \sqrt{7}} \cong 2\,[ps] \ll R_L C_{db} \tag{3-126}$$

3.7 Amplification Chain Biasing

One of the most difficult thing to achieve when connecting several amplifiers in series is two make sure that the bias of the input of the second stage is bias the same way as the gate bias of the first stage so that the amplifier's bandwidth is not disturbed. This can be achieved in many ways, one way is by adding a coupling capacitor between amplifiers and thereby creating a d.c. separation between each stage. In this method, each stage input gate bust be biased independently. However, it was found that adding a bias circuit for the second stage and a coupling capacitor not only reduces the gain that was attained by a previous amplification state but also reduces the desired bandwidth. Therefore, the output of a previous state must be preprogramed and balanced to bias the following amplification state (Figure 3-32).

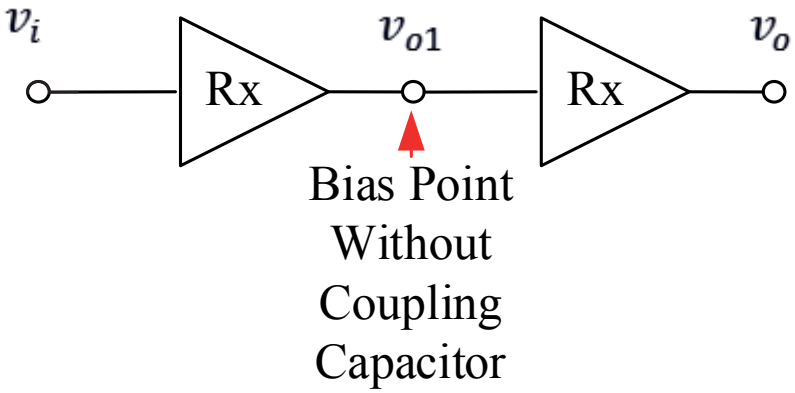


Figure 3-32 Connection of Two Identical Amplifiers Coupled without the Need of a Coupling Capacitor. Quiescent Point of First Amplifier Bias the Gate Input to the Second Amplifier

To properly bias subsequent amplification stages, the quiescent point of the previous amplification stage must be set by adjusting the active output load voltage ($V_{LOAD,BIAS}$). To do this, a transient analysis with an input pulse voltage to the input of the first stage is analyzed.

It is known that reducing the gate bias voltage or common mode voltage to the amplification stage reduces the bandwidth of the amplifier. Figure 3-33 illustrates that for the design of this thesis, the amplifier load bias voltage ($V_{LOAD,BIAS}$) must be set around 0.46 V.

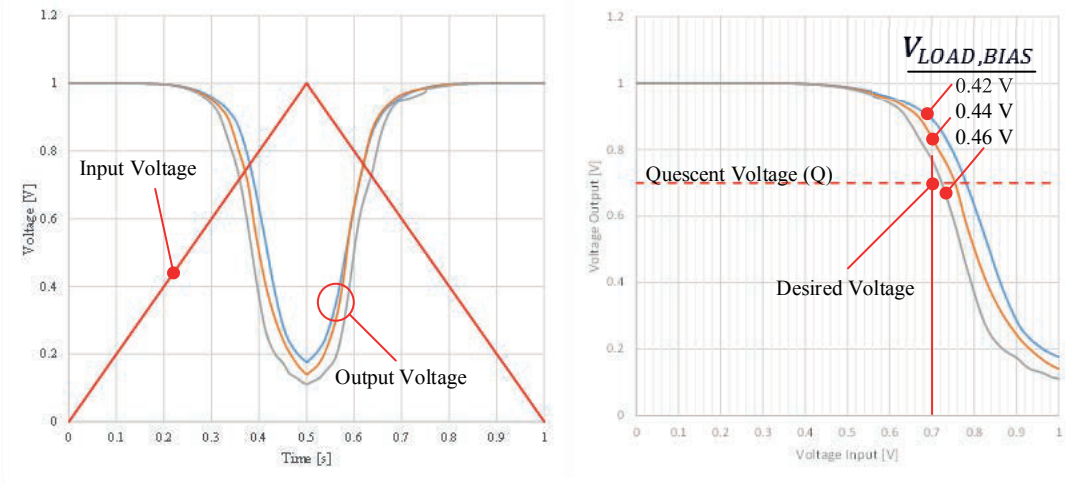


Figure 3-33 Evaluation of Amplifier Quiescent Point Voltage (Q). The Quiescent Point of the First Amplifier Stage Affects the Input Gate Bias of the Second Stage

The load bias voltage was set to 0.46 V because reducing the voltage will also reduce the gain at 30 GHz (Figure 3-30).

Table 3-2 Measured DC Parameters for Amplifier in Figure 3-21 Using Cadence® Virtuoso® Analog Design Environment—Transient Analysis

DC Amplifier Parameter	Measured value	Unit
N0 Common Mode Voltage	0.7	V
N0 Gate Capacitance	84.220778	fF
N0 Drain-to-Source Capacitance	1.121117	µF
N0 Drain Current	7.0345	µA
N0 Gate-to-Source Voltage	0.678	V
N0 Gate Resistance	4.158	TΩ
N0 Drain-to-Source Resistance	102.38587	kΩ
N2 Source Voltage	21.7103	mV
N2 Drain Capacitance	39.4	µA
N2 Drain to Source Resistance	3.08623	kΩ
Output Resistance	105.4721	kΩ
Output Capacitance	1.143	µF
Load Bias Voltage	0.46	V

Based on the measured d.c. parameters for the proposed amplifier, connecting the amplifiers in series does not cause any impedance matching issues when the amplifiers are connected in series. Observe that the output capacitance is much larger than the input capacitance which makes little effect in the overall bandwidth since the output capacitance is one of the main parameters that sets the cutoff frequency as explained in previous sections. Also, the input resistance of the amplifier is much larger than the output resistance. When these resistances are placed in parallel, the equivalent resistance is basically the output resistance of the amplifier.

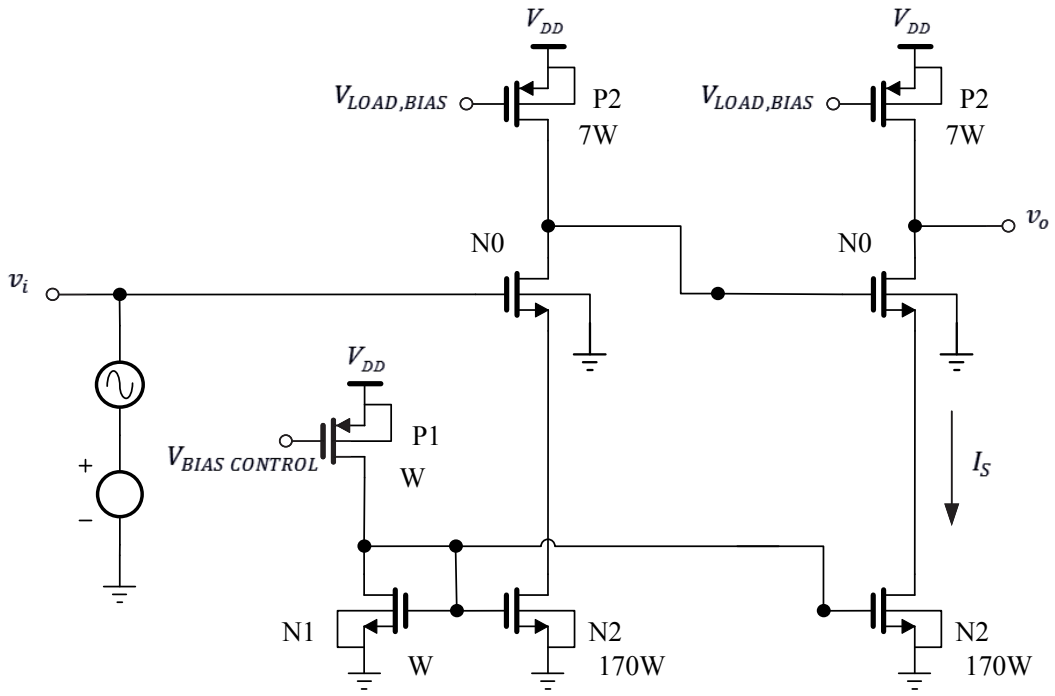


Figure 3-34 Two Stage Amplifier with No Coupling Capacitance between the Stages is Necessary

The circuit described herein can only support no more than three stages of amplification. The second stage voltage gain amplification at a frequency of 30GHz is 10.72 dB. The first stage voltage gain amplification at the same frequency is 2.70 dB. This is due to the fact that in every stage, the quiescent point moves lower than the desired 0.7 V. An impedance matching circuit should be adapted to ensure that every stage is properly biased.

3.8 Differential Amplifier Configuration.

This section describes how to connect the designed amplifier from the previous section. This circuit does not require a coupling capacitors between stages.

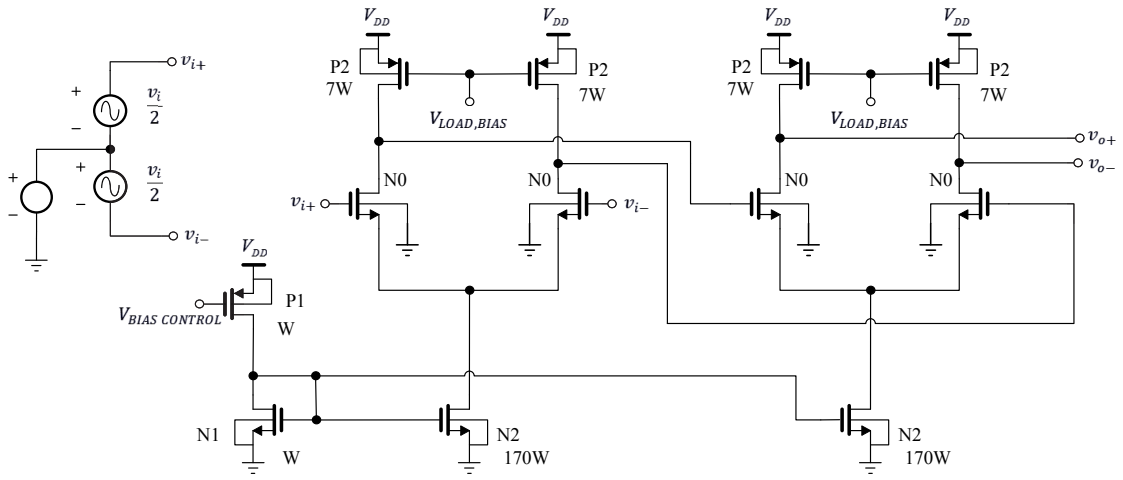


Figure 3-35 Two Stage Differential Amplifier with No Coupling Capacitance between the Stages is Necessary. Active Load and Output Power Control

The circuit depicted in Figure 3-35 has the same voltage gain response than the circuit from Figure 3-34. This circuit is also designed to reduce the signal-to-noise ratio.

3.9 Pulse Shaping

In order to create a curve that slowly tapers from zero decibels upwards to a frequency of 30 GHz, a high pass filter is connected in series with a low pass filter amplifier, This will create a band pass filter that emulates the inverse lower frequency response of a channel. Consider the circuit in Figure 3-36 with a transfer function expressed in (3-127).

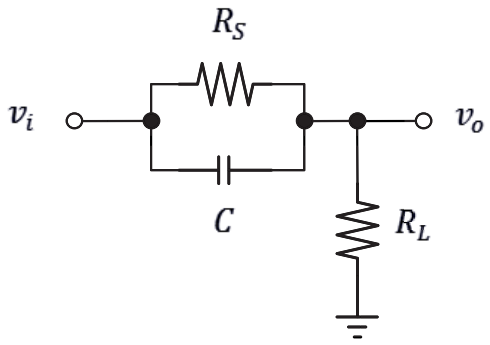


Figure 3-36 Hi Pass Filter

$$\frac{v_o}{v_i} = \frac{R_L}{R_s + R_L} \frac{\left(1 + \frac{s}{\left(\frac{1}{R_L R_s C}\right)}\right)}{\left(1 + \frac{s}{\left(\frac{R_s + R_L}{R_L R_s C}\right)}\right)} \tag{3-127}$$

$$\omega_z = \left(\frac{1}{R_L R_s C}\right) \tag{3-128}$$

$$\omega_z = \left(\frac{1}{R_L R_s C}\right) \tag{3-129}$$

$$\omega_z \ll \omega_z \tag{3-130}$$

Then the circuit is placed in series with the amplifier to form a band pass filter. Note that the series resistance (R_s) should be small so that there is little d.c. attenuation created by the high pass filter.

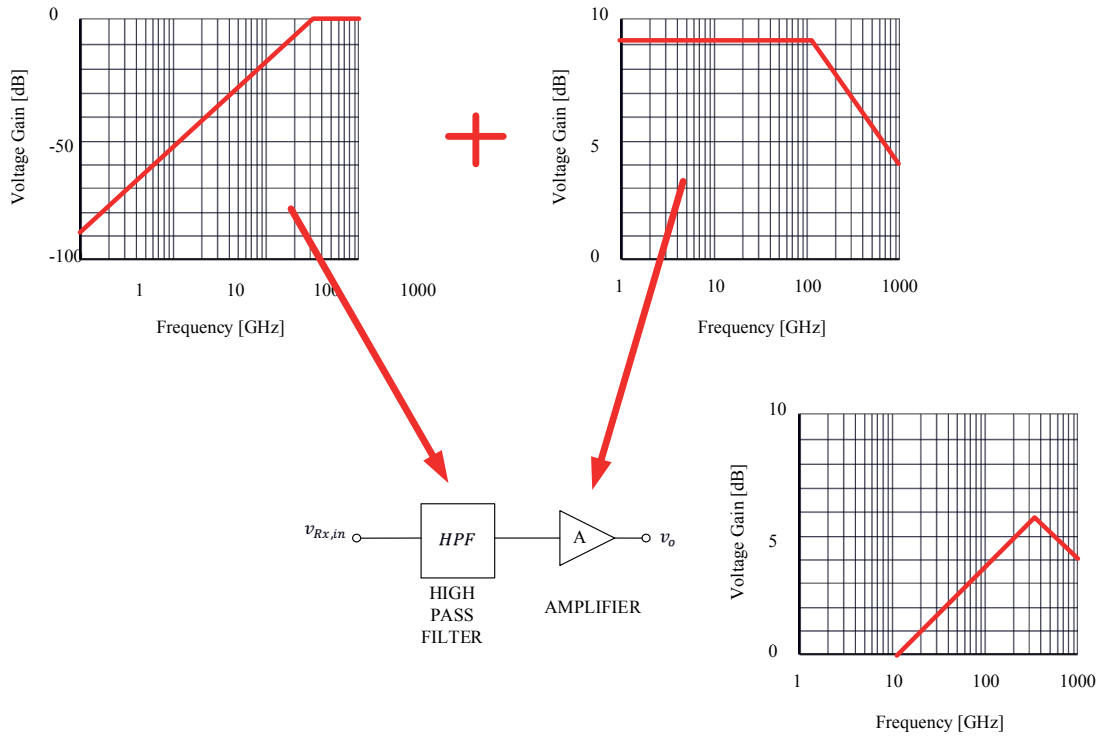


Figure 3-37 Equalizer Model Using a High Pass Filter in Series with an Amplifier

In order to better control the shape of curve for which the equalizer circuit is designed, the a series low pass filter is connected to the circuit to create or shape the signal needed by the equalizer.

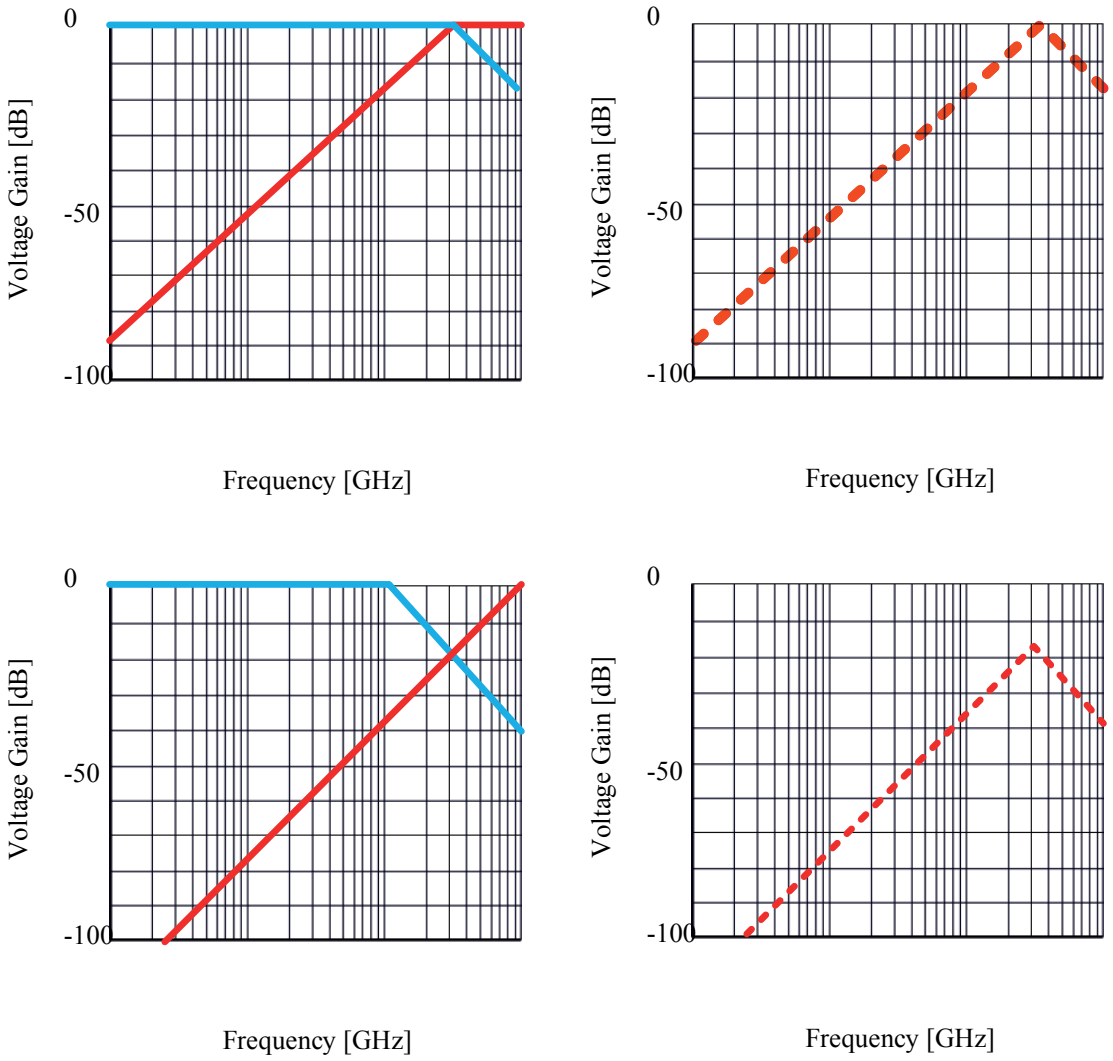


Figure 3-38 Bode Plot Representation of a Pulse Shape Signal using a Low Pass and a High Pass Filter Connected in Series

Figure 3-38 represents a bode plot of a low pass filter and a high pass filter—depicted on the left. The right bode plots represent the addition of the two frequency responses from the low pass and the high pass filters.

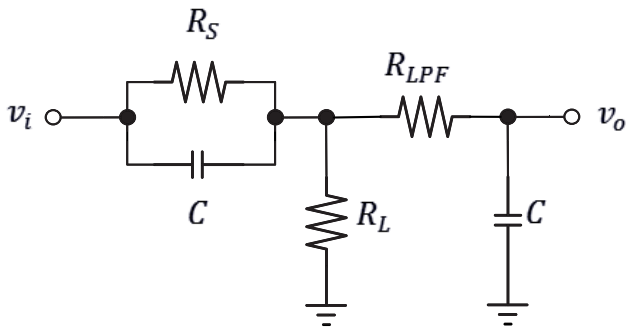


Figure 3-39 Passive Pulse Shape Filter

A pulse shape filter is a filter that shapes the signal to have the inverse curve of a channel wireline. This filter adds additional attenuation to the channel. The amplifier must be able to amplify the loss signal to get an overall voltage gain of at least zero decibels at Nyquist frequency.

Figure 3-40 shows the result of a passive pulse shape filter connected in series with the amplifier. Note that by changing the series resistance value of the high pass filter, the signal is attenuated at the lower frequencies but little attenuation is made at the frequencies close to the Nyquist frequency.

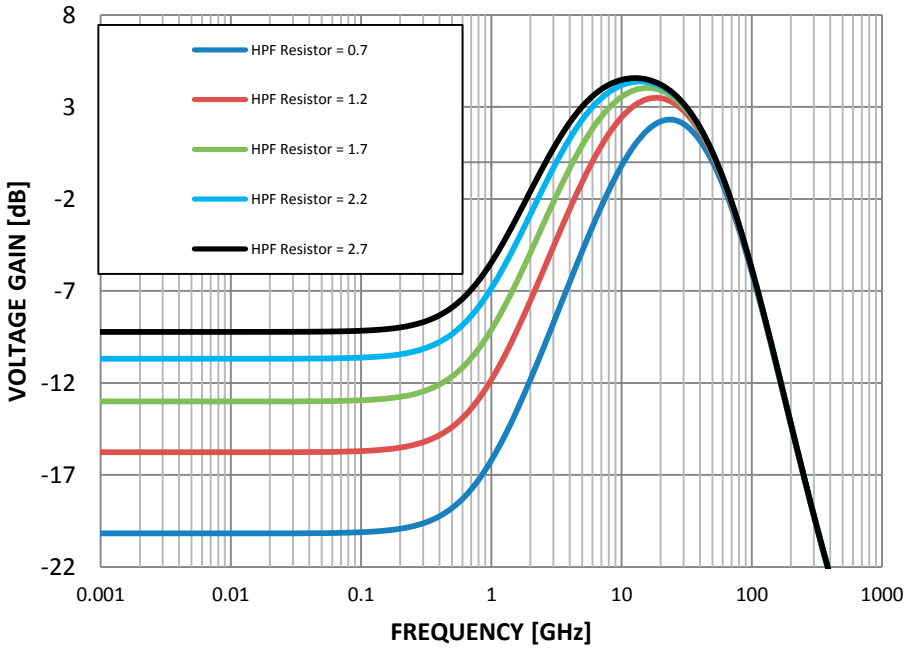


Figure 3-40 Variable Passive Pulse Shape Filter. HPF Resistor is Programmed or Varied to Add Attenuation to the Lower Frequency Range

The shape and amplification of the signal is arbitrary and depends highly on the channel response. The ability to program the pulse shape is important. The output of the pulse shape filter is sometimes called *passive peaking*.

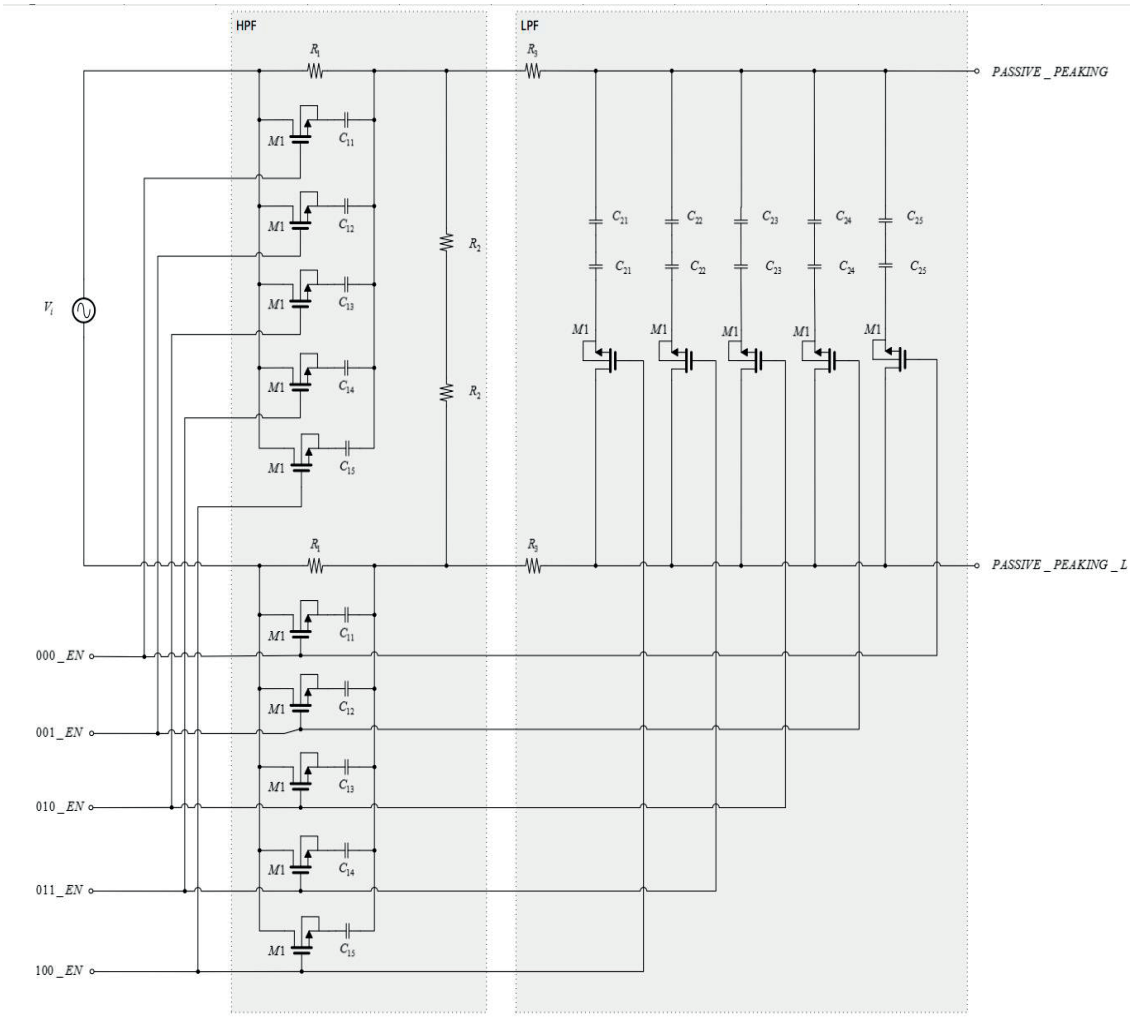


Figure 3-41 Programmable Differential Pulse Shape Filter

3.10 30 GHz Equalizer Circuit Elements

As mentioned in this thesis, there are two basic elements needed to create a 30 GHz front end equalizer design: (a) a programmable differential passive pulse shape filter, and (b) a programmable differential voltage gain amplifier (VGA).

The first element is responsible to create the shape or profile of the inverse loss created by the channel. The pulse shape filter is programmable so that it is capable to

compensate or equalize the loss created by various types and lengths of channel microwares. The pulse shape must be able to boost the signal at the Nyquist frequency. In this case, the passive filter shapes the signal with a boost at 30 GHz.

The second electronic circuit element of an equalizer is a high bandwidth VGA. The VGA cutoff frequency which is commonly refered as the frequency where the loss is -3 dB from the lowest frequency, does not have to be set exactly at 30 GHZ because when connected to the pulse shape filter, all the lower frequencies will be attenuated but tapered so that it creates the desired amplification at the Nyquist frequency. The amplification, must be such that it elevates the attenuated Nyquist frequency of 30 GHz to a voltage gain above zero decibels.

4 Results

4.1 High Pass Filter

To calculate the right series resistance (R_s), the series capacitance (C_s) and the load resistance (R_o) for the high pass filter design, the following calculations were performed,

$$\frac{v_o}{v_i} = \frac{R_o}{R_o + \frac{R_s}{\left(1 + \frac{s}{\omega_1}\right)}} \tag{4-1}$$

$$\frac{v_o}{v_i} = \frac{R_o\left(1 + \frac{s}{\omega_1}\right)}{1 + \frac{s}{\omega_1\left(\frac{R_o + R_s}{R_o}\right)}} \tag{4-2}$$

$$\omega_1 = \frac{1}{R_s C_s} \tag{4-3}$$

Table 4-1 High Pass Filter Calculated Values for Passive Filter Elements

SELECTED ZERO FREQUENCY FOR UPPER LIMIT [GHz]	SELECTED DC GAIN; LOWER LIMIT [dB]	SELECTED UPER GAIN @ THE POLE [dB]	CALCULATED RESISTANCE RO [Ω]	CALCULATED POLE FREQUENCY f1 [GHz]	CALCULATED Rs [Ω]	CALCULATED Cs [pF]	CALCULATED ω1 [Grads]	CALCULATED ωo [Grads]
5	-100	-3	0.00001	4.99407E-05	100118.653	31.83098862	6.283185307	31.41592654

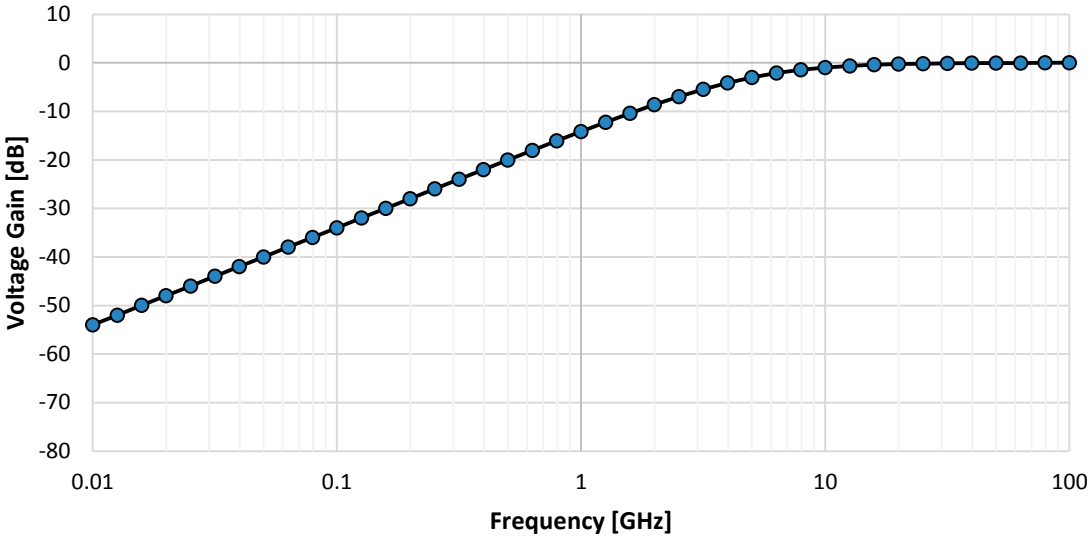


Figure 4-1 Frequency Response for High Pass Filter (HPF) Design

4.2 Low Pass Filter

To calculate the right series resistance (R_s), the load capacitance (C_o) for the low pass filter design, the following calculations were performed,

$$\frac{v_o}{v_i} = \frac{1}{1 + \frac{s}{\omega_3}} \tag{4-4}$$

$$\omega_3 = \frac{1}{R_s C_o} \tag{4-5}$$

Table 4-2 Low Pass Filter Calculated Values for Passive Filter Elements

SELECTED LOW PASS FREQUENCY [GHz]	SELECTED CAPACITOR [pF]	SELECTED CUTOFF FREQUENCY [dB]	CALCULATED ω [Grads]	CALCULATED R1 [Ω]
10	200	-3	62.83185307	0.079577472

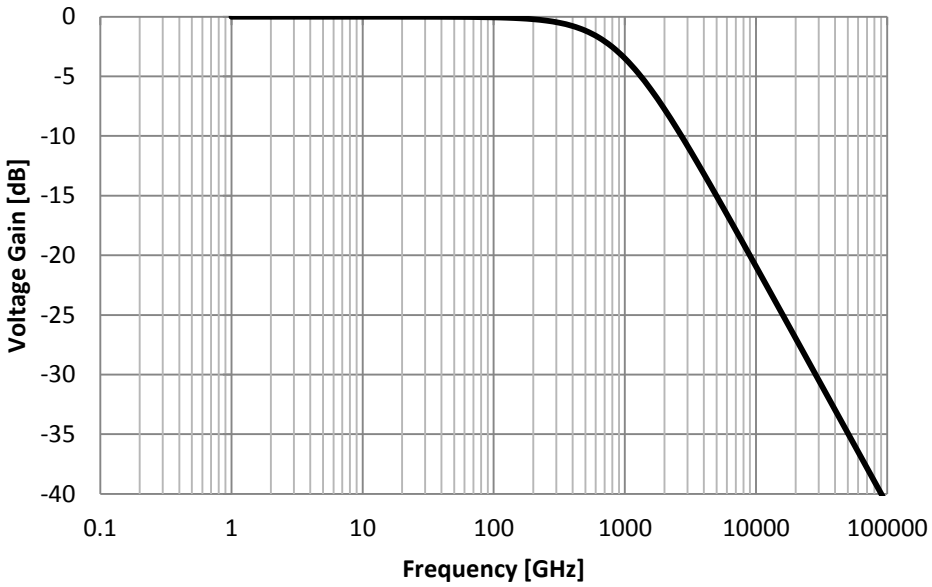


Figure 4-2 Frequency Response for Low Pass Filter (LPF) Design

4.3 Pulse Shape Filter

This section shows when the low pass filter and the high pass filter are connected together to form the pulse shape filter.

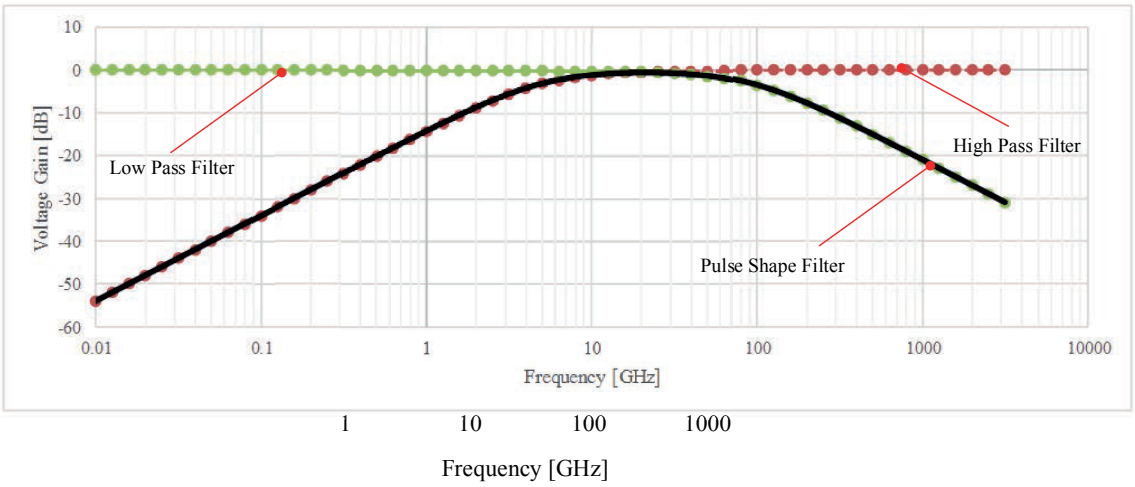


Figure 4-3 Frequency Response for Pulse Shape Filter (PSF) Design

4.4 30 GHz Equalizer, 28 nm Technology

This section shows the results of the 30 GHz programmable front end equalizer.

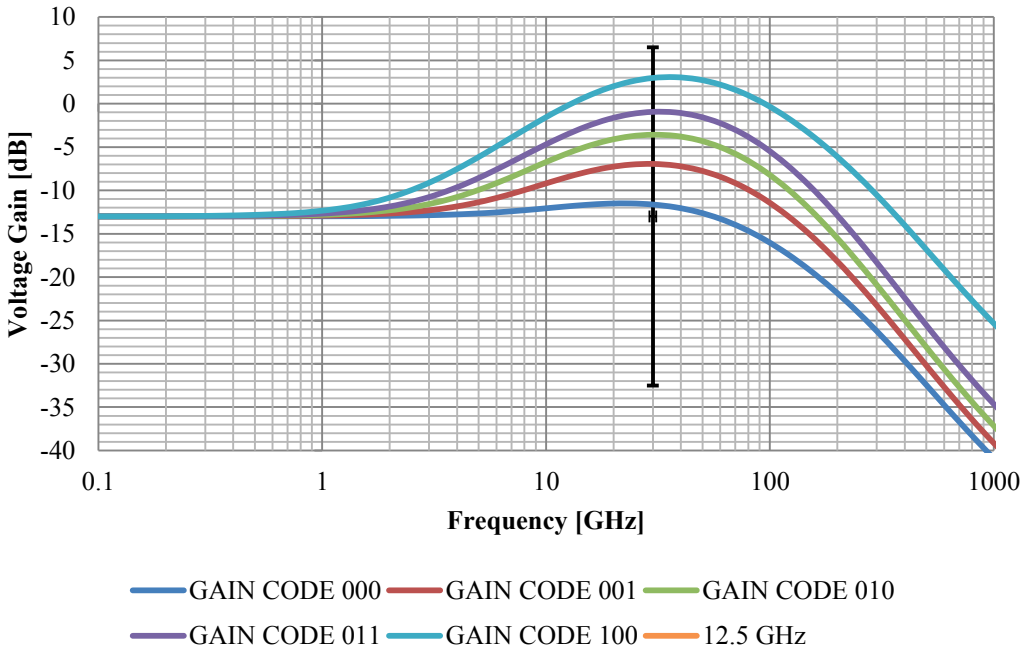


Figure 4-4 This Thesis Equalizer Voltage Gain Response—Logarithmic Frequency

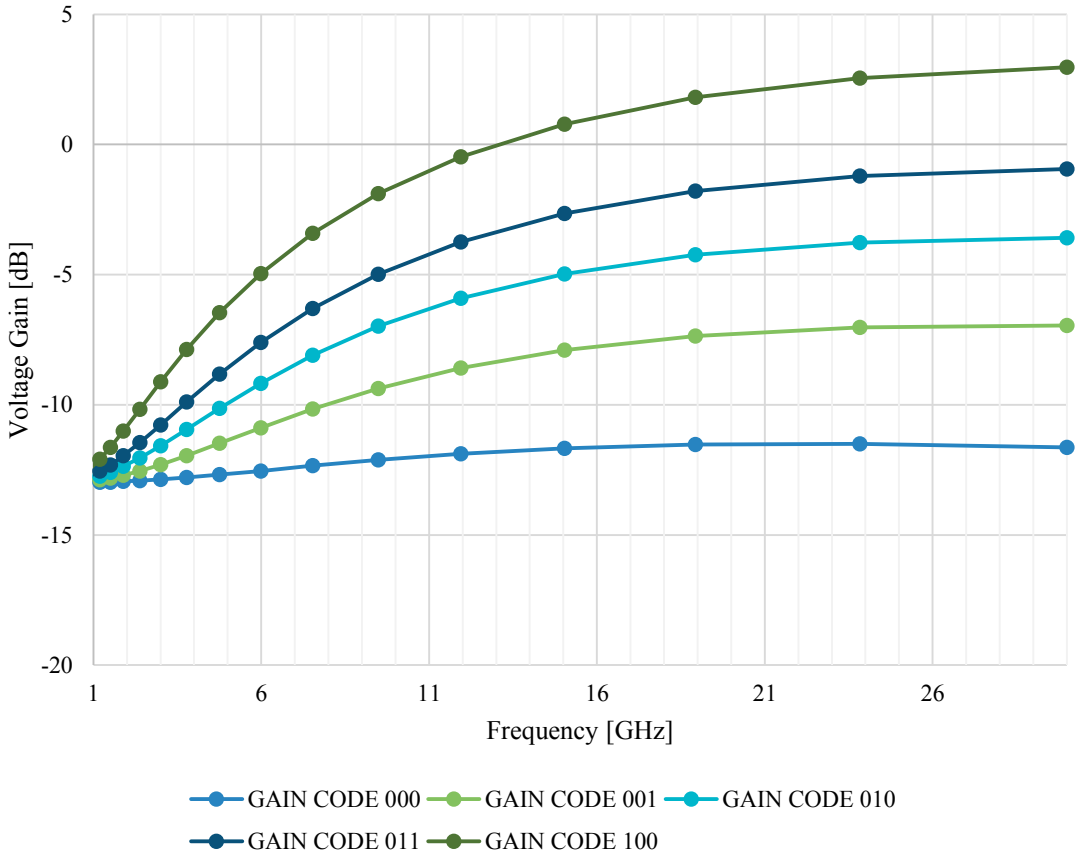


Figure 4-5 This Thesis Equalizer Voltage Gain Response—Linear Frequency

5 Conclusion

The motivation behind using USB 3.0 technology was based on two factors: Ease-of-use, and port expansion. Similarly, PCIe® is a technology that allows high speed point-to-point serial communication between two microcircuit devices. Both PCIe® and USB technologies grew from being the connection solution between PC peripherals or microcircuit devices to being the solution of network communications between a diverse selection of mobile and hardware products to minimize the amount of wire link connections and increase reliability. To date, the wired and wireless USB interfaces are the world's most popular answer to connectivity for PC, Mobile applications, and Consumer Electronics because of their low cost, fast implementation, and versatile data rate transmissions while PCIe® is a common transmission bus protocol between microcircuit devices. Both PCIe® and USB technologies are scalable and backwards compatible. Moreover, both technologies employ the 8b/10b data symbol coding per ANSI X3.230-1994 to increase the reliability of the transmitted signal.

Modeling an accurate transmission line in a CAD system is difficult because of the available different types of transmission lines which have different dimensional properties, manufacturing processes, material composition, and electrical parameters. One of the most important parameters reviewed in this thesis was the transmission line loss parameter. A simple CAD model approach was implemented to incorporate the transmission line on a circuit. Attenuation of the signal in transmission lines is dependent on the length of the transmission line, the transmission line interelement capacitance, and the transmitted signal frequency.

This thesis demonstrated a design that can be used when using the popular FR4 wireline which is predicted to support a 200 Gb/s transmission line if the transmission line is 25 cm-long and the transmitter has an output of 100 mV. It was demonstrated that the capacity of the channel is inversely proportional to the length of the channel. Point-to-point communication between two microcircuit devices benefit if the devices are as closed as possible and the transmission line or wireline is shielded from FR noise that may be induced into the wireline from other wirelines or from the external ambient. In addition, limiting the amount of vias between the devices decreases the effects of the interelement capacitance introduced by the via stubs.

A simple circuit model was proposed based on observations of measured and calculated behaviors of a microstrip wireline. The proposed simple model takes under consideration small 1 cm-long channel segments. The model can be connected to simulate single channel as well as differential channels.

This thesis explained the importance of deriving, measuring, and understanding the transit frequency of the transistor to better plan for any application that requires the use of an amplifier. This is due to the fact that the most critical device in an equalizer or amplifier design is the component that does the active amplification. In the case of this thesis, amplification is done using a common source NMOS amplifier. Knowing the transit frequency and current gain at various settings of the gate-source voltage to find the best efficient bias point.

A passive high pass filter connected to a low pass filter create a pulse shape filter that if connected in series with can be connected in series with an amplifier, the resulting

circuit becomes a simple equalizer. There are three basic elements of an equalizer of the type described in this thesis.

(1) A programmable differential pulse shaper; and

(2) A programmable differential voltage gain amplifier.

Further amplification on the signal can be made by applying an amplifier with impedance matching at the output of the equilizer.

6 References

[1] Global Industry Analyst, Inc. *USB 3.0 – A Global Strategic Business Report.* March 2013.

[2] USB Group. *USB 3.0 SuperSpeed Equalizer Design Guidelines.* June 10, 2011.

[3] USB Group, *Universal Serial Bus 3.1 Specification,* Rev 1.0, July 26, 2013.

[4] ISSCC, *2014 Digest of Technical Papers*, VOL. 57, ISSN 0193-6530, February, 2014.

[5] ISSCC, *2013 Digest of Technical Papers*, VOL. 56, ISSN 0193-6530, February, 2013.

[6] Kimura et al, *28Gb/s 560 mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision-Feedback Equalizer in 28 nm CMOS*. (Reference [4] Session 2.1).

[7] Won Jung and Razavi, *A 25 Gb/s 5.8 mW CMOS Equalizer*. (Reference [4] Session 2.4).

[8] Bai et al, *A 0.25pJ/b 0.7V 16Gb/s 3-Tap Decision-Feedback Equalizer in 65nm CMOS*. (Reference [4] Session 2.5).

[9] Mammei et al, *A Power-Scalable 7-Tap FIR Equalizer with Tunable Active Delay Line for 10-to-25Gb/s Multi-Mode Fiber EDC in 28 nm LP-CMOS*. (Reference [4] Session 8.3).

[10] Huang et al, *A 28Gb/s 1pJ/b Shared-Inductor Optical Receiver with 56% Chip-Area Reduction in 28nm CMOS*. (Reference [4] Session 8.4).

[11] Balan et al, *A 130mW 20Gb/s Half-Duplex Serial Link in 28nm CMOS*. (Reference [4] Session 26.1).

[12] Ierssel et al, *Signal Capacity of FR4 PCB for Chip-to-Chip Communication*. Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03. Vol.5, Pgg. V-85 - V-88.

[13] Gallager, *Information Theory & Reliable Communication*. Wiley, 1968.

[14] Razavi, *Fundamentals of Microelectronics*. 1st Ed. New Jersey: Wiley, 2006.

[15] Howe, *Microelectronics, An Integrated Approach*. Upper Saddle River, NJ: Prentice Hall, 1997. ISBN: 0135885183. As interpreted and presented by Alamo, *Microelectronics Devices and Circuits – Fall 2005, Lecture 23 – Frequency Response of Amplifiers (I): Common-Source Amplifier*. Massachusetts Institute of Technology, December 1, 2005

[16] Jepers, *The Gm/Id Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits*. New York: Springer, 2010.

[17] Rao, *Analog Front-End Design Using the Gm/Id Method for a Pulse-Based Plasma Impedance Probe System.* Thesis BSEE, Utah State University, 2010.