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Time-based, Low-power, Low-offset 5-bit 1 GS/s Flash ADC Design in 65nm CMOS Technology

Mehdi Nasrollahpour
San Jose State University

TIME-BASED, LOW-POWER, LOW-OFFSET 5-BIT 1 GS/s FLASH ADC DESIGN IN 65nm CMOS TECHNOLOGY

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Mehdi Nasrollahpour

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by

Mehdi Nasrollahpour

APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

SAN JOSÉ STATE UNIVERSITY

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Dr. Sotoudeh Hamedi-Hagh	Department of Electrical Engineering
Dr. Morris Jones	Department of Electrical Engineering
Dr. Robert H. Morelos-Zaragoza	Department of Electrical Engineering

ABSTRACT

TIME-BASED, LOW-POWER, LOW-OFFSET 5-BIT 1 GS/s FLASH ADC DESIGN IN 65nm CMOS TECHNOLOGY

By Mehdi Nasrollahpour

Low-power, medium resolution, high-speed analog-to-digital converters (ADCs) have always been important block which have abundant applications such as digital signal processors (DSP), imaging sensors, environmental and biomedical monitoring devices. This study presents a low power Flash ADC designed in nanometer complementary metal-oxide semiconductors (CMOS) technology. Time analysis on the output delay of the comparators helps to generate one more bit. The proposed technique reduced the power consumption and chip area substantially in comparison to the previous state-of-the-art work. The proposed ADC was developed in TSMC 65nm CMOS technology. The offset cancellation technique was embedded in the proposed comparator to decrement the static offset of the comparator. Moreover, one more bit was generated without using extra comparators. The proposed ADC achieved 4.1 bits ENOB at input Nyquist frequency. The simulated differential and integral non-linearity static tests were equal to +0.26/-0.17 and +0.22/-0.15, respectively. The ADC consumed 7.7 mW at 1 GHz sampling frequency, achieving 415 fJ/Convstep Figure of Merit (FoM).

DEDICATION

I would like to dedicate this thesis to my parents. My father who is my role model in the whole aspects of my life. He is the reason I continued my education to make him lofty and proud as he coveted, and my mother who always supports me with her everlasting love. My parents offered unwavering encouragement for the endeavors I have pursued. Their staunch supports, love, and inspiration have given me valor to attain this degree. They made my life be in debt to them.

I would also like to dedicate my works and achievements to my nephews, Parham and Amirpasha that they have always been missed. Love all of you to the moon and back.

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"Think for your lord's gratification, be intellectual and truthful - Ferdowsi"

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LIST OF ABBREVIATIONS

ADC – Analog-to-Digital Converter

CMOS – Complementary Metal Oxide Semiconductor

DAC – Digital-to-Analog Converter

DNL – Differential Non-linearity

ENOB – Effective Number of Bits

FoM – Figure of Merit

INL – Integral Non-linearity

LSB – Least Significant Bit

PVT – Process, Variation, and Temperature

SFDR – Spurious-Free Dynamic Range

SNDR – Signal-to-Noise Distortion Ratio

SNR – Signal-to-Noise Ratio

S&H – Sample-and-Hold

TG – Transmission Gate

UWB – Ultra-Wideband

PWM – Pulse Width Modulation

TDC – Time-to-Digital Converter

VCO – Voltage-Controlled Oscillator

SAR – Successive Approximation Register

LDO – Low Drop-Out

PLL – Phase-Locked-Loop

FFT – Fast Fourier Transform

CHAPTER ONE
Introduction

Analog-to-digital converters (ADCs) form the interface between the exterior world and digital circuitry. They convert true-to-life signals into digital bits in order to further digitally process and evaluate the signal. Flash ADCs have been a pertinent choice for several applications because they have a much lower latency and an instantaneous comparison of the signal with pre-assigned reference levels. The use of Flash ADC in renewable energy systems has been of great interest recently due to their ability to be operated within a stringent power usage limit and high resolution [1].

However, there are several other applications in which Flash ADCs are given priority, especially in the digital signal processing field and in ultra-wideband (UWB) transceiver architecture [2-4]. In recent years, there has been extensive research in the development of low power ADCs for bio-medical applications that have very high sensitivity [5]. One of the major reasons for the extensive research is that all of these applications work on a limited power supply; hence, power consumption is of the utmost priority. The ADC accounts for a sizeable portion of power consumption in any module; hence, a reduction in its power consumption is highly favorable while optimizing such mixed-signal-based application modules.

In this work, we describe the working, design and simulated results of a 5-bit 1 GS/s Flash ADC that is optimized for low power consumption, while also employing an offset cancellation technique in order to decrement the static offset of the comparator, which is a fully differential dynamic comparator [6]. The ADC described in this thesis has fairly

low power consumption when compared to the other state-of-the-art 5-bit ADCs [7-9]. The thermal code generated is digitally processed with a Verilog-A code that will be presented in the appendix.

The thesis is divided into the following sections: Chapter 2 describes the different time-based Flash ADC architectures and their functionality and Chapter 3 discusses the Flash ADC different design concerns and blocks. Chapter 4 accentuates the working and design calculations involved in the comparator, phase detector, bit generation idea, and the Flash ADC architecture circuit implementation. The fifth chapter focuses on the simulation results obtained from the same ADC and a concise comparison with other state-of-the-art work, which is presented in Chapter 6. The final chapter provides a conclusion for the proposed study.

CHAPTER TWO
Time-Based ADCs

There are several ADCs that do not work based on voltage quantizing. Instead, these architectures quantize the time, frequency, or current. This chapter will talk about various time-based Flash ADCs. Based on the power budget, resolution, and dynamic range, the right decision can be made for designing the ADC.

2.1 Slope and Integrating ADCs

Slope and integrating ADCs try to convert the analog signal to digital binary codes in the time domain. The basic block diagram is shown in Fig. 2.1. The analog signal will be sampled through the sample-and-hold (S&H) block and kept on the capacitor. Stored voltage on the capacitor will be discharged by the current source, I_{ref}. A ramp signal will be generated on the capacitor during this process. By starting the ramp signal, a triggered signal will be activated to enable the counter. Another triggered signal will be generated by reaching the zero voltage that disables the counter. The digital counter is directly proportional to the input signal [10]. This ADC does not have any complexity since the integral non-linearity (INL) will be defined by linearity of the ramp signal. Therefore, the differential non-linearity (DNL) does not depend on the component that will result in ADC monotonicity.

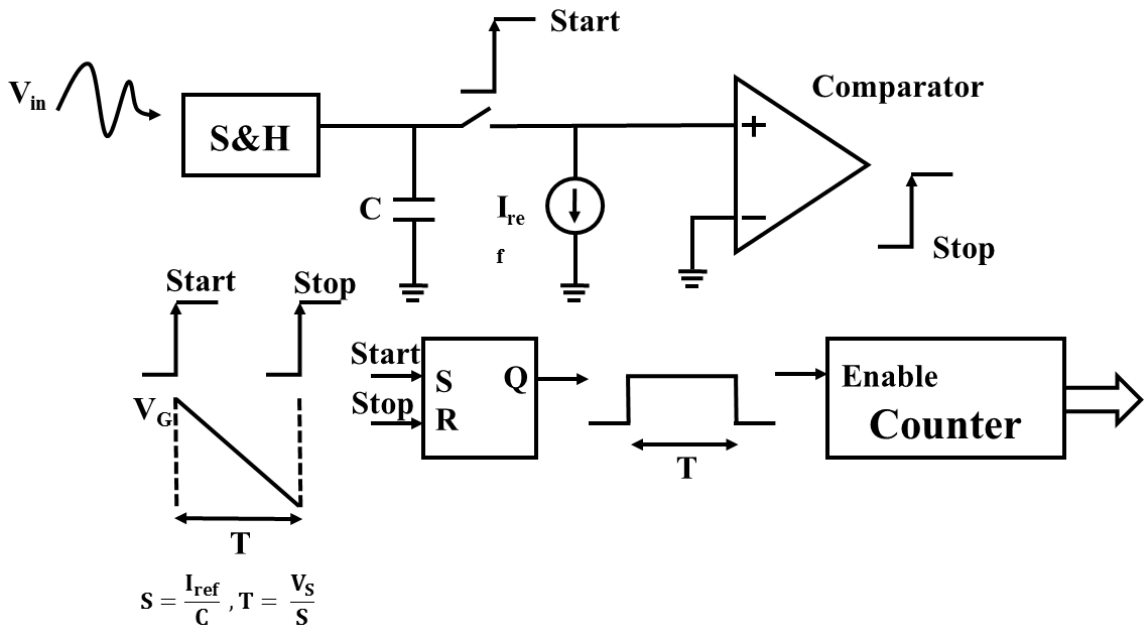

Fig. 2.1 Slope and integrating ADC schematic diagram

Obviously, the capacitor plays the most important role in the performance of this ADC, so the sampling frequency for this ADC architecture cannot be so high. High resolution is achievable by having the high-frequency clock. This high-frequency clock itself consumes large power. It is recommended that the counter be replaced with a sophisticated time-to-digital converter (TDC) to have high-speed slope-based ADCs [11,12].

2.2 PWM ADC

PWM time-based architecture developed and filed about 70 years ago [13]. The conceptual schematic of the PWM ADC is depicted in Fig. 2.2 [14].

First of all, the input signal is pulse modulated through the pulse width modulator; then it will be quantized through a counter. As we know, PWM is a process for transferring the data from the amplitude domain to the time domain. This block includes

a non-linear behavior that creates considerable distortion. It is proved in [15] that the non-linearities and distortions can be circumvented if the modulation frequency is eight times more than the input signal frequency. A complicated TDC can be substituted by the counter, like the slope-based ADCs.

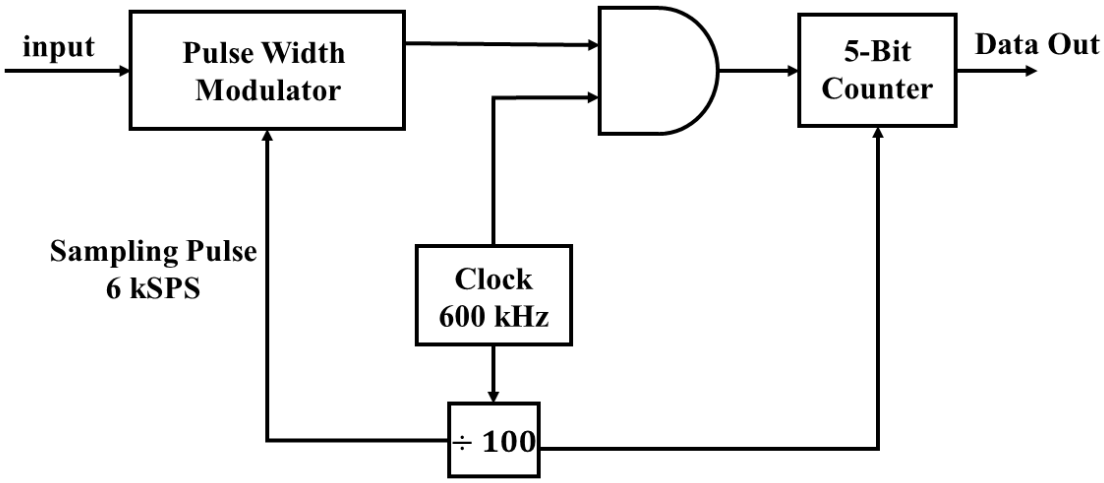

Fig. 2.2 PWM ADC schematic diagram

2.3 Level-Crossing or Asynchronous ADC

Level-crossing ADCs, also known as asynchronous ADCs, have some reference voltages and comparators [16-20]. When the input signal passes a specific value (threshold level), the ADC starts sampling and quantization during these instants. The signals and the basic schematic are depicted in Fig. 2.3 and Fig. 2.4 [21]. Since the input signal is time variable, the samples are different. At the instant the input voltage crosses the threshold value, the comparator makes the decision and generates output. The ADC is called asynchronous because the working performance does not depend on any reference clock. On the contrary, it depends on the input signal. A sign or block is required to

discern which comparator is working. Since the performance depends on the input signal, the power consumption severely changes due to the input activity. For example, if the input signal remains the same, there is no digital power consumption as no threshold value is passed. Like the Flash ADCs, comparator offset and mismatches play an important role in ADC performance. The quantization block works at a certain frequency, which is referred to as the sampling frequency. Time quantization should occur at Nyquist frequency to reconstruct the original signal from the discrete signal. Nyquist frequency requires that the sampling frequency should be at least two times the input signal. Higher input frequencies need a greater sampling frequency.

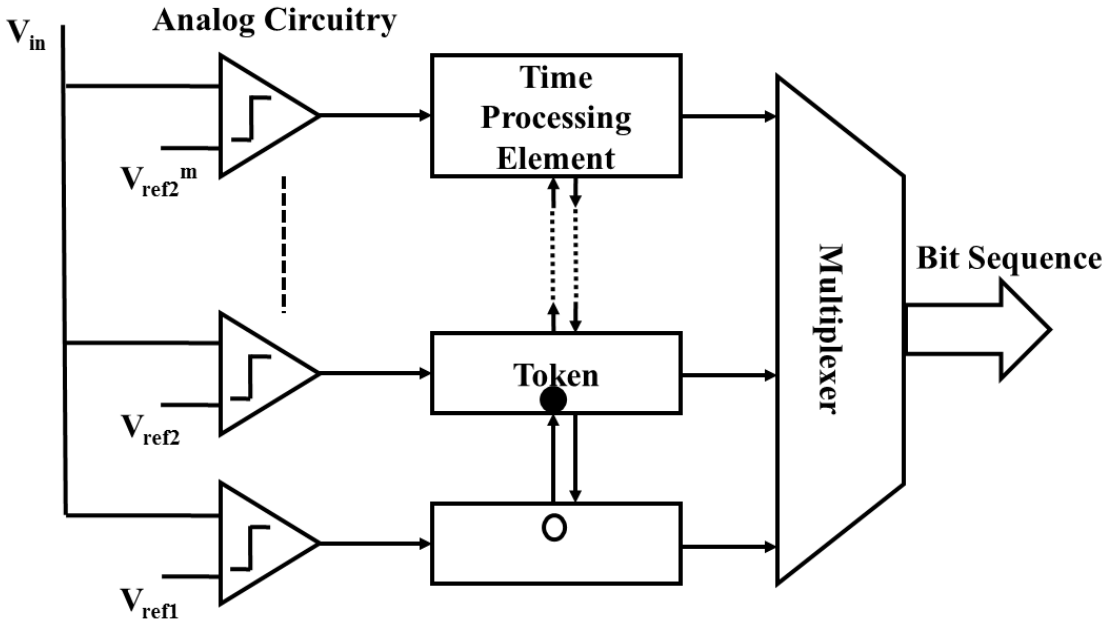

Fig. 2.3 Level-Crossing or asynchronous ADC schematic diagram

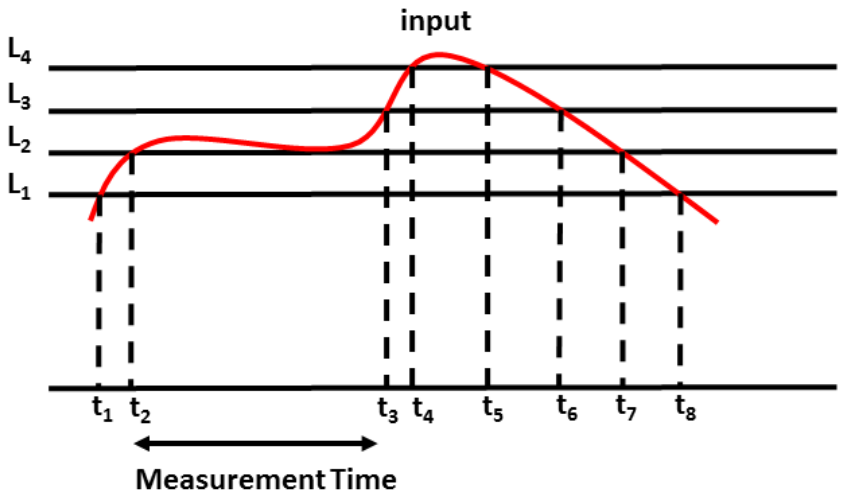

Fig. 2.4 Clocking in Level-Crossing ADC

2.4 Voltage Controlled Delay Cell-Based ADCs

The schematic diagram of the voltage-controlled delay cell based ADC is shown in Fig. 2.5. Obviously, a delay will be given to the input signal after the sampling, and the delay time will be digitized by a TDC. The start signal will go through the voltage-controlled delay cell which is controlled by the input voltage. The TDC output depends on the input signal. Designing a delay cell which can linearly modulate the input signal in a large dynamic range mandates a challengeable design.

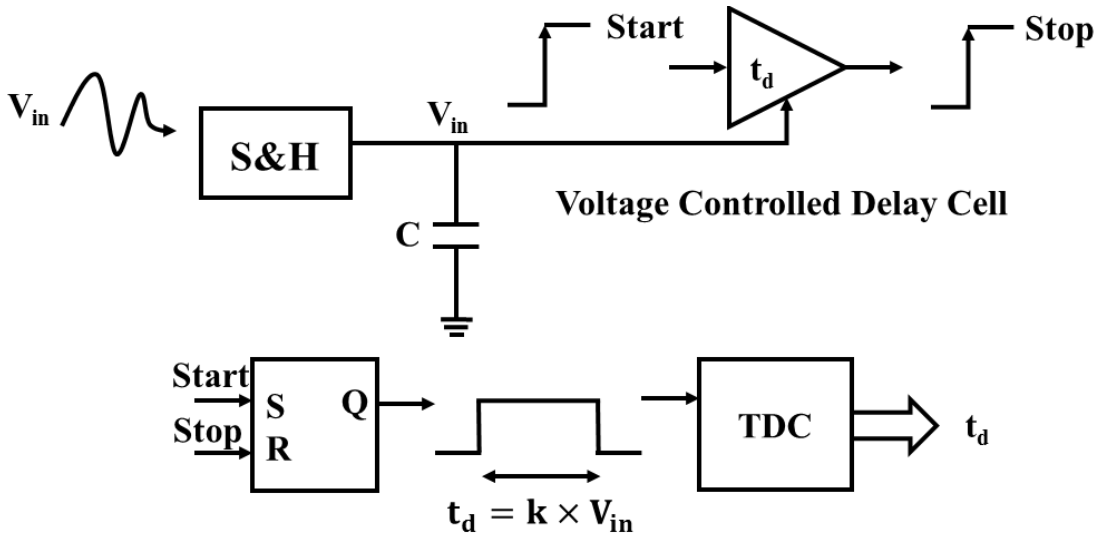

Fig. 2.5 Voltage-controlled delay cell based ADCs schematic diagram

2.5 Voltage to Frequency Converter Based ADC

Frequency can be interpreted by the phase and the phase is another definition for the time. In this ADC, the input signal is going to be converted to the frequency (phase); then the frequency (phase) can be digitized by a frequency (phase) to digital converter.

In this ADC type, the input analog signal should be converted to the frequency (phase), which is exactly the definition of the voltage-controlled oscillators (VCOs) [22,23]. The VCO-based ADC schematic is depicted in Fig. 2.6. As is obvious in Fig. 2.6, the small period of time between start and stop signals is available for quantizing the frequency through the counter. The mapping table which usually shows the VCO characteristics is exploited for processing the counter output. The ADC resolution can be determined by:

$$\text{Resolution} = \log_2\left(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}}\right) \quad (2.1)$$

Where f_{sample} is the inverse of time between the start and stop signal, f_{max} is the maximum VCO frequency and f_{min} is the minimum VCO generated frequency.

As we know, the ring oscillator has the maximum tuning range between the other VCOs. It means it can be used as the VCO in this ADC type to have the maximum resolution. The speed can be increased by using the multi-phase VCOs. The input voltage is converting to the frequency domain through the VCO and the counter counts the rising and falling edges. Assuming N stages ring oscillator, the resolution can be calculated by:

$$\text{Resolution} = \log_2\left[\left(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}}\right) \times 2N\right] \quad (2.2)$$

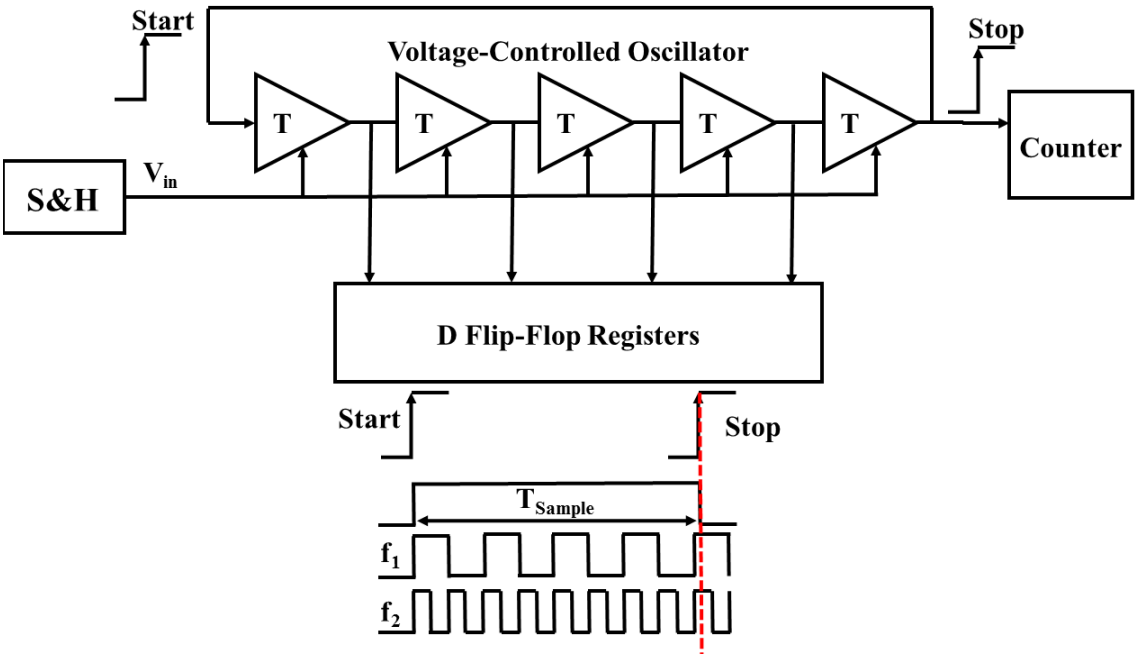

Fig. 2.6 Voltage-to-frequency converter based ADC schematic diagram

Jitter, linearity, process and temperature variations are some issues which make designers give careful consideration to this architecture design. One of the advantages

which this circuit has, is that the voltage-to-frequency converter and the quantizer are simultaneously happening in VCO. Since the phase of the output is a quantity which depends on the input voltage, VCO can be served as the first order noise shaping constructor [24-26].

As mentioned above, the jitter and the non-linearity of the input and output are suffering the VCOs. VCO non-linearity can be improved by applying a feedback which acts like a 2^{nd} order $\sum\Delta$ ADC as represented in Fig. 2.7. There have been several state-of-the-art published works with the same idea [25-27].

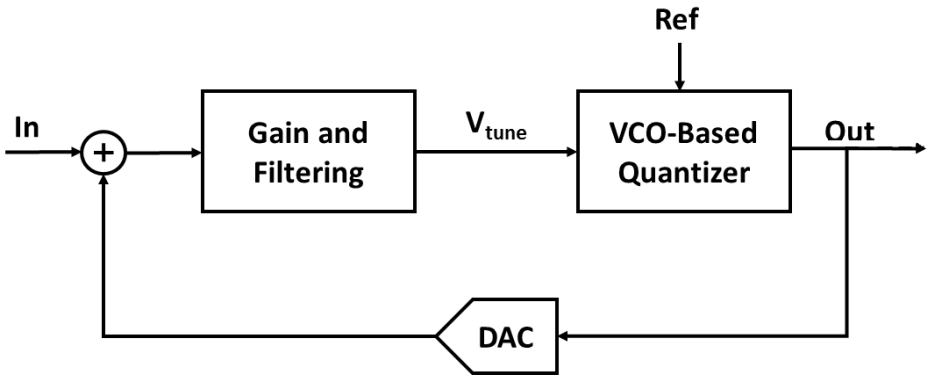

Fig. 2.7 Non-linearity improvement with feedback loop

CHAPTER THREE
Flash ADC Background

Fig. 3.1 depicts the schematic block diagram of the conventional Flash ADC architecture. Flash ADC usually consists of a comparator, resistor ladder, and logic encoder [28]. The critical component of any A/D converter is the comparator circuit. The characteristics and performance of the comparator determine the overall performance of the ADC. The different parts of the conventional Flash ADC will be explained in the following subsections.

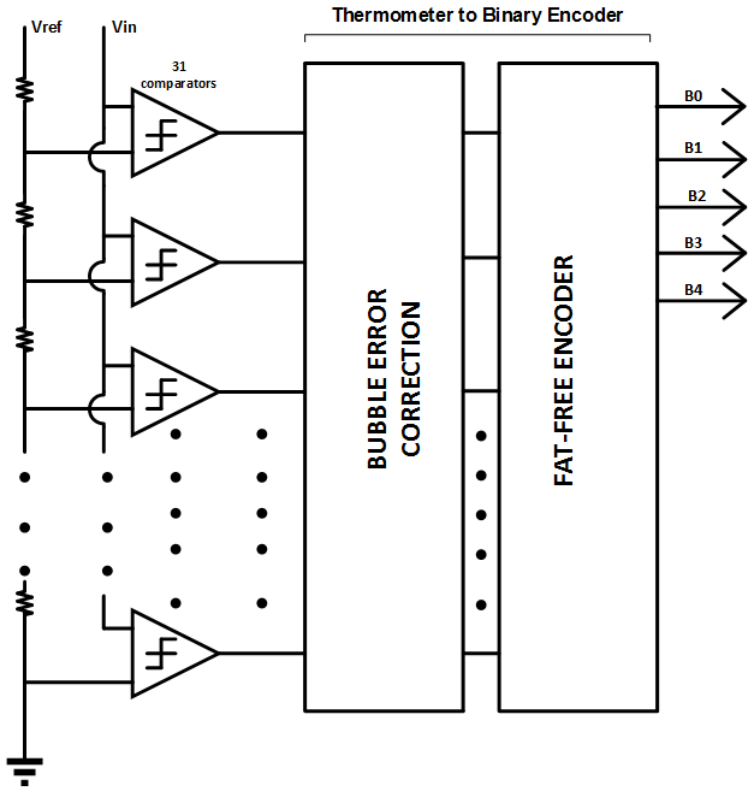

Fig. 3.1 Conventional Flash ADC architecture

3.1 Comparator

The major trade-off in designing a comparator is between the offset voltage and the power consumption of the comparator. The static power consumption of a comparator can be drastically reduced by dynamic topology implementation [29]. This also would mean that positive feedback will be provided by means of a latch, thereby speeding up the decision-making process. To ensure that the offset of a comparator remains low, larger input transistors should be used and ensure that the amplification phase of the comparator provides large enough differential voltage to subside the offset of the cross-coupled latch stage. In order to find a trade-off between offset and power consumption, the comparator circuit used here comprises of a cascaded amplifying stage along with a usual regenerative latch stage [30].

The comparators mainly compare the two instantaneous differential input voltages and will return the result in the form of high or low voltages based on the difference sign. There are three different architectures for building the comparators [31]:

1. Amplifier with the high gain, differential input, and single ended output.
2. Latched comparators which are implemented in two different ways: latch only comparator, and high sensitivity latch with low gain preamplifier.
3. Sampled data comparators with track and hold input circuit, in which the offset can be nullified.

The first kind of comparator needs to have a large gain which is not accessible in MOSFET technologies. Therefore, many stages should be used to satisfy the required gain of the comparator. This method unveils the tradeoff between bandwidth and offset.

The comparator gain does not need to be linear since it should pull the output voltage up or down rapidly. Hence, a back-to-back inverter which forms a latch can be used for regeneration by forming a positive feedback loop. The Latch small signal model shows that the latch can be modeled by the amalgamation of single-pole amplifier and positive feedback. The latch can compensate the amplifier gain since the latch is three times faster than the amplifier. However, the latch has a fairly high input offset voltage, as high as 100 mV. Using the preamplifier along with the latch can resolve this issue [32]. The gain of the preamplifier will compromise the comparator speed and input referred offset of latch.

3.2 Offset Consideration

A major hurdle while designing Flash ADC is the kickback noise and the effect it has on the resistive ladder and offset voltage. These can often lead to a shift in the reference level, resulting in an erroneous decision. Some procedures for implementing the resistor ladder have been established to prevent these errors [33,34].

Offset in amplifier-based comparators can be canceled by using a capacitor in series with cascaded amplifiers. The capacitor can be used either in the input of the amplifiers or the output. Output offset can be nullified by using the recommended switching circuits, as shown in Fig. 3.2 [30]. Output series offset cancellation can almost cancel the offset, and there is no need for closed loop stability. Nonetheless, the gain for each amplifier stage should be small, and the utilized offset cancellation capacitor can degrade the overall performance of the circuit.

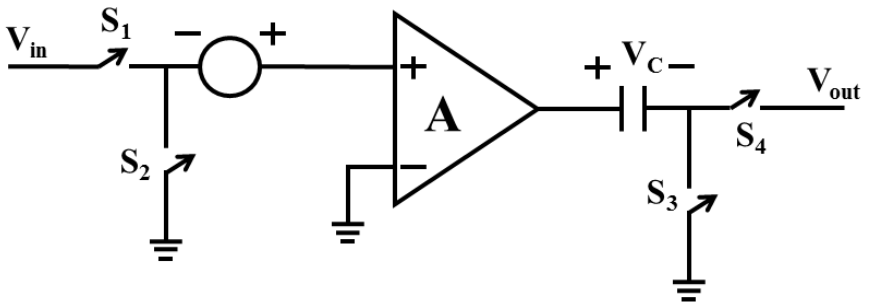

Fig. 3.2 Output series offset cancellation

Input offset cancellation circuit can be built like Fig. 3.3 [35]. The feedback loop should provide stability conditions due to the feedback loop around the amplifier. A C-array can be used to store the offset in the applications such as C-array successive approximation register (SAR) ADCs [36]. Input offset cancellation cannot completely cancel the offset. In the same manner, the capacitor can reduce the overall performance.

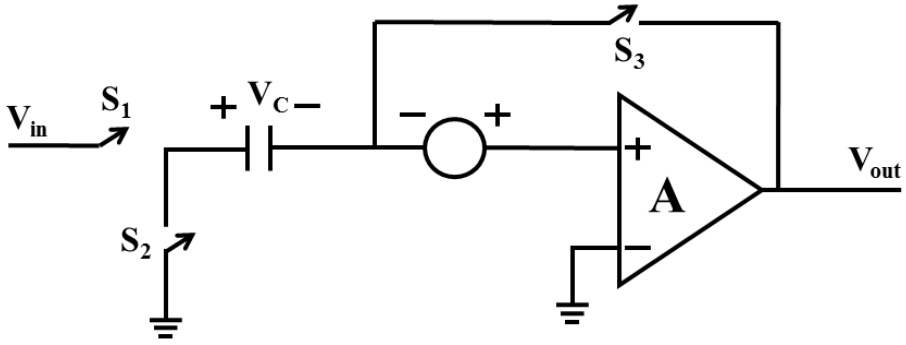

Fig. 3.3 Input offset cancellation

The offset voltage of latched comparators can be omitted with the auto-zeroing technique. The proposed technique is shown in Fig. 3.4 [37]. During the phase S_1, the amplifier brings the offset to the input by the unity gain. The capacitor C+ is charged to the offset value and the input voltage was previously applied to the capacitor's left plate

before S_1. The offset will be stored on the capacitor and will be canceled in the differential performance of the amplifier during S_3.

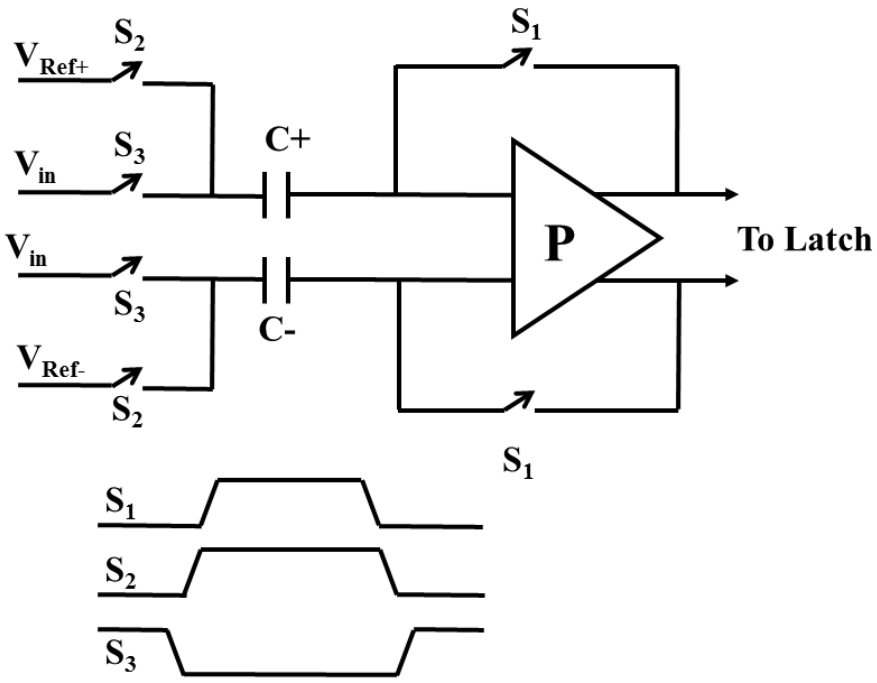

Fig. 3.4 Auto-zeroing technique offset cancellation

3.3 Encoder

As mentioned in the previous sections, the comparator outputs are high or low which the values more than the reference voltage are high and the values less than the reference voltage are low. To some extent, the generated outputs act like the thermometer as shown in Fig. 3.5.

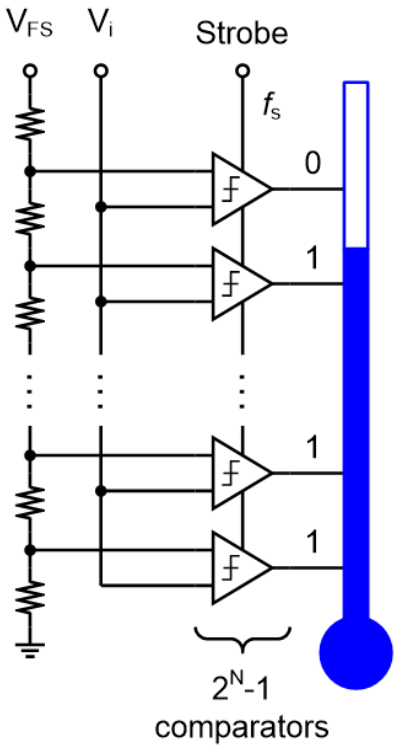

Fig. 3.5 Output thermometer code

Therefore, the necessity of the blocks at the output might arise here to convert the thermal code of the comparator array to the binary codes. Each thermometer code converts to one of the N codes before converting into binary. Two challenges will appear in the thermometer to binary encoder design: Speed and error handling capability [38, 39].

3.4 Errors in FLASH ADC

The errors in Flash ADC are divided into two categories; metastability and bubble errors. Metastability happens when the comparator cannot decide and compare the inputs, so the output is neither high nor low. The comparator output is indistinguishable, and the encoder interprets the thermal code as either high or low.

Based on Flash ADC performance and Fig. 3.5, the thermal codes should act like a thermometer. Therefore, a wrong decision can be made by the comparator corruption called “bubble errors”. There are three sources which can result in bubble errors:

1. Comparator offset voltage larger than half of the least significant bit (LSB) that might change zero crossing points for the comparators which are next to each other.
2. Error in comparators sampling time.
3. Propagation delay variations which happen in high input frequencies [40].

Bubbles can be suppressed easily. By using three-input NAND instead of two-input NAND, one bubble can be suppressed as depicted in Fig. 3.6 [41]. In the same manner, two bubbles can be suppressed by four-input NAND.

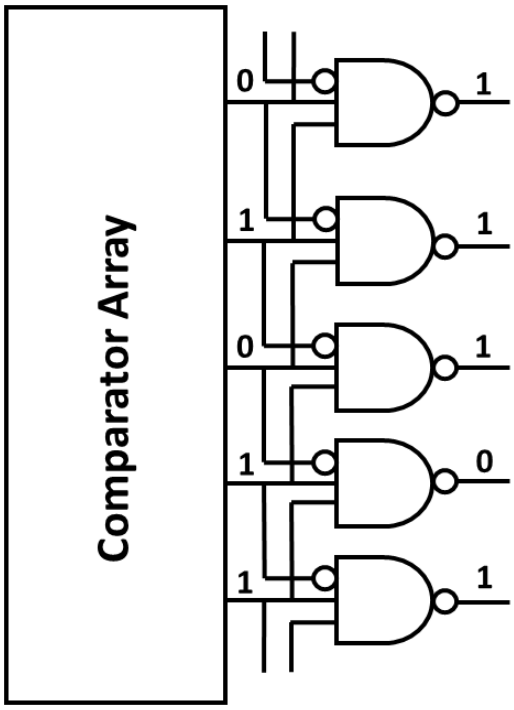

Fig. 3.6 Bubble error correction

Gray coding is another efficient way to overcome the errors. The gray coding is summarized in the following table. Each G_i is affected by only one T_i that means the contribution of each input is less and consequently less errors. Metastability state probabilities are lower with Gray coding and this encoder provides more time for the generation by using pipelining [42].

Table 1. Thermometer to Binary Gray Encoder

Thermometer Code							Gray			Binary		
T_1	**T_2**	**T_3**	**T_4**	**T_5**	**T_6**	**T_7**	**G_3**	**G_2**	**G_1**	**B_3**	**B_2**	**B_1**
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	1	0	0	1
1	1	0	0	0	0	0	0	1	1	0	1	0
1	1	1	0	0	0	0	0	1	0	0	1	1
1	1	1	1	0	0	0	1	1	0	1	0	0
1	1	1	1	1	0	0	1	1	1	1	0	1
1	1	1	1	1	1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1	0	0	1	1	1

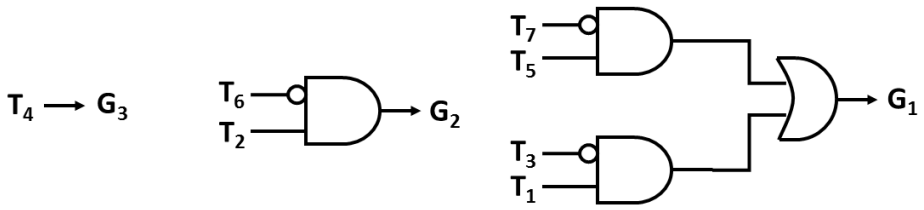

Fig. 3.7 Bubble error correction with Gray coding

3.5 Resistor Ladder

The voltage divider is the first section of Flash ADCs to generate the different level of the references. The common voltage divider is based on the equal resistors which are connected in series to provide equal voltage levels as the reference voltages to be compared to the input voltage. The important parameters are power consumption and the susceptibility to the noise. If the voltage divider uses small resistors, power consumption will increase, while the small resistors will suppress the noise injection. Feeding the input signal to the resistor ladder is the major source for the noise injection. The procedure for injecting the noise through the input signal is depicted in Fig. 3.8 [43].

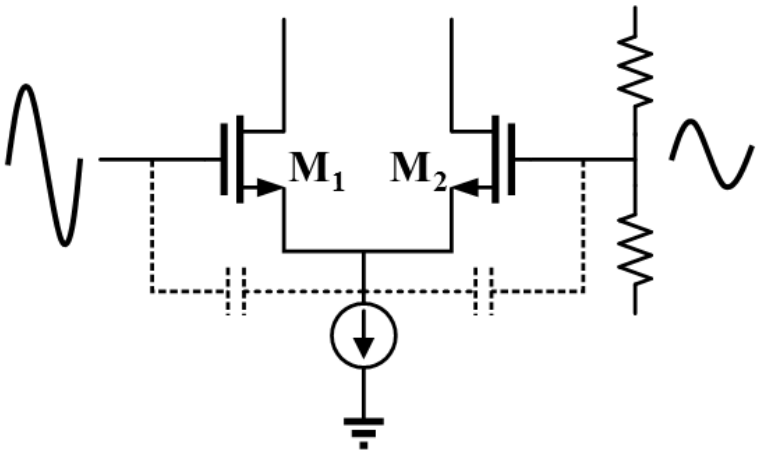

Fig. 3.8 Noise injection to the resistor ladder

As the resistor at the input of the preamplifier increase, the noise injected to the ladder is higher. It is obvious that the worst case will happen in the middle of the ladder. In practical circuits and fabrication, it should be noted to minimize the wiring from the ladder to the preamplifier. These sources can degrade the voltage divider performance.

The voltage divider is mainly consisting of the resistors, so the thermal noise contribution regarding the resistor ladder should be considered. Resistor thermal noise can be calculated as follows [44]:

$$v_n = \sqrt{4kTR\Delta f} \tag{3.1}$$

Where k is constant, T is the temperature and R is the resistor. Since the resistor value is small in the voltage divider, the thermal noise contribution is negligible.

There are different structures for Flash ADC ladders using capacitors, resistors, and the combination of them which are presented in [45-47]. Besides, a low drop-out (LDO) voltage regulator can be used to make the resistor ladder stable [48, 49].

CHAPTER FOUR
Circuit Implementation

The description of the proposed Flash ADC design is divided into four different sections. First, the novel idea which is used for extra bit generation is explained. Next section describes the comparator circuitry design, and the required features. The phase detector circuit implementation is then presented. Finally, the last section will describe the overall circuit diagram and integration of all the blocks.

4.1 Proposed Extra Bit Generation Idea

Flash ADC requires 2^N-1 comparators to quantize the input voltage. Therefore, it is evident that one more bit data conversion rate will cost eight times more power consumption [50]. Generation of one more bit for high-resolution Flash ADCs is challenging. The main idea which will be explained thoroughly in the following paragraphs is depicted in Fig. 4.1. As shown in Fig. 4.1, a TDC can be used instead of the huge number of extra comparators to generate more bits.

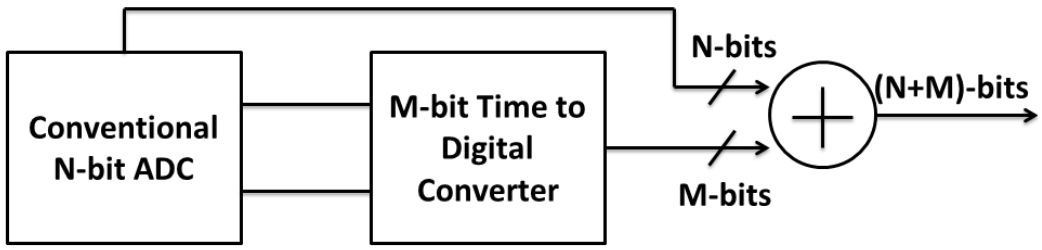

Fig. 4.1 Proposed idea block diagram

A Flash ADC consists of the resistor ladder, comparator, and encoding logic. The comparator plays the most significant role in the decision-making process. The proposed

idea is achieved from the fact that each comparator used in Flash ADC needs a certain time to reach the final value which can be defined as follows [51,52]:

$$t = \tau \times \mathrm{Ln}^{\frac{V_{in(diff)}}{A_{pre}V_O}} \tag{4.1}$$

Where τ, A_{pre}, $V_{in(diff)}$, and V_O are latch time constant, preamplifier gain, input differential voltage, and output voltage, respectively. It is evident from (4.1), the time needed for making the decision extremely depends on the input differential voltage between the input analog signal and the reference voltage generated by the resistor ladder, preamplifier gain, and the latch time constant. When the input difference voltage is smaller, the comparator output voltage can compare the inputs more slowly; hence, more time is required for the final decision to be reached. This time can be a good opportunity to do more comparisons. The conceptual schematic of proposed idea is shown in Fig. 4.2.

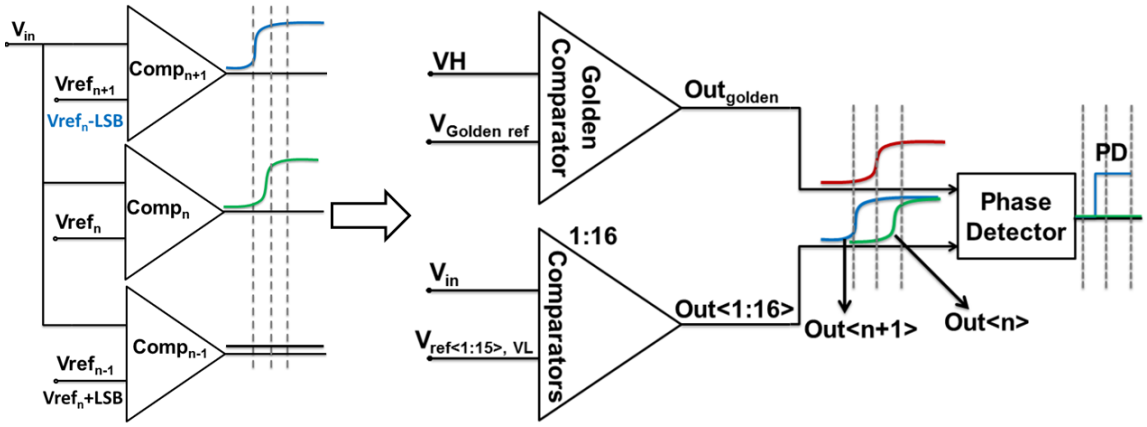

Fig. 4.2 Proposed idea concept

With regards to (4.1), the delay is at the maximum point for the closest comparator to the reference voltage, which is mainly contributing to the comparison. Therefore, a comparator can be utilized as reference, called the golden comparator. It will carry out the comparator's output comparison with the golden reference through the phase detector to perceive the anticipated comparison edge. Hence, the higher half-LSB and lower LSB can be distinguished by time analysis, as depicted in Fig. 4.3.

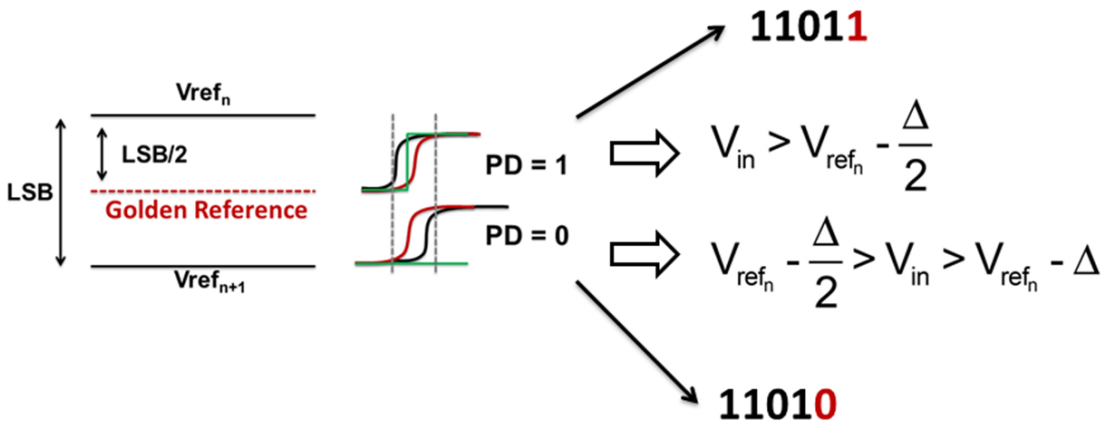

Fig. 4.3 Extra generated bit adding

In effect, each LSB distance is divided by two which means the input analog voltage could be converted by half-LSB, which is the new resolution. The proposed ADC could generate one more bit by using the only $2^{N-1}+1$ comparators which is less than the conventional method that we traditionally had used 2^N-1 comparators. It is worth mentioning that one more extra comparator has been used for the last edge detection.

The proposed idea works based on the comparator delay and it will be saturated after a certain input voltage difference, as demonstrated in Fig. 4.4.

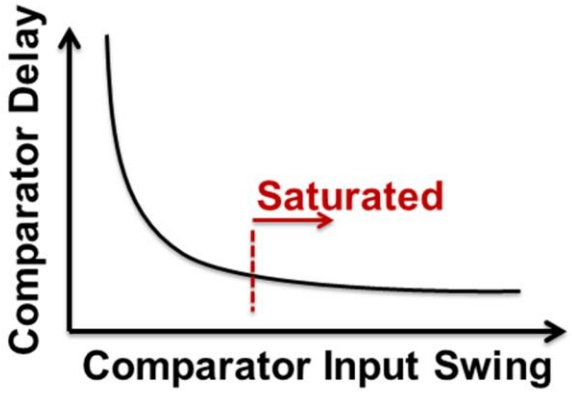

Fig. 4.4 Comparator delay characteristics

4.2 Comparator Circuit Implementation

A two-stage fully differential comparator has been designed in this thesis. Clocked regenerative comparators are suitable for high-speed Flash and SAR ADCs. Proposed comparator internal circuitry is shown in Fig. 4.5. Input voltage appears on the left plate of C_s and the common mode voltage will be applied to another plate when the clock is low. Consequently, V_{ref} and $V_{cm}\neg V_{in}+V_{ref}$ are applied to the left and right plates when the clock is high, respectively. It is worth mentioning that the comparator has been chosen to be differential since the proposed idea and time analysis are so sensitive to process, variation, and temperature (PVT).

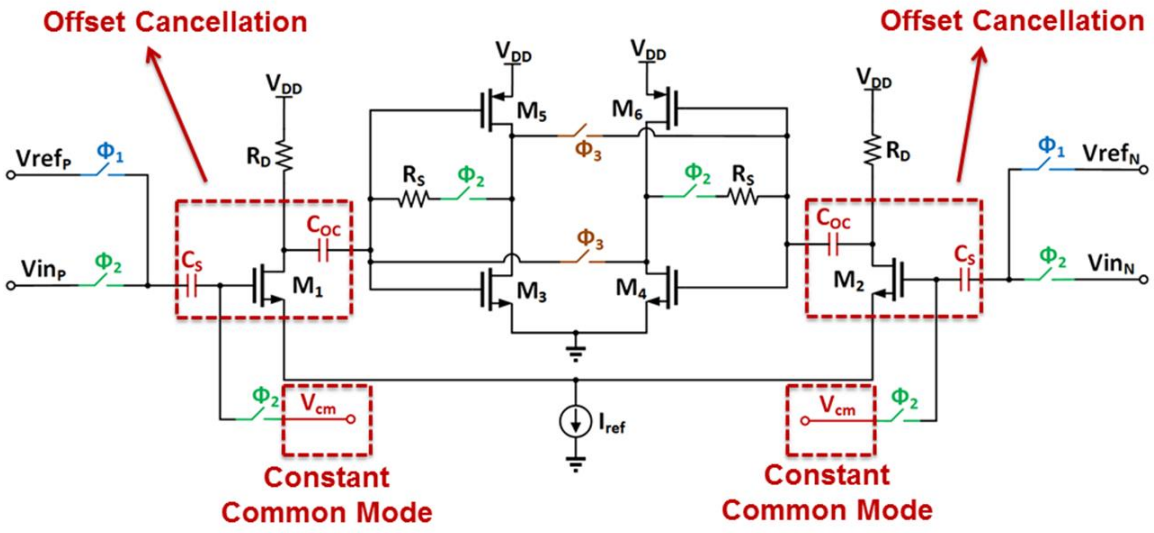

Fig. 4.5 Proposed comparator used in the Flash ADC

The proposed idea depends on the time analysis and the output delay of the comparator. The proposed comparator delay consists of the preamplifier and latch delay. Latch delay can be written as [53]:

$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta V_{out}}{\Delta V_{in}}\right) \tag{4.2}$$

Where $g_{m,eff}$, ΔV_{out}, C_L, and ΔV_{in} are defined as back to back effective transconductance, output differential voltage, load capacitor, and differential input voltage, respectively. The differential preamplifier output voltage can be calculated as:

$$A_{pre} = \frac{g_m \times R_D}{1+\frac{j\omega}{\omega_0}} \tag{4.3}$$

$$\Delta V_{o,pre} = 2R_D\omega_0 \left(\frac{I_{D,1}}{V_{OD,1}} + \frac{I_{D,2}}{V_{OD,2}}\right) e^{-\omega_0 t_{pre}} \tag{4.4}$$

Where R_D is the differential pair output resistor, ω_0 is the 3dB-bandwidth of the preamplifier, $I_{D,i}$ and $V_{OD,i}$ are the i-th transistor biasing current and overdrive voltage. Based on the (4.4) and (4.2), the total propagation delay for the two-stage comparator is:

$$t_p = t_{latch} + t_{pre} \tag{4.5}$$

$$t_p = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\Delta Vout}{\Delta Vo,diff}\right) + \ln\left(\frac{2\, R_D\, \omega_0}{\Delta Vo,diff} \times \frac{V_{OD,1}\, I_{D,2} + V_{OD,2}\, I_{D,1}}{V_{OD,2}\, V_{OD,1}}\right)^{\frac{1}{\omega_0}} \tag{4.6}$$

Equation (4.6) unveils the effects of different parameters on the propagation delay. The propagation delay of the comparator is inversely proportional to input common mode voltage. It is obvious by decreasing the common-mode voltage, the propagation delay will be increased. The proposed extra bit generation relies on the time analysis of the comparators output delay. Therefore, keeping the common mode voltage constant, is the main challenge which is considered into comparator design through the ϕ_2 switch when the clock is low.

The comparator delay with 1 mV voltage difference with respect to the reference voltage is simulated and the measured delay is 115 ps which shows that the comparator can work properly to 4.5 GHz. However, because of the time analysis on the comparator outputs, sampling frequency should not be high to provide enough time.

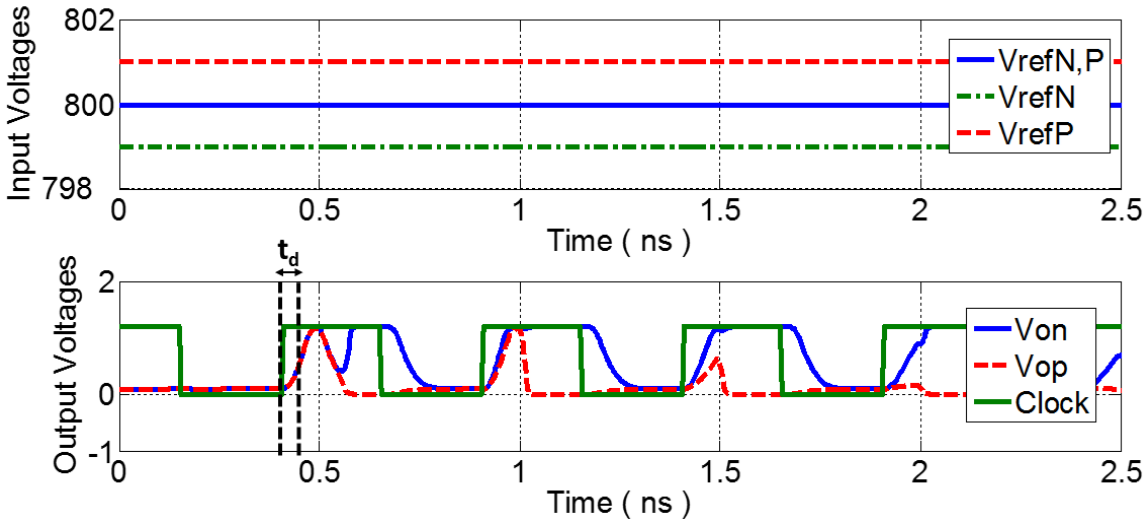

Fig. 4.6 Comparator delay

Comparators consume the most part of the total circuit power consumption. Comparator average power consumption at the worst case is 856 µW. The worst comparator delay happens while the input voltage difference is minimum. As shown in Fig. 4.7, the current drawn from the power supply is more while the latch is in regeneration state.

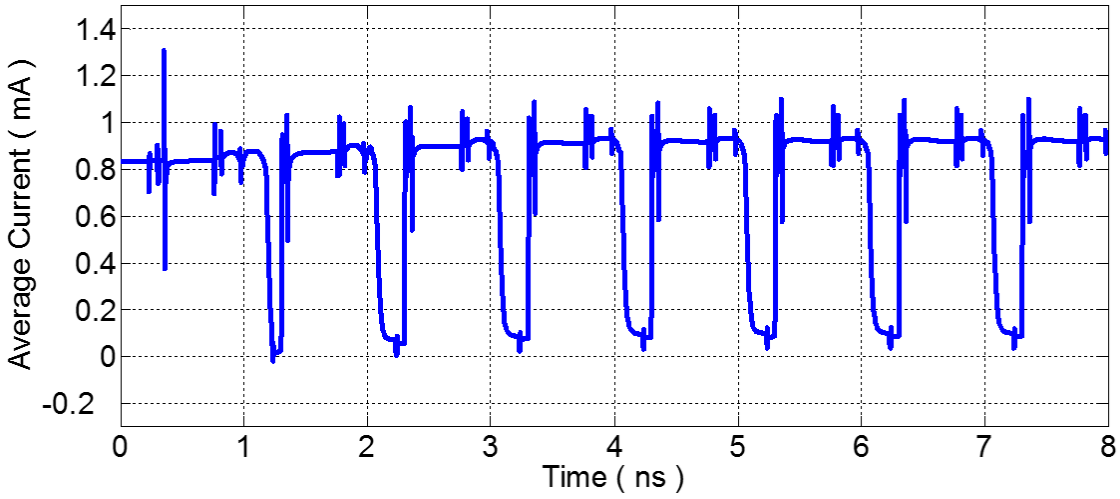

Fig. 4.7 Comparator average current

Dual offset cancellation is embedded to the circuit through the capacitors, C_S and C_{OC}. C_S will store the input offset voltage along with sampling the input signals, and the output offset voltage will be stored on C_{OC}. C_S should be chosen larger than C_{OC} since it has been used for the input offset storage purpose [54].

Comparator overdrive recovery plays an integral role in comparator design. The comparator will not be able to resolve the next input if the recovery time is not enough to discharge the previous state, an error will occur in the comparator output. Overdrive recovery test has been done and the results are shown in Fig. 4.8. It is obvious from the overdrive recovery test which the comparator can compare two different inputs right after each other without error occurance. Passive clamp, active restore, and low gain per each stage can minimize this effect.

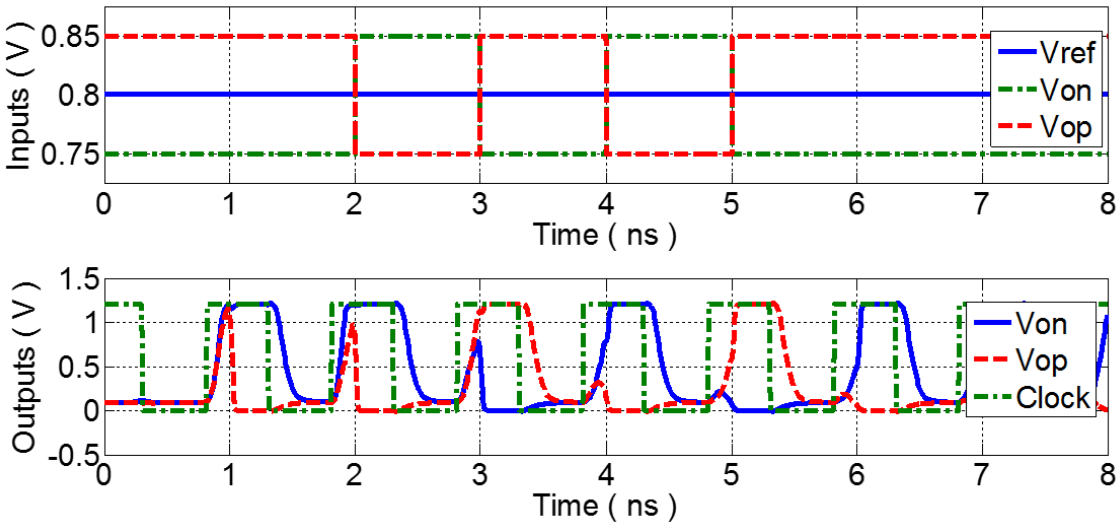

Fig. 4.8 Comparator overdrive recovery test

Several clocks with different duty cycles have been used to excite the comparator. This comparator works very fast because of the strong back to back inverter used at the comparator output. The latch should be deactivated when the preamplifier is amplifying the input voltage difference to reduce the power consumption. The other reason for the latch deactivation is preventing the comparator output from saturation. Since the comparator works based on the input voltage storage on the capacitor, it takes a time to charge and discharge the capacitor with respect to the input voltages. Therefore, the sample and set signals should be non-overlapping clocks. Clock signals used in the proposed comparator for transmission gates (TGs) are shown in Fig. 4.9.

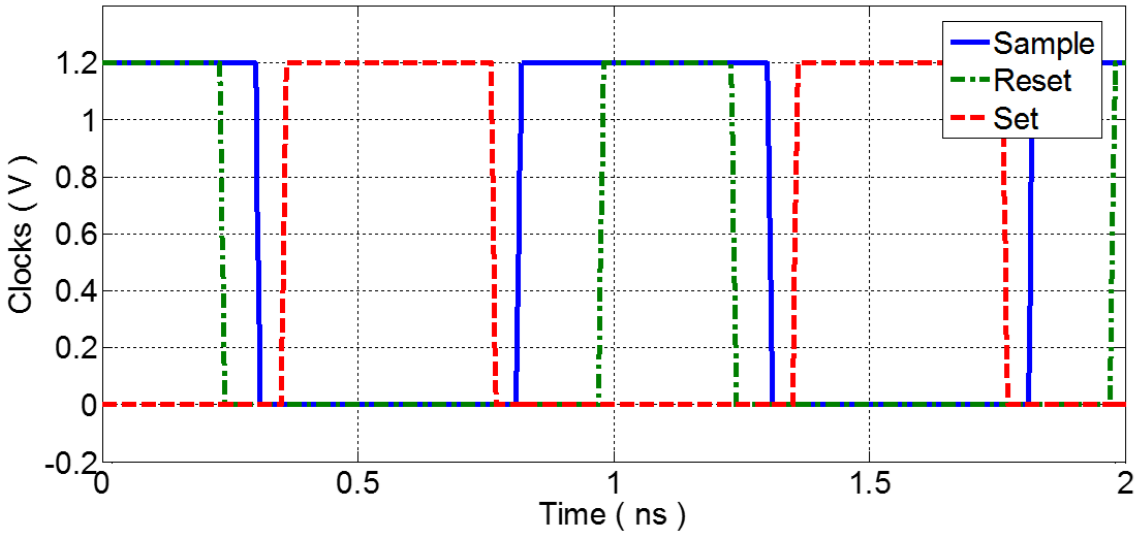

Fig. 4.9 Comparator clock signals

4.3 Phase Detector Design

The phase detector PD is an essential block in the various applications such as phase-locked-loops (PLL) which will turn the input phase difference over as high or low in output. In the other words, it works as a comparator which compares the phase, so it can be called as phase comparator. It can be made up of frequency mixer, analog multiplier, or logic circuits. Detecting the phase difference between the different comparators is so imperative in the proposed idea, so a precision phase detector which can detect the differences in the order of picoseconds is required. There are lots of different phase detector architectures which are suitable for various digital and analog applications [55-58].

The input voltages IN_1 and IN_2 have some phase differences. Consider the IN_1 is lagged; hence, the transistors M_1, M_9, and M_3 are off and M_2, M_8, and M_3 are on. The voltage difference will define the voltages at the XOR input gates through the back to

back inverters. Hence, the early signal will be high and the late signal will be down. The internal circuitry for the utilized phase detector is shown in Fig. 4.10.

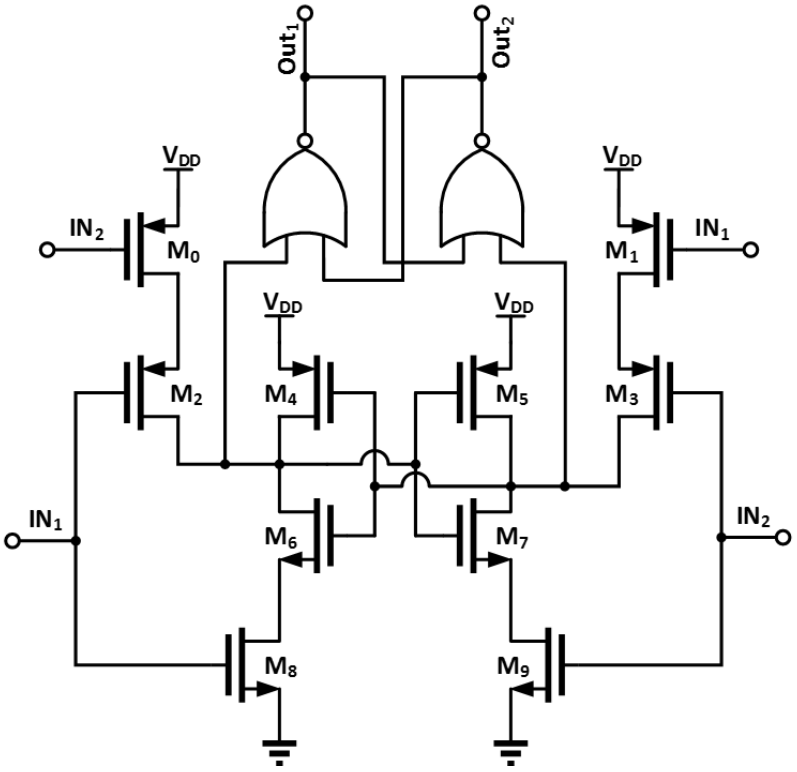

Fig. 4.10 Phase detector internal circuitry

The phase detector performance is evaluated and the results are brought in Fig. 4.11. As shown in Fig. 4.11, when the golden comparator output is lagged, the phase detector starts to generate a pulse at the output. In the same way, the phase detector output is low while the golden comparator is lead. The functionality of the circuits is shown at the transition edge but the complete process from far point of view has been shown in Fig. 4.12.

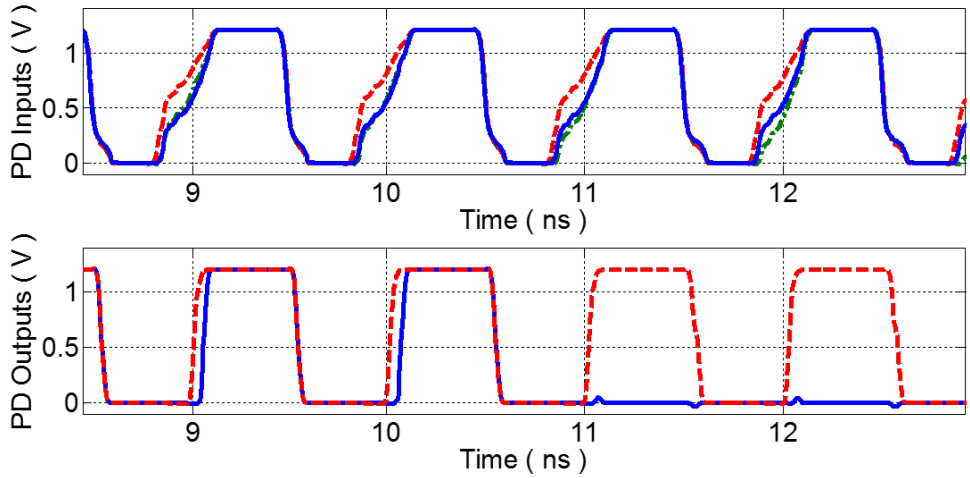

Fig. 4.11 Phase detector performance from close point of view

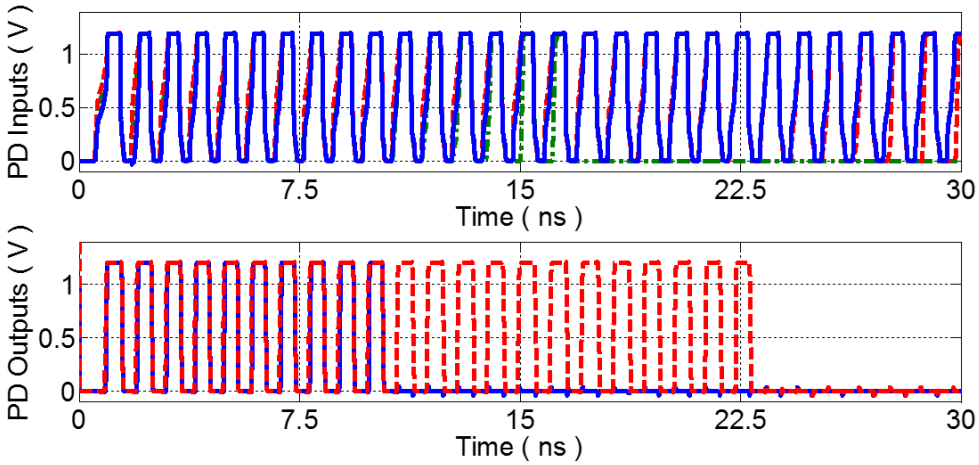

Fig. 4.12 Phase detector performance from far point of view

4.4 Overall Circuit Diagram

The comparator, phase detector, and the proposed idea were discussed in above sections. The integration of the blocks will be described in this section. Sixteen comparators used for the comparison purpose which the last one is added as a dummy comparator because of the last transition edge detection. The upper comparator, called the

golden comparator, is used for the extra bit generation through the comparator output comparison to the golden one.

The buffers are used to make the comparator outputs and the golden comparator output more clear for the comparison purpose and preparing enough drive capability for the comparator output since the output capacitor seen at the comparator output is considerable. Golden comparator senses the most capacitance due to the connection to the sixteen phase detector inputs. Each phase detector input capacitance has been monitored and it acts like 50 fF capacitor. Therefore, fifteen 50 fF capacitors are used at the output of each comparator to make the delay equal and the comparison valid. It is worth mentioning that the input characteristics of each phase detector have been processed by R-C test which means the input resistor and capacitor can be found by finding the input time constant.

Three Verilog-A blocks are built to help the simulations because an ideal DAC is required for doing the dynamic test. Therefore, the internal codes of Verilog-A blocks can be found in the appendix.

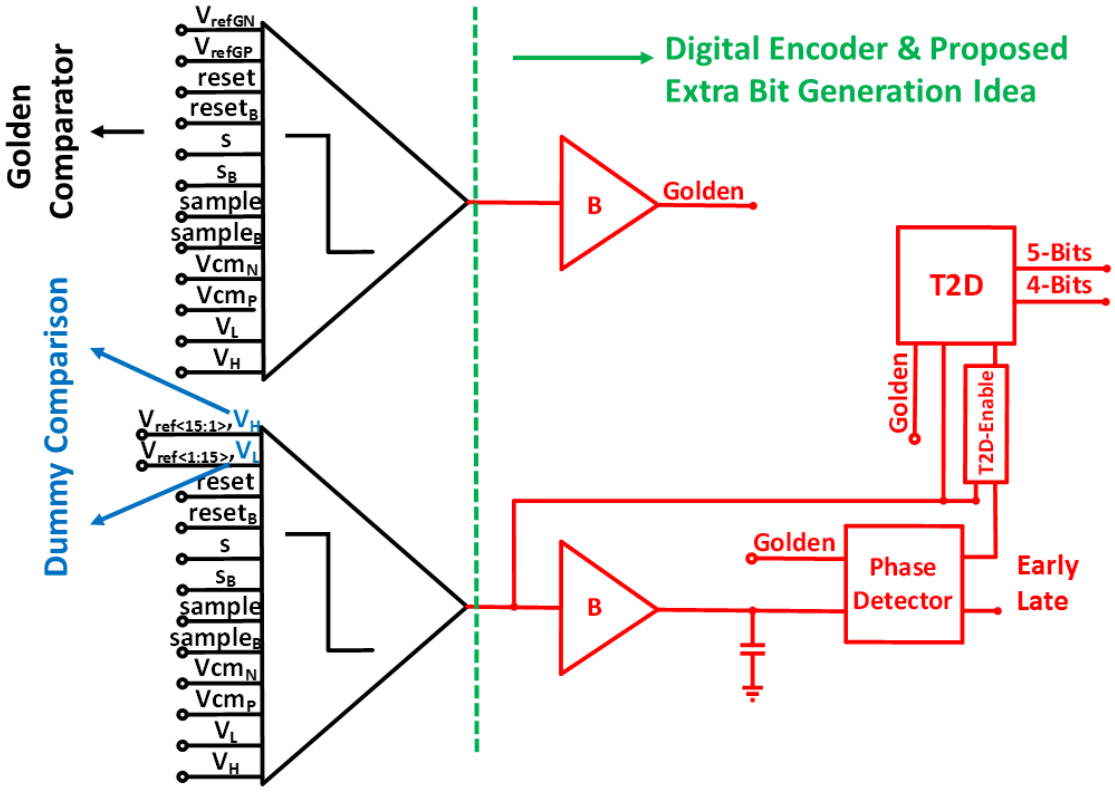

Fig. 4.13 Overall proposed Flash ADC block diagram

CHAPTER FIVE
Simulation Results

Proposed Flash ADC functionality has been monitored and assessed by doing the required simulations. The power consumption, dynamic test, and static test which can unveil the transient and frequency characteristics of the proposed ADC are done and the results are presented in the following subsections.

5.1 Power Consumption

Power consumption is one of the significant parameters considered in this study. As explained before, adding one more bit to the ADC will cause eight times more power consumption [50]. The proposed Flash ADC has been designed in TSMC 65 nm CMOS technology with 1.2 V power supply. The total power consumption includes three different sections; resistor ladder, comparators, and digital bit extraction circuit.

5.2 Static Tests

The more critical linearity measurement is measuring INL and DNL static tests which cannot be easily compensated in the digital domain because it depends on the overall performance of the ADC. They are known as the dynamic metrics for assessing the frequency performance of the presented ADC.

5.2.1 Differential Non-linearity

DNL is defined as the deviation of code width from ideal Δ (1LSB) when going through the transfer curve of an ADC. The end points should be connected to take away the offset and full scale error effects, and then the ideal transfer curve of the ADC will be achieved with the same offset and full scale error.

Ideally, ADC transition points are equal to Δ (1LSB) and the offset and full-scale error are removed for DNL calculation. DNL[k] shows the difference between the widths of the k-th code from its ideal width. Therefore, the DNL can be calculated as follows [59]:

$$\mathrm{DNL[k]} = \frac{\mathrm{Width[k]-LSB}}{\mathrm{LSB}} \tag{5.1}$$

Where Width[k] is the width of k-th code. It is obvious from (5.1) that the worst case DNL is -1 when the code width is zero which can be considered as a missing code. Moreover, it can be shown that the sum of all DNL numbers should be ideally equal to zero for an ADC.

The DNL performance of the proposed ADC is shown in Fig. 5.1. The DNL is calculated by applying a very slow ramp signal at the input so that 100 samples are taken for each code to reach reliable DNL value. According to the calculations, the worst case DNL is equal to +0.26 for the positive side and –0.17 for the negative side.

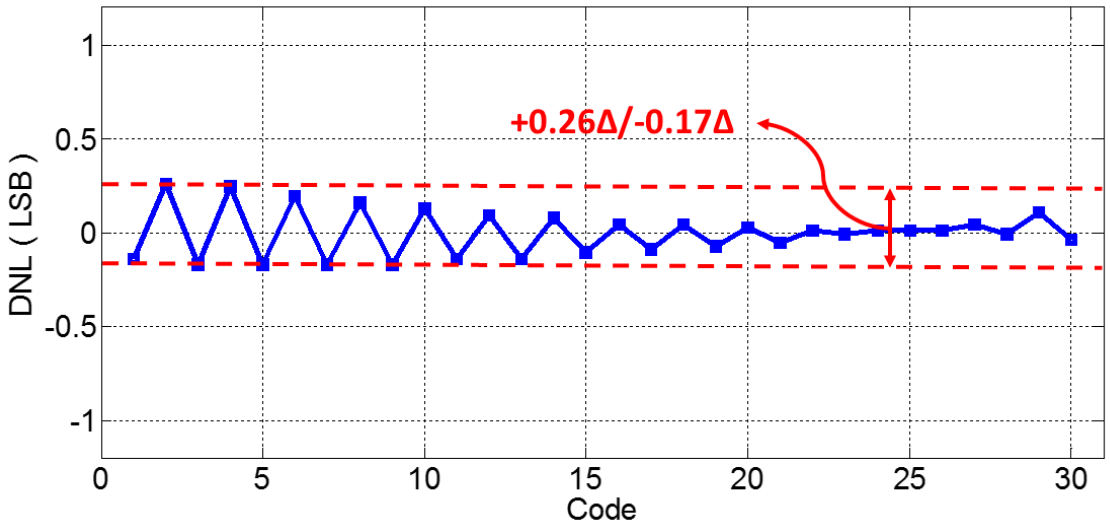

Fig. 5.1 DNL simulation results

5.2.2 Integral Non-linearity

The main static measure for quality of a data converter is usually INL which is more global type of measurement. It is basically a deviation of code transition from its ideal location. In the same way, the endpoints are connected to find the ideal characteristics. Ergo, the INL would be the difference between the real transition point and the ideal transition point.

The INL can be calculated by constructing an ideal staircase between first and last transition, and then the INL can be calculated by using the equation (5.2) [59].

$$\mathrm{INL[m]} = \frac{\mathrm{T[m]-T[ideal]}}{\mathrm{W[ideal]}} \tag{5.2}$$

Where W[ideal] is the ideal width for each code (LSB), T[m] is the m-th transition point and the T[ideal] is the m-th ideal transition point. However, the most common way for calculating the INL is (5.3). It can be inferred from (5.3) that the last code INL will be zero with respect to (5.1).

$$\mathrm{INL[m]} = \sum_{i=1}^{m-1} \mathrm{DNL[i]} \tag{5.3}$$

INL performance of the proposed ADC is shown in Fig. 5.2. The INL is calculated by applying a very slow ramp signal at the input so that 100 samples are taken for each code to reach a reliable INL value. According to the calculations, the worst case INL is equal to +0.22 for the positive side and –0.15 for the negative side.

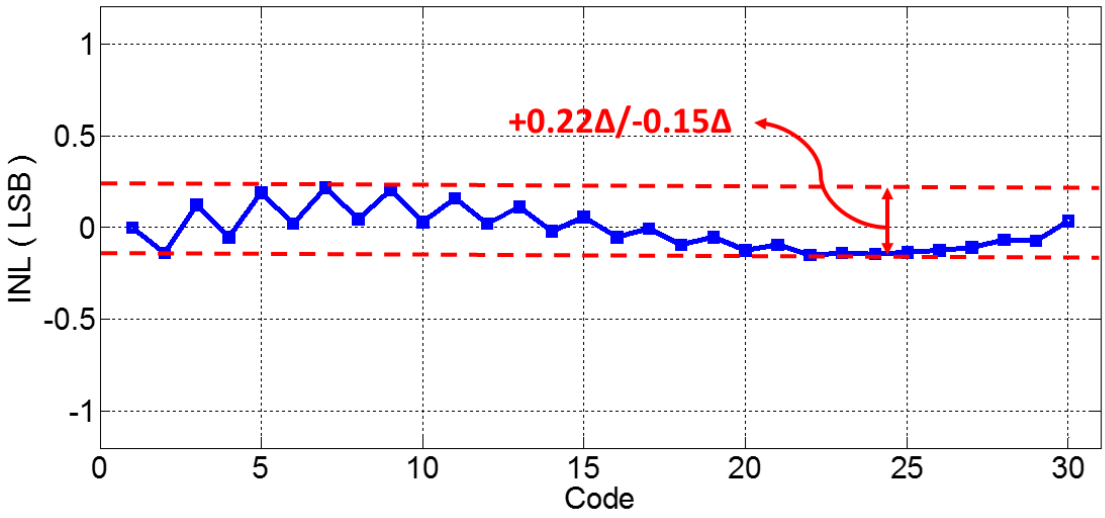

Fig. 5.2 INL simulation results

The transfer function can be generated by applying a low slope ramp. The slope should be too low to make sure that the simulation results are valid. One hundred samples per each code are required for running the ramp test based on the rule of thumb. A ramp test with the slope of 62.5k is applied to the input. The proposed ADC transfer function, which is monotonic, is depicted in Fig. 5.3.

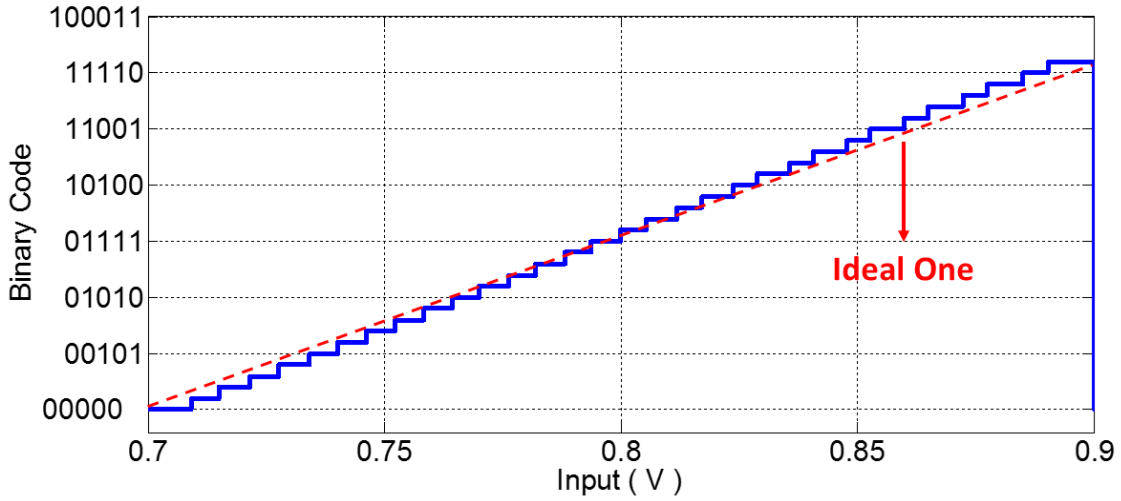

Fig. 5.3 Input analog signal conversion to digital code transfer characteristics

5.3 Dynamic Tests

The static test does not tell the full story of the ADC as we know that there was no information about the noise and high frequency effects on the static test. Therefore, there should be another test metric to assess the frequency characteristics.

In case of ADC testing, the device under test is an ADC that the input signal would be a sinusoidal signal from analog signal generator; the output would be digital codes. One way to find the quality of the proposed ADC is to have a DAC with much better performance. Hence, the output digital codes of the ADC would be the input of the digital to analog converter, and then the DAC output would be an analog signal. Ergo, the output signal frequency characteristics can be evaluated through a spectrum analyzer. The dynamic test block diagram of the analog-to-digital conversion is depicted in Fig. 5.4. A clean sinewave should be applied to the input and the spectral performance should be assessed at the output by using an ideal DAC converter.

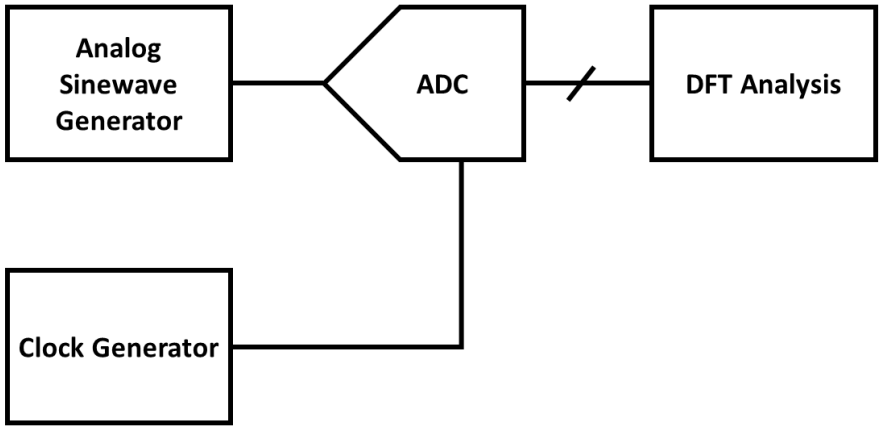

Fig. 5.4. Dynamic test block diagram

Another way of doing the dynamic test is using data acquisition system. Data acquisition system will grab the digital code from ADC and save it as a file. Then the process can be done by running a MATLAB code which is presented in the appendix.

There are some spectral performance metrics for ADCs including non-idealities which are going to be explained and simulated here. These parameters show how far the proposed ADC is from the ideal one.

Signal-to-noise ratio (SNR) which is defined as the signal power over the noise power which includes quantization noise, thermal noise, and flicker noise. It is worth mentioning that the signal power, DC component, and the harmonics power should set to zero for measuring the noise power. SNR is defined as follows [60,61]:

$$\text{Signal} - \text{to} - \text{noise ratio} = \frac{\text{Signal Power}}{\text{Noise Power}} \tag{5.4}$$

Signal-to-noise distortion ratio (SNDR) which is defined as the signal power over the noise power plus the distortion power that includes all the harmonic components. SNDR can be measured by:

$$\text{SNDR} = \frac{\text{Signal Power}}{\text{Noise Power+Distortion Power}} \tag{5.5}$$

The other parameter is spurious-free dynamic range (SFDR) which is defined as the signal power over the largest harmonic power. SFDR can be expressed by:

$$\text{SFDR} = \frac{\text{Signal Power}}{\text{Largest Harmonic Power}} \tag{5.6}$$

Effective number of bits (ENOB) is another dynamic test metrics of the proposed ADC. A question that might arise here is whether an ADC with less than 31.86 dB SNDR is exactly 5-bits ADC or not? 5-bits ADC needs at least 31.86 dB SNDR. Hence, ENOB is a parameter which shows how far the proposed Flash ADC is close to the ideal 5-bits Flash ADC. The ENOB can be computed as:

$$\text{ENOB} = \frac{\text{SNDR}-1.76\ \text{dB}}{6.02\ \text{dB}} \tag{5.7}$$

The ideal ENOB is achievable only in the case of neglecting thermal noise, DNL, and INL. Usually, it can be achieved by building low frequency and low resolution ADC but for the high frequency and high resolution ADCs is almost impossible. Rule of thumb for good performance/power trade-off is about one bit less than the specified number of bits.

Low noise design is costly because there is four times penalty in power per bit (ENOB) or 6 dB extra SNDR. That comes from the fact which the $\frac{g_m}{C}$ should be kept constant because of the working frequency of the ADC. The current should be bigger to increase the transconductance gain of the amplifier to make the noise smaller (transit frequency of MOS transistor is constant value) as it is obvious from the following equations:

$$v_n = \sqrt{\frac{KT}{C}} \tag{5.8}$$

$$f_T = \frac{g_m}{C} \tag{5.9}$$

$$g_m \propto I \tag{5.10}$$

The spectral test is done in two different input frequencies; Nyquist and DC. Because of the fast Fourier transform (FFT), the input frequency should be defined by (5.11). Bin 3 and bin 499 has been considered as the DC and Nyquist frequency, respectively. N shows the number of FFT points which is assumed 1024 in this study. Therefore, the DC frequency is equal to 487.3 MHz and the Nyquist frequency is equal to 2.93 MHz.

$$f_{in} = \text{bin} \times \frac{f_{sample}}{N} \tag{5.11}$$

The dynamic test for the Nyquist input frequency has been done and the simulation result is depicted in Fig. 5.5. As shown in the simulation results, achieved SNDR and SFDR are equal to 26.4 dB and 33.91 dB, respectively. Therefore, the calculated ENOB is 4.1 bits.

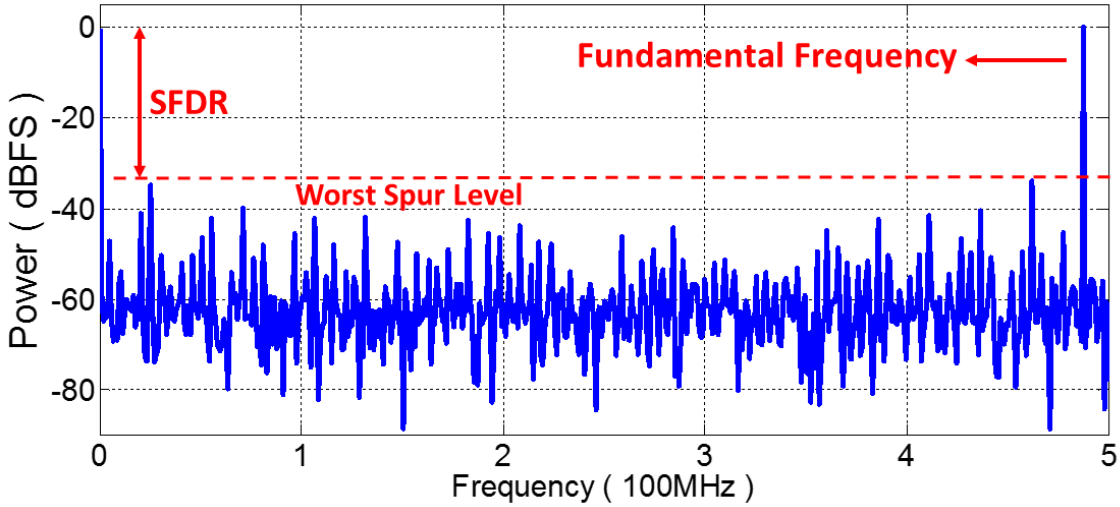

Fig. 5.5 Nyquist input frequency dynamic test results

In the same manner, the dynamic test for the DC input frequency is done and the simulation result is depicted in Fig. 5.6. As shown in the simulation results, achieved SNDR and SFDR are equal to 28.69 dB and 32.66 dB, respectively. Therefore, the calculated ENOB is 4.47.

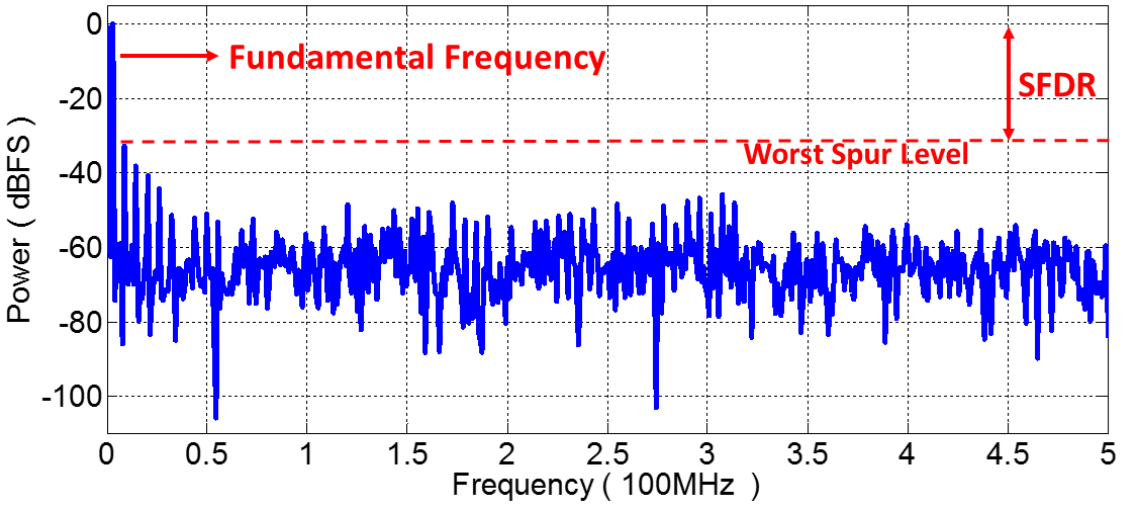

Fig. 5.6 DC input frequency dynamic test results

The dynamic test has been done in different input frequencies and the results are shown in Fig. 5.7, Fig. 5.8, and Fig. 5.9. It can be seen from Fig. 5.7 which the effective resolution bandwidth (ERBW) for the proposed ADC is more than Nyquist frequency.

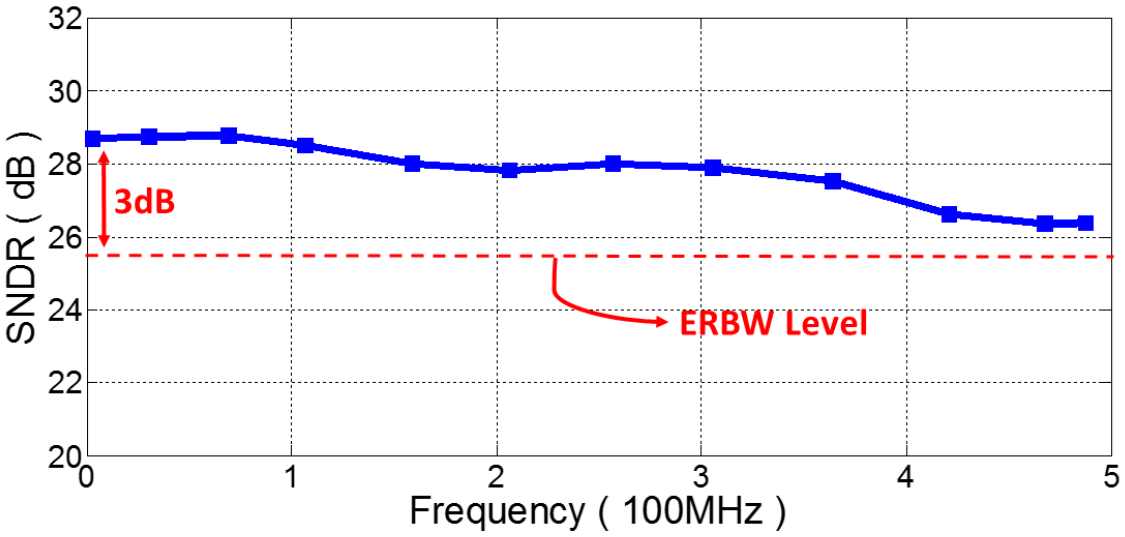

Fig. 5.7 SNDR measurements in different input frequencies

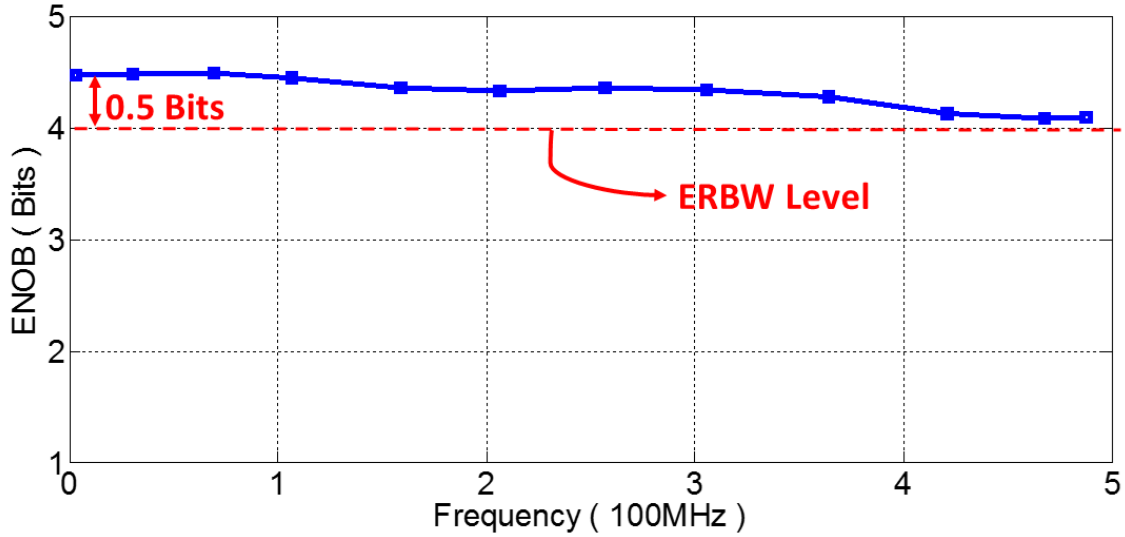

Fig. 5.8 ENOB measurements in different input frequencies

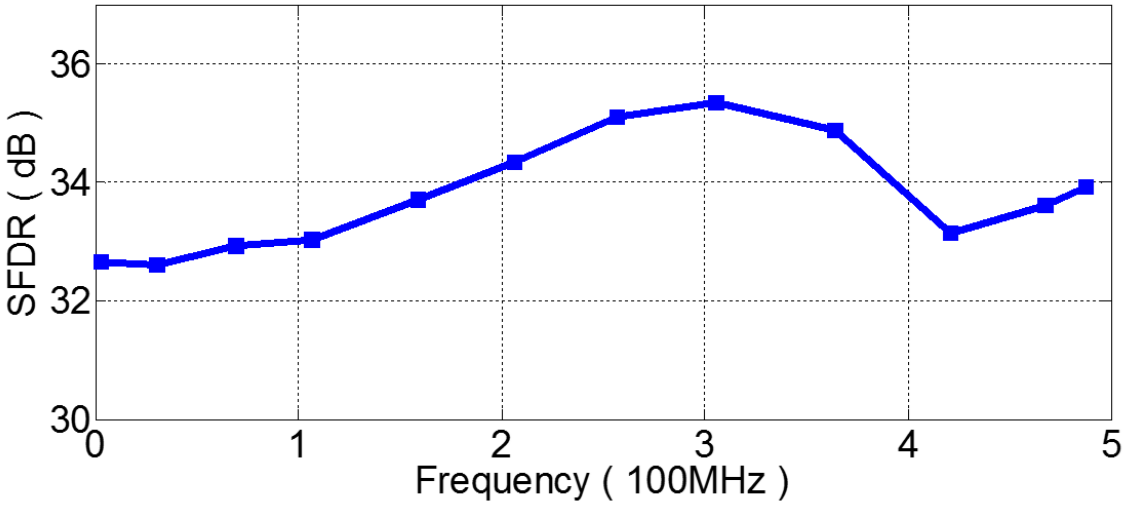

Fig. 5.9 SFDR measurements in different input frequencies

The comparator offset rejection performance is assessed by running the Monte Carlo simulation with 500 points iterations. Monte Carlo simulation confirms that the input referred offset voltage is equal to σ_{OS} = 723 μV. Simulated Monte Carlo histogram is demonstrated in Fig. 5.10.

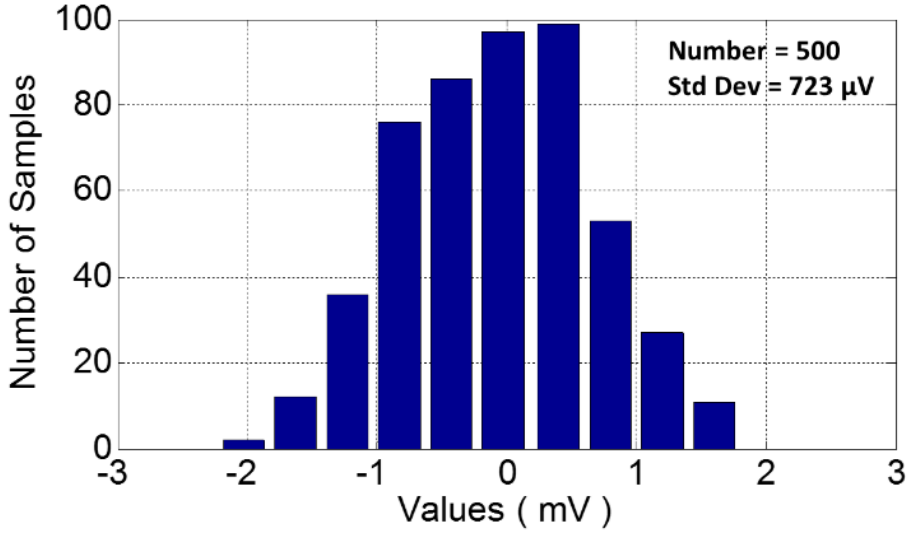

Fig. 5.10 Monte Carlo Simulation

CHAPTER SIX
Results Comparison

The performance of the proposed ADC is compared to previous works with the same Flash architecture and the results are summarized in Table 2. The calculated FoM is equal to 415 fJ/Convstep. Furthermore, comparison with all of the previously published ADCs has been done through the Murmann survey as shown in Fig. 6.1, Fig. 6.2, and Fig. 6.3 [62]. The f_{synq}, $f_{in,hf}$ are the sampling frequency and the input frequency which the dynamic test including ENOB measurement has been done. It is worth mentioning that the FoM used for this comparison is Walden FoM which can be defined as [63]:

$$\mathrm{FOM} = \frac{\mathrm{P}}{2^{\mathrm{ENOB}} \times \mathrm{f_s}} \tag{6.1}$$

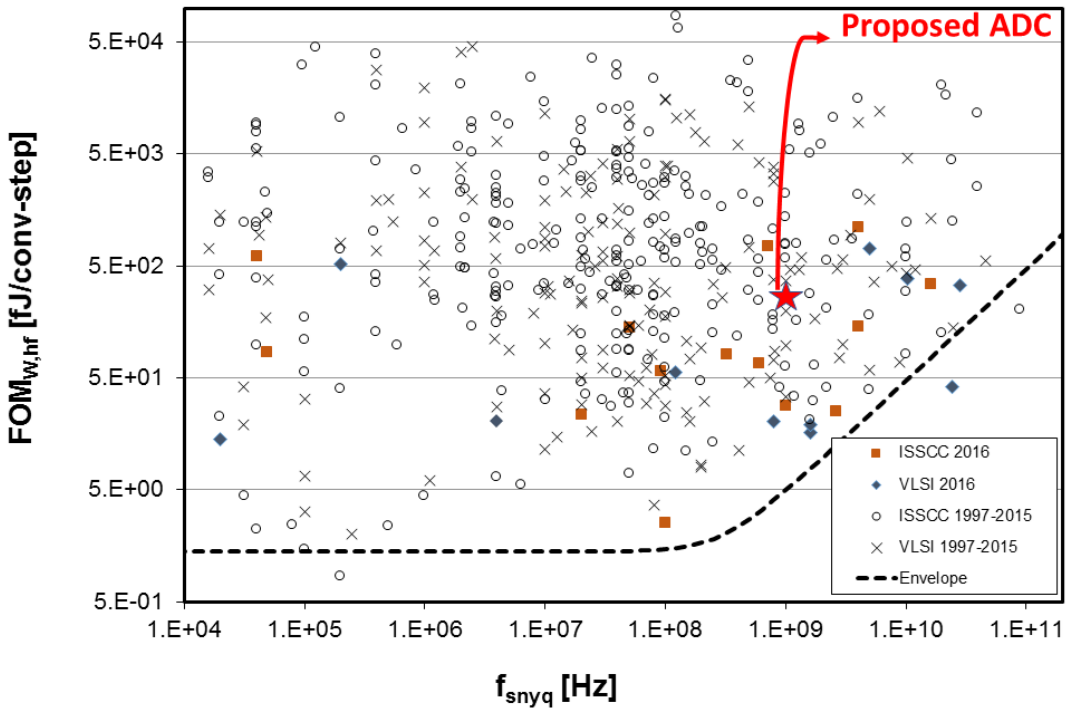

Fig. 6.1 Walden FoM comparison

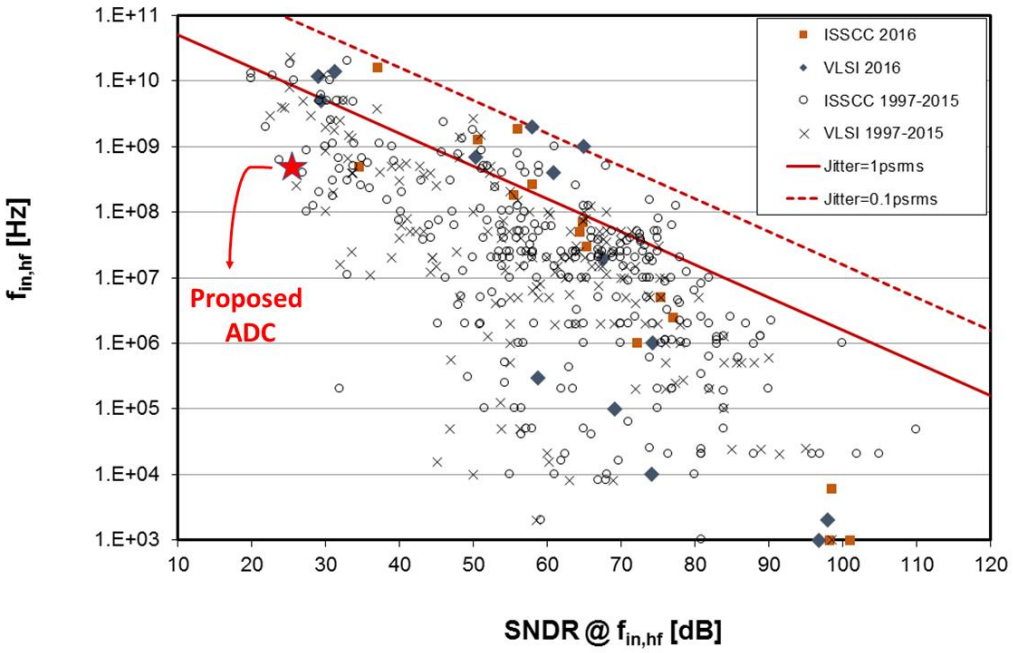

Fig. 6.2 Aperture Comparison

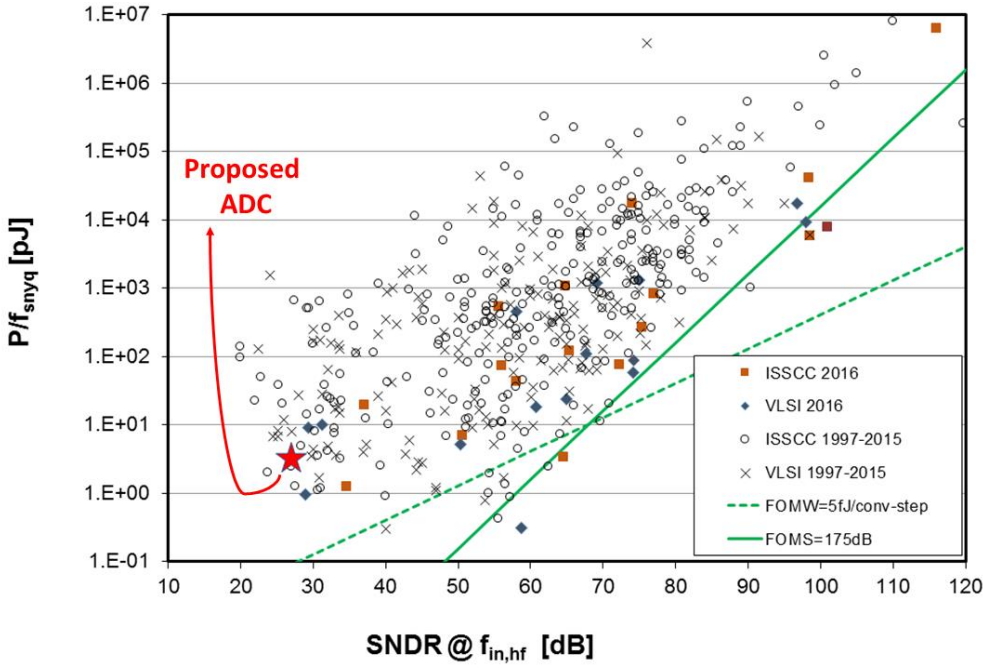

Fig. 6.3 Energy comparison

Table 2. Comparison to The Previous State-of-the-art Publication

Reference / Parameter	[64]	[65]	[66]	[67]	[68]	[69]	[70]	[71]	This Work
Technology (nm)	65	90	180	90	45	90	90	90	65
Resolution	7	6	4	7	7	6	5	6	5
V_{Supply} (V)	1.2	1.2	1.8	1.2	1.15	0.9	1	1.2	1.2
f_s (GHz)	2	1	1.8	1.5	1.4	3.5	1.75	3	1
ENOB (Bits)	6.04	5.4	3.7	6.05	6.17	4.69	4.6	5.3	4.1
INL (LSB)	0.64	0.74	0.3	0.64	1	0.96	0.39	0.2	0.22
DNL (LSB)	0.58	0.49	0.29	0.7	0.74	0.5	0.38	0.2	0.26
Power (W)	20.7	18.7	15.5	204	33.24	98	7.6	90	7.7
FoM (pJ/Conv.step)	0.157	0.44	0.695	2.06	0.57	0.95	0.15	2.28	0.415

CHAPTER SEVEN
Conclusion

A time-based Flash ADC has been designed in deep-submicron CMOS technologies. The number of comparators has been reduced about 45% in compare to the traditional Flash ADCs which are usually power hungry. The proposed Flash ADC was designed in 65 nm TSMC CMOS technology and has been compared to previous work through the calculated Walden FoM which is 415 fJ/Conv.step.

The static and dynamic tests are done to assess the proposed ADC's performance. The proposed architecture could achieve 4.1 bits ENOB at Nyquist frequencies and 4.47 bits ENOB at DC frequencies. The static performance of the proposed ADC was evaluated by doing a static test which resulted in 0.26 and 0.22 LSB for DNL and INL, respectively. The analog-to-digital conversion process was done by consuming merely 7.7 mW while the sampling frequency is 1 GHz.

It can be concluded that the proposed Flash ADC is suitable for low power applications such as biomedical devices. As the number of the comparators has been reduced considerably, the chip area is reduced. Therefore, a 5-bit analog-to-digital conversion process is done just by implementing 4-bit conversion.

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Appendix A: Ideal DAC Verilog-A Code

```
// VerilogA for TIME-BASED-FLASH-ADC, DAC-Ideal, veriloga

`include "constants.vams"

`include "disciplines.vams"

module dac_5bit_ideal (vd4, vd3, vd2, vd1, vd0, vout);

electrical vd4, vd3, vd2, vd1, vd0, vout;

parameter real vref  = 0.8 from [0:inf);

parameter real trise = 0 from [0:inf);

parameter real tfall = 0 from [0:inf);

parameter real tdel  = 0 from [0:inf);

parameter real vtrans  = 0.4;

real out_scaled; // output scaled as fraction of 32

   analog begin

      out_scaled = 0;

      out_scaled = out_scaled + ((V(vd4) > vtrans) ? 16 : 0);

      out_scaled = out_scaled + ((V(vd3) > vtrans) ? 8 : 0);

      out_scaled = out_scaled + ((V(vd2) > vtrans) ? 4 : 0);

      out_scaled = out_scaled + ((V(vd1) > vtrans) ? 2 : 0);

      out_scaled = out_scaled + ((V(vd0) > vtrans) ? 1 : 0);

      V(vout) <+ transition( vref*out_scaled/32, tdel, trise, tfall );

   end

endmodule
```

Appendix B: Thermal-to-Digital Converter Verilog-A Code

```
// VerilogA for Flash_ADC, T2D, veriloga

`include "constants.vams"

`include "disciplines.vams"

module T2D(in,clk,in_e,out_5Bits,out_4Bits,B0,B1,B2,B3,B4);

input [1:15] in;

input in_e, clk;

output out_4Bits,out_5Bits,B0,B1,B2,B3,B4;

integer  A,B,C,D, E,F,G,H,I, E2,F2,G2,H2;

genvar jc;

electrical [1:15] in;

electrical out_5Bits,out_4Bits,in_e,B0,B1,B2,B3,B4;

electrical clk;

analog begin

@(initial_step)

   begin

      C=0;

      A=0;

      B=0;

//       E=0;

//       F=0;

//       G=0;
```

```
//        H=0;
//        I=0;
end
@(cross(V(clk)-0.6,+1))
begin
    A = 0;
    if ( V(in_e) > 0.6 )
        C = 1;
    else
        C = 0;
    for (jc=1; jc<16; jc=jc+1)
    begin
         if ( V(in[jc]) > 0.6 )
            D = 1;
        else
            D = 0;
        A = A + D;
    end
    B  = A*2 + C ;
    E = B % 2;
    E2 = B / 2;
    F = E2 % 2;
```

```
    F2 = E2 / 2;
    G = F2 % 2;
    G2 = F2 / 2;
    H = G2 % 2;
    H2 = G2 / 2;
    I = H2 % 2;
end
V(out_5Bits) <+ B;
V(out_4Bits) <+ A;
V(B0) <+ E;
V(B1) <+ F;
V(B2) <+ G;
V(B3) <+ H;
V(B4) <+ I;
end // of analog
endmodule
```

Appendix C: Thermal-to-Digital Converter Enable Verilog-A code

```
// VerilogA for mehdi, T2D_Enable, veriloga

`include "constants.vams"

`include "disciplines.vams"

module T2D_Enable(in1, in2, out);

input [1:16] in1,in2;

output out;


real  A, B, C, D;

genvar jc;

electrical [1:16] in1,in2;

electrical out;

analog begin

@(initial_step)

   begin

      A=0;

      B=0;

   end

A = 0;

B = 0;

for (jc=1; jc<17; jc=jc+1)

   begin
```

```
        if ( V(in1[jc]) > 0.6 )
           D = 1;
        else
           D = 0;
           A = A + D;
    end
for (jc=1; jc<17; jc=jc+1)
    begin
        if ( V(in2[jc]) > 0.6 )
           C = 1;
        else
           C = 0;
           B = B + C;

    end
begin
if (( A == B ) && (A != 0))
        V(out) <+ 1.2;
else
        V(out) <+ 0;
end
end //analog
```

```
endmodule
```

Appendix D: Dynamic Test Measurement MATLAB Code

```
clear all

clc

data = csvread('1024.csv',1,0);

x = data(1:end,1);

y = data(1:end,2);

%z = abs(y);

P = abs(y);

%P = (z.^2)/1024;

plot(x,abs(P))

N = 5;

Power_Sort = sort((P(2:end)),'descend');     %removing DC bin

Sig_Power = (Power_Sort(1))     %fin

Ext_Power = (sum(Power_Sort(2:end))) %measuring the distortion and noise

SNDR = 10*log10(Sig_Power/Ext_Power)

SQNR = 6.02*N+1.76

NFloor = SQNR - 10*log10((2^10)/2)

ENOB = (SNDR-1.76)/6.02

SFDR = 10*log10(Sig_Power/max(Power_Sort(2:end)))

Tot_Power = sum(P(1:end))
```