Optimizing Ferroelectric Nanowire FET for Sub-60mV/decade Sub-threshold Slope

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OPTIMIZING FERROELECTRIC NANOWIRE FET FOR SUB-60MV/DECADE
SUB-THRESHOLD SLOPE

A Thesis
Presented to
The Faculty of the Department of Electrical Engineering
San José State University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science

by
Abhishek Kartik Raol
August 2020
The Designated Thesis Committee Approves the Thesis Titled

OPTIMIZING FERROELECTRIC NANOWIRE FET FOR SUB-60MV/DECADE SUB-THRESHOLD SLOPE

by

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APPROVED FOR THE DEPARTMENT OF ELECTRICAL ENGINEERING

SAN JOSÉ STATE UNIVERSITY

August 2020

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ABSTRACT

OPTIMIZING FERROELECTRIC NANOWIRE FET FOR SUB-60MV/DECADe SUB-THRESHOLD SLOPE

by Abhishek Kartik Raol

Limitations in traditional scaling methods require novel devices to increase computational density without scaling down device size. Ferroelectric materials’ negative capacitance property reduces the subthreshold slope beyond the previous theoretical ideal of 60 mV/decade and improves computational density without reducing transistor size. The research herein characterizes fields in isolated ferroelectric material, ferroelectric-oxide interfaces, and ferroelectric material integrated in the gate-stack of a ferroelectric nanowire-FET (FeNW) to achieve sub 60 mV/decade subthreshold slope. The research attains sub 60 mV/decade subthreshold slope across multiple FeNW configurations, and subsequently provides a ferroelectric-to-oxide capacitance, ratio-based design method to approaching sub-60 mV/decade subthreshold slope and narrowing the device design space. The research concludes by disclosing design tradeoffs when attaining sub 60 mV/decade subthreshold slope, to provide an engineer or physicist insight on the applications and limitations of the present state of ferroelectric nanowires and ferroelectric FETs.
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LIST OF ABBREVIATIONS

$C_{fe}$ Ferroelectric layer capacitance
$C_{fox}$ Series capacitance of ferroelectric and oxide layer capacitance
FeFET Ferroelectric Field Effect Transistor
FeCAP Ferroelectric capacitor structure
FoxCAP Series ferroelectric-oxide capacitor structure
FeNW Ferroelectric nanowire structure
FET Field Effect Transistor
HfO$_2$ Hafnium dioxide
$I_d-V_g$ Drain current vs gate voltage relationship and/or curve
$I_{on}$ Drain current, during ON gate bias
$I_{off}$ Drain current, during OFF gate bias
$L$ Channel length
MOSFET Metal-Oxide Field Effect Transistor
$S_{device}$ TCAD Sentaurus device simulator
$S_{visual}$ TCAD Sentaurus visualization tool
SiO$_2$ Silicon dioxide
S.S. Subthreshold slope in milli-Volts per decade (mV/decade)
t$_{fe}$ Ferroelectric layer thickness
t$_{ox}$ Oxide thickness
t$_{si}$ $1/2$ of silicon channel thickness
TCAD Technology Computer-Aided Design
$V_d$ Drain voltage
$V_{fe}$ Voltage across ferroelectric Layer
$V_g$ Gate voltage
Y-HfO$_2$ Yttrium-doped Hafnium dioxide
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|                                | \( c_0 = 6\gamma_{fe} \) | (5.1.a) (5.1.b) (5.1.c) respectively |
| Macroscopic field              | \( E = E_0 - E_1 \)  
|                                | \( E_0: \text{Applied External Field} \)  
|                                | \( E_1: \text{Depolarization Field} \) | (5.2) |
| Landau-Khalatnikov (LK) based TCAD Electric field-polarization relationship | \( E = 2\alpha P + 4\beta P^2 + 6\gamma P^5 - 2g\Delta P + \rho \frac{dP}{dt} \) | (5.3) |
| Electric field                 | \( E = \frac{V}{d} \) | (6.0) |
| Charge-based capacitance equation | \( C = \frac{dQ}{dV} \) | (7.0) |
| Fixed charged-based capacitance equation | \( C = \frac{Q}{V} \) | (7.1) |
1 INTRODUCTION

1.1 Device Scaling Limitations

Research in novel semiconductor devices is rooted in the seminal issue regarding degradation of Moore’s scaling law. The industry has followed constant field scaling with linear down-scaling of feature sizes to linearly increase CPU frequency, power, and computation density, among other circuit and device performance metrics as seen in the Fig.1 [1]. However, short channel effects such as drain-induce-barrier-lowering, band-to-band tunneling and process variations are significant sources of performance degradation in sub-micron devices, and even more so in current 10 nm and below technology nodes. As such, down-scaling device sizes face laws of diminishing return, and a need exists for novel methods of scaling up device performance, aside from constant field scaling. With the growth of high bandwidth, high-frequency computing, subthreshold slope improvement can scale CPU frequency, and is a core design target for the present research. An ideal MOSFET turns on instantaneously when an ON-voltage is
applied to the gate. The subthreshold slope measures the switching speed of a MOSFET, where a lower subthreshold slope is the desired metric. The subthreshold slope measures the amount of gate voltage needed to change the current by a decade. An ideal MOSFET would instantly turn on, meaning a MOSFET with a subthreshold slope of 0 mV/decade. However, an ideal 0 mV/decade subthreshold slope is unattainable, due in part to the gate capacitance of the MOSFET. The subthreshold slope is proportional to the capacitance seen on the gate of a MOSFET; a smaller capacitance on the gate-stack results in a smaller subthreshold slope [2]. A typical scaled technology achieves a subthreshold slope around 70 mV/decade, which is still higher than the theoretical ideal of 60 mV/decade. The subthreshold slope is calculated by:

\[
S.S. = \left(\frac{KT}{q}\right) \cdot \ln(10) \cdot \left(1 + \frac{C_{si}}{C_{ox}}\right)
\]

where:

\[
n_{norm} = (1 + \frac{C_{si}}{C_{ox}})
\]

Traditional scaling methods reduce oxide thickness, which increases the oxide capacitance, reduces n, and reduces the subthreshold slope. However, with this method, n always remains greater than 1, hence the 60 mV/decade limit. By achieving a negative oxide capacitance with the use of ferroelectric material, n can drop below 1, and a sub 60 mV/decade slope is possible. Achieving a sub 60 mV/decade subthreshold slope and demonstrating the novel device’s utility in a SRAM cell enables higher computational density without scaling device size, and will usher in a new era of device scaling methods.

1.2 Motivation for Ferroelectric FETs

The main case for ferroelectric FETs is to design steep subthreshold slope devices which enable fast switching speed, high frequency computing and high \(I_{on}/I_{off}\) ratios. Currently, the use of high-K dielectrics on the gate-stack allows good coupling of the gate to the channel to increase oxide capacitance, improve subthresholds slope and increase
\( I_{on}/I_{off} \) ratio. However, even if a device with an infinitely large-K dielectric existed, it would allow only a sub 60 mV/decade subthreshold slope as observed in Eq. (1.2). To surpass a sub-60 mV/decade subthreshold slope, the ‘n’ term in Eq (1.3) must be less than 1. Ferroelectric material’s ability to exhibit an effective negative capacitance, when placed on the gate, allows it to achieve an effective negative gate-stack capacitance by reducing the ‘n’ term Eq. (1.3) below 1, resulting in a sub-60 mV/decade subthreshold slope according to Eq. (1.2). Moreover, this frequency scaling can be achieved without scaling down device size, allowing possibly cheaper and easy to fabricate, high performance FETs. Second, the remnant polarization characteristics described in section 1.3 allows charge storage during device OFF state, which opens applications for non-volatile memory using a standard FET with a ferroelectric integrated gate-stack. Furthermore, remnant polarization characteristics of FeFETs allow positive \( I_{on} \) threshold and negative \( I_{off} \) threshold voltages, which allow adjustable threshold voltage MOSFETs. Such behavior is useful in neuromorphic computing applications, where information paths retain memory based on previous read/write cycles. The study of ferroelectric materials is not new, but research on ferroelectric material behavior and its integration into traditional FETs is lacking, considering the potential benefits of ferroelectric FETs. Rigorous TCAD simulations prior to fabricating experimental ferroelectric FETs will allow device engineers to study ferroelectric behavior, and its benefits and limitations to narrow the application space of ferroelectric devices and shape its future. The motivation of the present study is to understand how device design variables affect ferroelectric behavior, and how that ferroelectric behavior affects device performance, so a device engineer can understand how to optimize a ferroelectric FET for his or her design specifications.

1.3 Fundamentals of Ferroelectric Material

Ferroelectric materials exhibit a unique set of properties apart from traditional dielectrics such as SiO2 or HfO2. First, ferroelectric materials exhibit spontaneous
polarization, due to unstable dipole moments in ferroelectric ions. Ferroelectric ions induce a dipole moment which creates a charge displacement opposing an external electric field. Moreover, ferroelectric dipole moments are unstable and remnant, meaning the dipole moment’s polarization charge remains after the external field is removed. In traditional dielectrics, the polarization charge is lost once the electric field is removed. As such, ferroelectric materials exhibit charge-based polarization-memory. Furthermore, ferroelectric materials spontaneous polarization enables effective negative capacitance. In Fig.2, an external applied field $E_0$ traverses from a high potential (right side of image in Fig.2), to the low potential (left side of image in Fig.2). Within the material, fictitious surface charges are induced by the external electric field, creating a polarization field across the material between each dipole moment, denoted by the blue +/- signs, within the material. The surface charge density creates an internal depolarization field $E_1$ across the material which opposes the direction of the external electric field $E_0$.

Critical to ferroelectric material is the polarization $P$, which is the average density of dipole moments within the material, i.e. the material’s average dipole moment per unit volume [3]. Ferroelectric materials exhibit dipole moments with polarization charge opposing the direction of the external electric field, or a charge distribution opposite in magnitude to a normal, non-ferroelectric dielectric. Therefore, according to Eq. (7.1), a negative charge distribution under the same voltage gives an effective negative capacitance in a ferroelectric-layer capacitor.

$$C = \frac{Q}{V} \quad (7.1)$$

Although an isolated ferroelectric capacitor provides an effective negative capacitance, the Landau Khalatnikov free energy theorem of ferroelectric material shows the voltage gain $\alpha_f$ of negative capacitance gives positive feedback and an unstable runoff capacitance. Therefore, a ferroelectric capacitor must be in series with a positive capacitor.
for the system to be stable. For this demonstration, we will use a positive oxide capacitance $C_{ox}$ as the positive series capacitance, where $-\alpha_f Q$ represents the ferroelectric capacitance $C_{fe}$ (Fig. 3). The total series capacitance is $C_{f,ox}$, is given by the expressions:

$$C_{f,ox} = \frac{Q}{V} = C_o (V_1 + \alpha_f Q) \quad (4.1)$$

$$C_o \frac{1}{1 - \alpha_f C_o} \quad (4.2)$$

With the series positive and negative capacitance, the series capacitance system obeys the following conditions: If:

$$1 > \alpha_f \rightarrow C_{ox} + C_{f,ox}$$

$$1 = \alpha_f C_{ox} \rightarrow \infty C_{f,ox}$$

$$1 < \alpha_f C_{ox} \rightarrow -C_{f,ox}$$

### 1.4 Literature Review

Prior research in the field demonstrates sub 60 mV/decade subthreshold slope using FeFETs. FeFETs demonstrate a Vth shift and significant improvement in $I_{on}/I_{off}$
ratios [4]. H-FeFETs with Ferroelectric layer on the FET drain, enable a programmable Vt of the MOSFET which allow high and low Vt states to vary the channel resistance, increase the on-to-off current ratio, thus improving the memory wall for Non-Volatile memory applications.

1.4.1 Physics and Modeling of Ferroelectrics

Ferroelectric behavior and software simulations of ferroelectric material rely on the Landau-Khalatnikov (LK) dynamical ferroelectric model, to extract coercive electric fields and compute hysteresis behavior [5]. The LK equation is a function of ferroelectric polarization parameters $\alpha, \beta, \gamma$ and $\rho$. Modifying the ferroelectric polarization parameters of the LK equation, changes the coercive field strength of ferroelectric material and impacts the hysteresis behavior, Synopsys TCAD Sentaurus solves the Poisson equation with the LK equation, giving the polarization to electric-field relationship in Eq. (5.3) [6].

$$E = 2\alpha P + 4\beta P^2 + 6\gamma P^5 - 2g\Delta P + \rho dP dt \quad (5.3)$$

1.4.2 Designing and Characterizing Ferroelectric Devices

Experiments with tri-gate, and gate-all-around FETs with a ferroelectric gate-stack have approached, and in the case of a gate-all-around FET surpassed the sub 60
mV/decade subthreshold slope. Increase in $t_{fe}$ shows $I_{off}$ reduction as well as increased subthreshold slope in the gate-all-around nanowire. The nanowire research also modified the aspect ratio of the nanowire and found lower aspect ratios produce better subthreshold slope and better $I_{on}/I_{off}$ ratios. Non-negative benchmark nanowire FETs showed impressive 60 mV/decade subthreshold slope, and including a ferroelectric layer in the gate-stack, showed significant improvements in subthreshold slope with a best case around 40 mV/decade [7]. Chatterjee’s research at UC Berkeley of a tri-gate ferroelectric FET, analyses polarization and Id-Vg hysteresis in the FinFET structure [8]. The research consists of a silicon substrate, 200 nm buried oxide and 20 nm silicon-on-insulator device layer. The devices gate-stack consists of a 2 nm SiO2 layer, 5 nm HfO2 dielectric with dielectric constant of 18 and a gate metal work function of 4.8 eV. They began with analysis of a pure ferroelectric capacitor to understand field behavior of the ferroelectric layer before integrated the ferroelectric capacitor on the gate of a FinFET in TCAD. The research also fabricated the ferroelectric FET to successfully calibrate the TCAD ferroelectric parameters to the experimental results, however sub 60 mV/decade subthreshold slope was not observed. Even so, the research demonstrates accurate TCAD matching of sprocess simulation to experimental results of a ferroelectric FinFET.
2 RESEARCH METHODOLOGY

2.1 Synopsys Sentaurus TCAD Environment for Ferroelectric Research

The present research integrates, models, and simulates ferroelectric materials and devices in the Synopsys, Sentaurus TCAD Version Q-2019.12 Software, as seen in Fig.4. Critical to the research herein, Sentaurus TCAD Version Q-2019.12 utilizes a ferroelectric license to characterize static properties of ferroelectric material, remnant polarization, saturation polarization and coercive field. The ferroelectric license also parameterizes the transient response of ferroelectric material by the relaxation time and the nonlinear coupling constant [9].

Fig. 4: Synopsys sentaurus TCAD software version.

To integrate ferroelectric material, in the TCAD structure editor we place a region named “R.FE12,” referencing the ferroelectric material “FE12,” modeled after yttrium-doped hafnium dioxide (\(Y\mathrm{–}HfO2\)). In Sentaurus Device, calling a physics function for the “FE12” material, calling the polarization function, and including the compatible polarization model in the math section, enables ferroelectric specific simulations, including but not limited to remnant polarization and coercive field. In the polarization function, within the “FE12” physics section of Sentaurus Device, defining the
ferroelectric polarization parameters alpha, beta, gamma and rho, allows modification of the polarization and coercive field strength of the ferroelectric material. To obtain a plot of the polarization field and generate hysteresis curves in Sentaurus Visual, we include a polarization/vector in the plot section of Sentaurus Device. For this research, we use a 2D planar structure of a nanowire to study the fields and apply cylindrical coordinates, which rotates the 2D structure about the middle of the Si channel to simulate the 3D FeNW. Details on the design and simulating of the FeNW are discussed in chapter 4.

2.2 Design of Experiment

We start by creating a pure-isolated ferroelectric capacitor to study how the polarization field, ferroelectric capacitance and hysteresis behave under certain $V_{fe}$. Studying FeCAP demonstrates what static $V_{fe}$ gives us a desired negative capacitance $C_{fe}$, and how different $V_{fe}$ sweep ranges affect polarization field hysteresis of the ferroelectric capacitor. We also study the ferroelectric thickness effect, and ferroelectric polarization parameters’ effects on polarization and $C_{fe}$. We then proceed by attaching a series oxide capacitance to construct a series ferroelectric-oxide capacitance $C_{fox}$, which is the gate-stack of the FeNW. First we observe $V_{fe}$ as a function of ferroelectric to oxide thickness ratios and under what conditions and $t_{fe}$/$t_{ox}$ ratios the FoxCAP exhibits negative capacitance. We then study the $t_{fe}$/$t_{ox}$ ratio effect on FeCAP hysteresis. Finally, we integrate the FoxCAP gate-stack on the FeNW with a silicon channel. Study of the FeCAP and FoxCAP applied a bias voltage to the ferroelectric contact, while grounding the “back gate” of the capacitor. In the FeNW configuration, the gate is the only lateral contact, with a source and drain contact on either ends of the channel length. Integrating the FoxCAP on the FeNW’s gate creates $C_{fox}$ in series with $C_{si}$. Sacrificing control of $V_{fe}$ and $V_{ox}$ in our device, we study the electrostatic potential distribution within the device and extract $C_{fe}$, $C_{ox}$, $C_{si}$ and $C_{fox}$ of the FeNW to find regions of negative capacitance corresponding to sub 60 mV/decade S.S. By studying the electrostatic
potential drop across the ferroelectric and oxide layers in the FeNW, we apply the voltage pulse seen at the oxide-silicon interface in the FeNW, to the oxide contact of the FoxCAP to compare the field and capacitance of the isolated FoxCAP to the FoxCAP integrated in the FeNW. We use a similar method to study the pure FeCAP.
3 THE FERROELECTRIC CAPACITOR

3.1 The Isolated Ferroelectric Capacitor

We begin the study of ferroelectric behavior by creating a pure ferroelectric capacitor (Fig. 5), to observe the polarization field hysteresis in the ferroelectric layer. A voltage is applied to the “gate contact” while grounding the “back gate” (V@ “back gate” = 0V). Under the aforementioned bias, the gate voltage is equivalent to the electrostatic potential difference across the pure ferroelectric capacitor, $V_{fe}$, and allows study of the ferroelectric capacitor under different $V_{fe}$ conditions. Characterizing the polarization field in the isolated ferroelectric layer enables a device designer understanding of how ferroelectric thickness and $V_{fe}$ affect the coercive field and by producing an effective negative capacitance, which is necessary for the target sub-60 mV/decade subthreshold slope.

![Fig. 5: Pure 6 nm ferroelectric capacitor in TCAD structure editor.](image)

3.1.1 Ferroelectric Thickness Effect on Hysteresis

The experiment herein varies ferroelectric thickness in a pure ferroelectric capacitor to measure the ferroelectric thickness effect on polarization hysteresis. With a voltage applied to the gate contact and the back gate grounded (see Fig. 5), the polarization field...
within the ferroelectric capacitor is measured as a function of the electrostatic potential difference across the ferroelectric capacitor $V_{fe}$. The electric field and electrostatic potential are directly proportional:

$$E = \frac{V}{d} \quad (6.0)$$

Fig. 6 demonstrates an increase in the polarization field hysteresis range $a$ with reduction in ferroelectric thickness as expected. The hysteresis plot (Fig.6) demonstrates a “flip” in the polarization field direction at a critical $V_{fe}$ for various ferroelectric thicknesses. The polarization field flips at both a negative and positive $V_{fe}$, where the absolute difference between the positive and negative “flip” $V_{fe}$ ’s, denote the hysteresis width. A device engineer should consider hysteresis width, as a larger hysteresis width
impacts the $I_{off}$ threshold voltage seen in a device’s Id-Vg curve, and directly correlates to Id-Vg hysteresis, explored in chapter 5.

3.1.2 Ferroelectric Polarization Parameters Effect on Hysteresis

The experiments herein vary the ferroelectric material polarization parameters alpha and beta to measure the effect on the polarization field hysteresis of a pure ferroelectric capacitor. The ferroelectric polarization parameters determine the voltage across the ferroelectric layer, given by:

$$V_{fe} = a_0Q_g + b_0Q_g^3 + c_0Q_g^5 \quad (5.0)$$

Where:

$$a_0 = 2\alpha t_{fe} \quad (5.1.a)$$

$$b_0 = 4\beta t_{fe} \quad (5.1.b)$$

$$c_0 = 6\gamma t_{fe} \quad (5.1.c)$$
Reduction in polarization parameter alpha (Fig. 7) reduces both polarization field hysteresis and the “flip” \( V_{fe} \) range. From Eq. (5.0), reduction in alpha, reduces \( V_{fe} \), and electric field being proportional to \( V \), the expected reduction in polarization field hysteresis is observed.

Reduction in polarization parameter beta (Fig. 8) reduces both polarization field hysteresis and the “flip” \( V_{fe} \) range. From Eq. (5.0), reduction in beta reduces \( V_{fe} \) and electric field being proportional to \( V \), polarization field hysteresis is reduced. Eq. (5.0) indicates alpha impacts \( V_{fe} \) most significantly, proceeded by beta, and polarization parameter rho, having an insignificant effect on \( V_{fe} \), thus having an insignificant effect on polarization hysteresis. Comparing alpha and beta reduction in Fig. 7 and Fig. 8 respectively, confirms the analytical expression of polarization parameters effect on \( V_{fe} \) in Eq. (5.0), as alpha
Fig. 8: Polarization hysteresis vs. $V_{fe}$ of the pure ferroelectric capacitor, varying ferroelectric polarization parameter: beta.

reduction shows greater reduction in both $V_{fe}$ range and polarization field hysteresis compared to beta reduction. Furthermore, the polarization field hysteresis difference between alpha and beta reduction, is more pronounced at $V_{fe} = 0V$, than around at large magnitudes $V_{fe} = \pm 5V$.

3.2 The Series Ferroelectric-oxide Capacitor

Following study of the pure ferroelectric capacitor, addition of a series SiO2 layer to the ferroelectric capacitor allows study of the gate-stack of the ferroelectric nanowire explored in detail in chapter 4. For the proceeding structure, a voltage is applied to the ferroelectric or “gate” contact, and the SiO2 or “oxide” contact is grounded ($V @ “oxide contact” = 0V$) (Fig.9).
3.2.1 Ferroelectric-oxide Thickness Ratio Effect on $V_{fe}$ in Ferroelectric-oxide Capacitor

Fig. 10 shows the gate charge and the electrostatic potential difference, $V_{fe}$ across the ferroelectric layer in the series ferroelectric-oxide capacitor. The larger ferroelectric thickness results in a larger $V_{fe}$ swing in the ferroelectric layer, under the same gate bias. During the gate voltage ramp, a positive gate voltage induces a negative $V_{fe}$, i.e. a voltage gain across the ferroelectric layer. Negative capacitance in the ferroelectric layer exists when $V_{fe}$ increases while the gate charge decreases, or when $V_{fe}$ decreases while the gate charge increases, according the capacitor charge equation:

$$C = \frac{dQ}{dV} \quad (7.0)$$

The net electric field follows the behavior of $V_{fe}$ in the ferroelectric capacitor. Fig. 11 demonstrates the polarization field opposing the net electric field and gate charge, within the ferroelectric layer.
Fig. 10: $V_{fe}$ and gate charge vs time in ferroelectric-oxide capacitor.

Fig. 11: $V_{fe}$ and polarization field vs time in ferroelectric-oxide capacitor.
4 A METHOD FOR APPROACHING SUB-60 MV/DECADE SUBTHRESHOLD SLOPE

4.1 Capacitance Ratios & Narrowing the Design Space Analytically

The present section narrows the design space with manual calculations by quantizing the ferroelectric capacitance $C_{fe}$, oxide capacitance $C_{ox}$ and total ferroelectric-oxide gate-stack capacitance $C_{f,ox}$ range in the subthreshold region, necessary to meet the sub 60 mV/decade subthreshold slope target. Subthreshold slope of an FeFET, is given by Eq. (1.0):

$$S.S. = \frac{\frac{KT}{q}}{\ln(10)} \cdot (1 + \frac{C_{si}}{C_{f,ox}})$$  \hspace{1cm} (1.0)

Where,

$$n = (1 + \frac{C_{si}}{C_{f,ox}})$$  \hspace{1cm} (1.2)

More specifically, targeting sub 60 mV/decade S.S. requires an S.S. between $0 \rightarrow 60$ mV/decade, an $n$ less than 1, and a negative $C_{fe}$ in the subthreshold region. As $(\frac{KT}{q}) \cdot \ln(10) = 60$ mV/decade, $n$ less than 1 enables a sub 60 mV/decade S.S. Furthermore, with a positive $C_{si}$ and an effective negative gate-stack capacitance, $C_{f,ox}$ in Eq. (1.2), gives an $n$ value less than 1; and $n$ less than 1 in Eq. (1.0) gives a sub-60 mV/decade subthreshold slope. Achieving $n$ less than 1 requires negative $C_{f,ox}$, where $C_{f,ox}$ equals:

$$C_{f,ox} = \frac{C_{fe} \cdot C_{ox}}{C_{fe} + C_{ox}}$$  \hspace{1cm} (4.0)

And, $C_{ox}$ is constant and positive and equals:

$$C_{ox} = \frac{E_{ox}}{t_{ox}}$$  \hspace{1cm} (3.0)

Because $C_{ox}$ remains constant, $C_{fe}$ range is determined as a ratio of $C_{fe}$ and $C_{ox}$. Finding the ratio $\frac{C_{fe}}{C_{ox}}$, enables the engineer to choose an appropriate ferroelectric and oxide thickness corresponding to the $\frac{C_{fe}}{C_{ox}}$ ratio in the subthreshold region to obtain a sub-60 mV/decade S.S. The proceeding analytical steps narrow the design space by
finding ferroelectric, oxide, total gate-stack, and silicon channel, capacitor ratios necessary for achieving a target sub 60 mV/dec S.S:

I Set S.S. target range between $0 \rightarrow 60\text{mV/decade}$, resulting in an $n$ range between 0 and 1 Eq. (1.0).

II Substituting Eq. (1.2) in $0 < n < 1$, gives:

$$1 > (1 + C_{si}/C_{fox}) > 0 \quad (1.2.1)$$

Using a negative $C_{fox}$, solve for $C_{fox}$ as a function of $C_{si}$:

$$1 > \left| \frac{C_{si}}{C_{fox}} \right| \quad (1.2.2)$$

$$\left| C_{fox} \right| > C_{si} \quad (1.2.3)$$

& $C_{fox} < 0 \quad (1.2.4)$

$$\left| \frac{C_{fox}}{C_{si}} \right| > 1 \quad (1.2.4)$$

Eq. (1.2.3) & Eq. (1.2.3) can be re-written as:

$$\frac{C_{fox}}{C_{si}} < -1 \quad (1.2.6)$$

III Find the $\frac{C_{fe}}{C_{ox}}$ range under the $\frac{C_{fox}}{C_{si}} < -1$ design constraint using Eq. (4.0):

$$C_{fox} = \frac{C_{fe} \times C_{ox}}{C_{fe} + C_{ox}} \quad (4.0)$$
Fig. 12: shows $C_{fe}/C_{ox}$ between -1 and -0.5 achieves $C_{fox} < -1$ with $C_{SiO2}=1$.

IV Find the n and S.S. range under the $C_{fe}/C_{ox}$ between -1 and -0.5, design constraint

Fig. 13: n range vs. $C_{fe}/C_{ox}$, with $C_{fe}/C_{ox}$ range between -1 and -0.5 to achieve $C_{fox} < -1$. 
Fig. 14: S.S. range vs. $C_{fe}/C_{ox}$, with $C_{fe}/C_{ox}$ range between -1 and -0.5 to achieve $C_{f_{ox}} < -1$.

The above analytical steps analytically derive and graph the ferroelectric, oxide, and silicon capacitance relationships in Fig.12, Fig13 and Fig.14. Table 1 summarizes the capacitance-ratio based design rules to optimize the FeNW for a sub-60 mV/decade subthreshold slope.

Table 1: Design Rules, Constraints and Ranges for Achieving 60 mV/decade Subthreshold Slope

<table>
<thead>
<tr>
<th>Design Rule</th>
<th>Design Constraint and/or Capacitance Ratio</th>
<th>Range Constraint for sub 60 mV/decade S.S.</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>S.S.</td>
<td>$0 : 60 \text{ mV/decade}$</td>
</tr>
<tr>
<td>#2</td>
<td>$n = (1 + \frac{C_{si}}{C_{f_{ox}}})$</td>
<td>$0 : 1$</td>
</tr>
<tr>
<td>#3</td>
<td>$\frac{C_{fe}}{C_{ox}}$</td>
<td>$-1 : -0.5$</td>
</tr>
<tr>
<td>#4</td>
<td>$C_{f_{ox}}$</td>
<td>$&lt; 0$</td>
</tr>
<tr>
<td>#5</td>
<td>$\frac{C_{f_{ox}}}{C_{si}}$</td>
<td>$&lt;-1$</td>
</tr>
</tbody>
</table>
4.2 Spotting the Negative Capacitance Region

4.2.1 Looking at Ferroelectric Nanowire Cutline

Fig. 15: Ferroelectric nanowire 2D planar structure in TCAD structure editor.

Fig. 16: Cutline plot of electrostatic potential across ferroelectric nanowire.

Fig. 16 shows the electrostatic potential perpendicular to the channel length of the FeNW. The right end of the electrostatic potential curve in Fig.16, labeled “Gate Contact on Ferro layer” corresponds to the Vg contact in Fig.15. Fig.16. shows the electrostatic potential cutline plot with 5V applied to the gate contact. The cutline plot demonstrates a positive $V_{fe}$, or a voltage gain across the ferroelectric layer in the FeNW, preceding a
voltage drop in the oxide and Silicon channel. The voltage gain in the FeNW’s FeCAP, enables a negative capacitance, improves the FET’s current drive, thus improving the FET’s subthreshold slope.

4.2.2 Spotting Negative Capacitance in Subthreshold Region

To improve subthreshold slope, a large $C_{foox}$ converges subthreshold slope to, but just above, 60 mV/decade. To achieve sub-60 mV/decade subthreshold slope, a negative $C_{foox}$, with a magnitude greater than $C_{si}$ must be attained under the conditions derived in section 4.1. Moreover, attaining the target negative $C_{foox}$ in the subthreshold region presents in colloquial terms: a narrow design space. The present section demonstrates a method using capacitor ratio optimization to attaining sub 60 mV/decade subthreshold slope. Fig.17 imposes the gate charge vs Vg plot, on the Id-Vg curve for three different ferroelectric thickness splits, all with an oxide thickness of 0.5 nm. The three ferroelectric thickness splits in Fig.17 are shown for redundancy in observing consistent FeCAP behavior in the FeNW subthreshold region. All 2 ferroelectric thickness splits demonstrate a subthreshold slope converging to, but above 60 mV/decade (Table 2). Focusing analysis on $t_{fe} = 6$ nm (red curves), box A in Fig.17 highlights a negative capacitance region, when gate voltage increases and gate charge decreases, confirmed by Eq. (7.0):

$$C_{foox} = \frac{dQ}{dV} \quad (7.0)$$

Achieving a negative capacitance enables convergence to, but greater than, 60 mV/decade. As derived in section 4.1 referring to Eq (4.0), a negative $C_{fepsilon}$ greater than $C_{ox}$, increases the numerator in magnitude, while decreasing the denominator, resulting in a large, positive $C_{foox}$, where a large positive $C_{foox}$ in Eq. (1.2) converges n to 1 thus, converging the subthreshold slope in Eq. (1.0) to 60 mV/decade. This Phenomena is confirmed in the Id-Vg behavior observed in similar current per voltage change in Fig.17 and the corresponding subthreshold slopes calculated in Table 2, where all three thickness splits
demonstrate a negative capacitance in the subthreshold region and converge to a 60 mV/decade subthreshold slope.

\[ C_{fox} = \frac{C_{fe} \cdot C_{ox}}{C_{fe} + C_{ox}} \quad (4.0) \]

\[ S.S. = \left( \frac{KT}{q} \right) \cdot \ln(10) \cdot \left( 1 + \frac{C_{si}}{C_{fox}} \right) \quad (1.0) \]

\[ SS_{norm} = \frac{KT}{q} \cdot \ln(10) \cdot \left( 1 + \frac{C_{si}}{C_{ox}} \right) \quad (1.2) \]

Fig. 17: Gate charge and drain current vs \( V_g \) of ferroelectric nanowire.

Table 2: Subthreshold Slopes of 3 \( t_{fe} \) Splits w/ \( t_{ox} = 0.5 \) nm

<table>
<thead>
<tr>
<th>( t_{fe} ) (nm)</th>
<th>S.S.(mv/Dec)</th>
<th>Vth(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>60.56193074</td>
<td>0.688156</td>
</tr>
<tr>
<td>4</td>
<td>60.56190374</td>
<td>0.61588497</td>
</tr>
<tr>
<td>2</td>
<td>60.69432505</td>
<td>0.59984935</td>
</tr>
</tbody>
</table>
4.3 Confirming Sub-60 mV/dec S.S. Analytical Conditions with the Capacitance Ratio & Id-Vg Overlap

The present section analyzes the capacitor ratios in the subthreshold region of a sub-60 mV/decade FeNW with the following configuration:

Table 3: Sub-60 mV/decade FeNW TCAD Design Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{fe} )</td>
<td>6 nm</td>
</tr>
<tr>
<td>( t_{ox} )</td>
<td>0.5 nm</td>
</tr>
<tr>
<td>tSI</td>
<td>3 nm</td>
</tr>
<tr>
<td>( \varepsilon_{OX} )</td>
<td>39 ( F/M )</td>
</tr>
<tr>
<td>( g_{wf} )</td>
<td>5.1 eV</td>
</tr>
<tr>
<td>ND</td>
<td>1.00E+19</td>
</tr>
<tr>
<td>( V_d )</td>
<td>0.1 V</td>
</tr>
<tr>
<td>( V_g )</td>
<td>5 V</td>
</tr>
<tr>
<td>alpha</td>
<td>-5.81E+10</td>
</tr>
<tr>
<td>beta</td>
<td>7.27E+19</td>
</tr>
<tr>
<td>S.S.(mV/Dec)</td>
<td>38.6235311</td>
</tr>
<tr>
<td>Vth(V)</td>
<td>0.98137574</td>
</tr>
</tbody>
</table>

To understand attaining sub-60 mV/dec S.S., see Chapter 5 which explores design trade-offs and optimizing the FeNW for S.S. The proceeding analysis uses TCAD simulation data to extract the ferroelectric, oxide and silicon channel capacitance of the FeNW from Table 3. Filtered TCAD capacitance ratio data, imposed on the Id-Vg curve, within the analytical design constraint ranges, verify if sub-60 mV/decade S.S. from TCAD, meets our analytical design constraints from section 4.1, conveyed in Table 1. Fig.19, Fig.20 and Fig.21 correspond to the analytical design ranges imposed by section 4.1 by extracting TCAD data in the section 4.1 design constraint ranges given by Table 1, and overlapping the capacitance ratio onto the Id-Vg curve under the same gate voltage bias’. The vertical, dashed orange line in Fig.19, Fig.20 and Fig.21, denote the threshold voltage of 0.98V, as seen in Table 3
Fig. 18: 38.6 mV/decade subthreshold slope $I_d-V_g$ curve.
Design Rule #1: Attaining subthreshold slope between 0 and 60 mV/decade.

A subthreshold slope of 38.62 mV/decade achieved, as seen in Table 3.

Design Rule #2: n range between 0 and 1

Fig. 19 shows derived n values between 0 and 1 values from TCAD simulation in the subthreshold region. N values less than 1 achieve sub 60 mV/decade S.S. according to Eq. (1.0).

Fig. 19: n & Id vs $V_g$ for table 3 FeNW.
Design Rule #3: \( \frac{C_{fe}}{C_{ox}} \) range = -1 : -0.5

Fig. 20 shows extracted \( C_{fe} / C_{ox} \) points between -0.5 and -1 in the subthreshold region. Therefore, according to Eq. (4.0), a negative \( C_{fox} \), necessary for \( n < 1 \) and sub-60 mV/dec S.S. is attainable.

Fig. 20: \( C_{fe} / C_{ox} \) & Id vs Vg for table 3 FeNW.
Design Rule #4 & #5:  $\frac{C_{fox}}{C_{Si}} < -1$, w/ $C_{fox} < -1$

Fig. 21 shows $\frac{C_{fox}}{C_{Si}}$ less than and greater in magnitude, than -1 which enables an n value less than 1, and a sub-60 mV/decade S.S.

Fig. 21: $C_{fox} / C_{Si}$ & Id vs $V_g$ for table 3 FeNW.
Chapter 4 presented methods to approaching and attaining sub-60 mV/decade S.S. We know a sub-60 mV/dec S.S. is attainable with a ferroelectric nanowire however, understanding design tradeoffs and conditions which S.S. improvement is possible, gives a device engineer and/or research physicist insight into the limitations and possible applications of ferroelectric nanowires and more generally, ferroelectric FETs. Chapter 5 varies design parameters: $t_{fe}$, $t_{ox}$, gate work function, ferroelectric polarization parameters, device temperature and bias conditions to study design variable effects on ferroelectric behavior, and FeNW performance metrics including subthreshold slope, threshold voltage and hysteresis.

5.1 Ferroelectric Layer Thickness Effect

The present section observes the effect of various $t_{ox}$ and $t_{fe}$ splits on the FeNW S.S. Larger oxide thickness splits worsen S.S. and for large oxide thickness’ ($t_{ox} = 1 \& 1.5$ nm), a large $t_{fe}$ , also worsens S.S. However, increasing $t_{fe}$ for thinner oxides ($t_{ox} = 0.5$ nm & 0.6 nm) does not have significant impact on the subthreshold slope, as S.S. thinner oxide with thicker ferroelectric layers, still converge to 60 mV/decade for a gate work function of 4.75 eV.
Fig. 22: Subthreshold slope vs \( t_{fe} \) for 4.75 eV gate work function.

### 5.2 Gate Work Function Effect

Fig. 23: Gate work function effect on Id-\( V_g \) and threshold voltage.
Reducing the gate work function of the FeNW decreases threshold voltage as seen in Fig.23 which is also true for a traditional FET. Reduction of the gate work function below 5.1 eV, has insignificant effect on the subthreshold slope as seen in the red, blue and green curves of Fig.23, and confirmed in the S.S. vs Vth scatter plot of Fig.24. However, the Figure 2 Id-Vg curve, shows a S.S. improvement for a 5.1 eV work function, which is confirmed in the increased S.S. design space in Fig.24 at, and above a work function of 5.1 eV. However, Fig.25 shows the threshold voltage ranges for our device when we use a work function of 5.1 eV and above.

Fig. 24: Subthreshold slope vs gate work function design space trade-off across 3 $t_{Fe}$ splits.
Fig. 25: Threshold voltage vs gate work function design space trade-off across 3 $t_{fe}$ splits.

Although all work functions below 5.1 eV converge within 3 mV/decade of 60 mV/decade S.S., achieving a sub-60 mV/decade S.S. significantly narrows the design space. While our analysis in section 5.1 and 5.2 reveals designing a FeNW with low S.S. forces a high Vth, we see that integrating a ferroelectric layer in series with a thick oxide in the gate-stack of a nanowire converges the subthreshold slope to 60 mV/decade under many gate work function splits, and we have flexibility in choosing a metal gate work function to design for a specific threshold voltage for our FeNW according to Fig.25.
5.3 Ferroelectric Polarization Parameter Effect

Reducing the magnitude of ferroelectric polarization parameter alpha, has the greatest effect on reducing the FeNW threshold voltage. Reducing polarization parameter beta reduction also exhibits threshold voltage reduction with a 4.75 eV gate work function.

Fig. 26: Threshold voltage vs ferroelectric polarization parameter beta, for various alpha values with a 4.75 eV gate work function.
Fig. 27: FeNW ferroelectric polarization parameter and gate work function vary split table.
We observed in the pure FeCAP from section 3.1.2 and again in Fig.28 for the FeNW, polarization parameter alpha carries the greatest impact on coercive field strength, according to the LK equation Eq. (5.3)

\[ E = 2\alpha P + 4\beta P^2 + 6\gamma P^5 - 2g\Delta P + \rho \frac{dP}{dt} \]  \hspace{1cm} (5.3)

In the Fig.27, an alpha parameter of -5.81E+10, corresponding to the red curve in Fig.28, has a S.S. of 61.38 mV/decade, and reduced alpha values -2.9E+10 and -2.0E+10, have S.S. of 60.63 mV/decade and 60.69 mV/decade respectively. Fig.28 shows Id-Vg curves over a hysteresis cycle initialized at \( V_g = -1V \), swept to \( V_g = 1V \), and returning to \( V_g = -1V \). Largest alpha Id-Vg curve exhibits a S.S. 1% greater than lower alpha values -2.9E+10 and -2.0E+10, and current hysteresis during Ion. Lower alpha values -2.9E+10 and -2.0E+10, do not exhibit strong Ion hysteresis, but show large hysteresis, and noise during \( I_{off} \).

Fig. 28: FeNW Id-Vg curve, varying alpha. black arrows denote \( V_g \) increase or decrease.
5.4 Temperature Effect

Fig. 29 to Fig. 31 each show approximately 375 FeNW splits including varying gate voltages between 1V and 5V, drain voltages varying between 0.1V and 2V, gate work functions varying between 4 eV and 4.25 eV, for $t_{fe} = 6$ nm, 7 nm and 8 nm. Below a critical threshold voltage, all FeNW splits converge to $\frac{Kt}{q} \approx 60$ mV/decade for $T=300K$, $T=200K$ and $T=100K$. For FeNW designs with threshold voltages, above critical $V_{th}$, sub-60 mV/decade S.S. is attainable across all ferroelectric thickness splits and bias conditions. Higher threshold voltage splits exhibit strong correlations with higher gate work functions.
Fig. 30: Subthreshold slope vs Vth @ T=200K ($t_{fe}= 7$ nm splits not run at higher gate voltages for this project).

Fig. 31: Subthreshold slope vs Vth @ T=100K ($t_{fe}= 7$ nm splits not run at higher gate voltages for this project).
Fig. 32: S.S. vs temperature design space trade-off with the varied device temperatures.

Fig. 33: S.S. vs threshold voltage design space trade-off with the varied temperatures.
5.5  Bias-Voltage Effect

Fig.34 Id-Vg curve demonstrates that drain voltage variation does not impact subthreshold slope in the FeNW. Drain voltage reduction, lowers Ion during saturation. \( V_d = 2V \) also shows least \( I_{off} \) current and noise.

![Id-Vg curve with varied Vd.](image)

Fig. 34: Id-Vg curve with varied \( V_d \).
6 CONCLUSIONS

The research objective was to optimize a ferroelectric nanowire to achieve a sub 60 mV/decade subthreshold slope and understanding the design trade-offs during subthreshold slope reduction. Our research champions the capacitor ratio method in the subthreshold region to reduce subthreshold slope. Study of the pure ferroelectric capacitor reveals alpha and $t_{fe}$ reduction have the strongest effect on reducing hysteresis in the ferroelectric capacitor. Furthermore, alpha reduction lowers threshold voltage in the ferroelectric nanowire. In the ferroelectric-oxide capacitor, larger ferroelectric thicknesses result in a greater electrostatic potential difference across the ferroelectric layer and show a weaker gate charge swing compared to thinner ferroelectric capacitors over the same applied voltage range. In chapter 4 we analytically narrow the design space for achieving sub 60 mV/decade subthreshold slope. To achieve a sub 60 mV/decade subthreshold slope, we need $n$ between 0 and 1, a negative $C_{fox}$, where $C_{fox} / C_{si} < -1$, and a negative $C_{fe}$, where $C_{fe} / C_{ox}$ is between -1 and -0.5. To confirm the analytical design rules, a 39.8 mV/decade FeNW is attained, using a gate work function of 5.1 eV. We superimpose TCAD capacitance ratio data on the FeNW Id-Vg by extracting capacitance ratios in the analytical design rule range and confirm that sub 60 mV/decade FeNW capacitance ratios adhere to our design rules in the subthreshold region. After achieving and characterizing sub 60 mV/decade S.S. FeNW behavior, we run splits to gain statistics to understand design trade-offs when attaining sub 60 mV/decade S.S. Using FeNWs with work functions below 5.1 eV allows convergence which approaches, but is greater than 60 mV/decade S.S. Above the critical 5.1 eV gate work function, the design space opens, and sub 60 mV/decade S.S. is achievable across various ferroelectric thickness ratios, and bias conditions. We then observe that the FeNW subthreshold slope follows a linear $kT/q$, improvement with temperature reduction.
7 FUTURE WORK

Beating the S.S./Vth Trade-off: Sub 60 mV/decade S.S. was achieved with a trade-off in Vth. Beyond this thesis, additional design variables including doping concentration, polarization parameters, $t_{fe}$, $t_{ox}$ are being explored to combat the Vth trade-off and attain sub-60 mV/decade S.S. with low Vth necessary for low power, high speed applications.

Sprocess: The present research was conducted in TCAD sdevice to understand design parameters impact on FeNW performance. Next, this research’s device, should be simulated in TCAD sprocess to understand optimize the ferroelectric fabrication process and understand its limitations.

Feature Scaling with FeFETs: More experiments should be run while reducing the gate length. This research’s goal was to improve performance without feature scaling, however integrating ferroelectric layers on sub-micron FETs may allow feature scaling while also scaling CPU frequency.

Ferroelectricity in Analog IC: Integrating a FeFET compact model in analog circuits. We show that ferroelectric material improves subthreshold slope and current drive, with a voltage enhancement from the ferroelectric layer of the FeFET. Researching and comparing FeFET and traditional MOSFET’s metrics, such as clock skew, jitter, and noise margin can give provide circuit designers new process design kits suitable for high-frequency circuit design.
References


